# SiC, GaN and more: Probing Technologies for HV-HC Power Devices

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# Overview

- Intro: power devices
- Probing challenges: High Voltage, High Current
- Arcing suppression: LuPo pressure chamber technology
- High Current – contact technologies
- Overcurrent and "burn" protection: SmartClamp
- Single-site vs. multi-site wafer test
- Known Good >>POWER<< Die (KGD)
- Summary and Outlook

# Power Devices

- **Where are these used ?**
  - Electric Vehicles (EVs): cars, trains, ships, (future)aircraft...
  - Renewable Energies – solar, wind, hydrogen
  - Efficcient power supplies: computing, chargers, mobile...

photo courtesy: Wolfspeed

- **Types**
  - discretes: MOSFETs, IGBTs, Diodes,
  - ICs: gate drivers, switching power supplies

- **Why SiC, GaN?**
  - very fast switching with little power loss, allows for
  - much smaller and energy efficient circuits

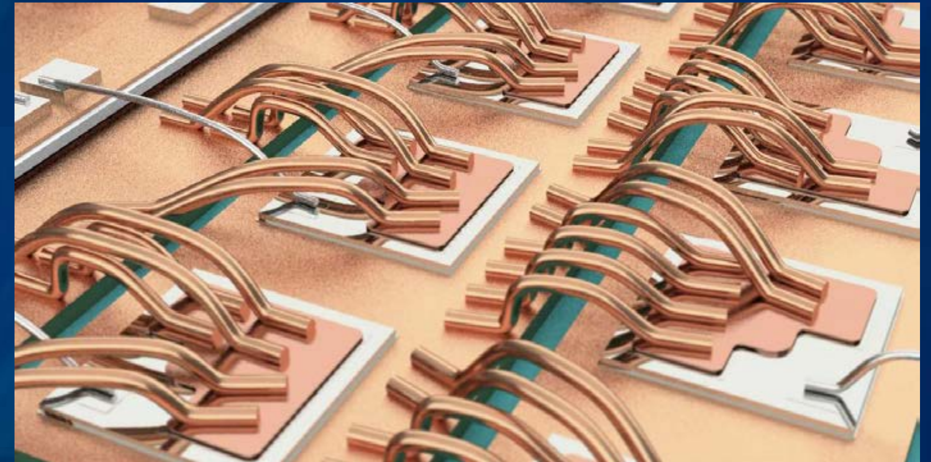
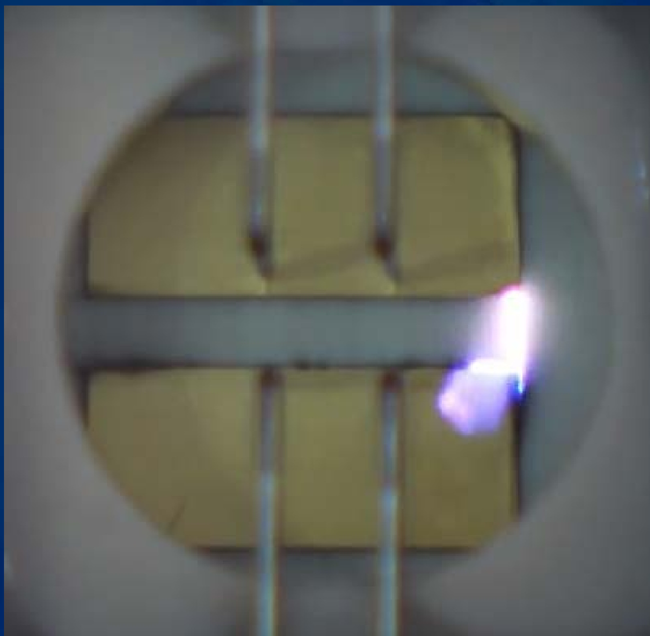


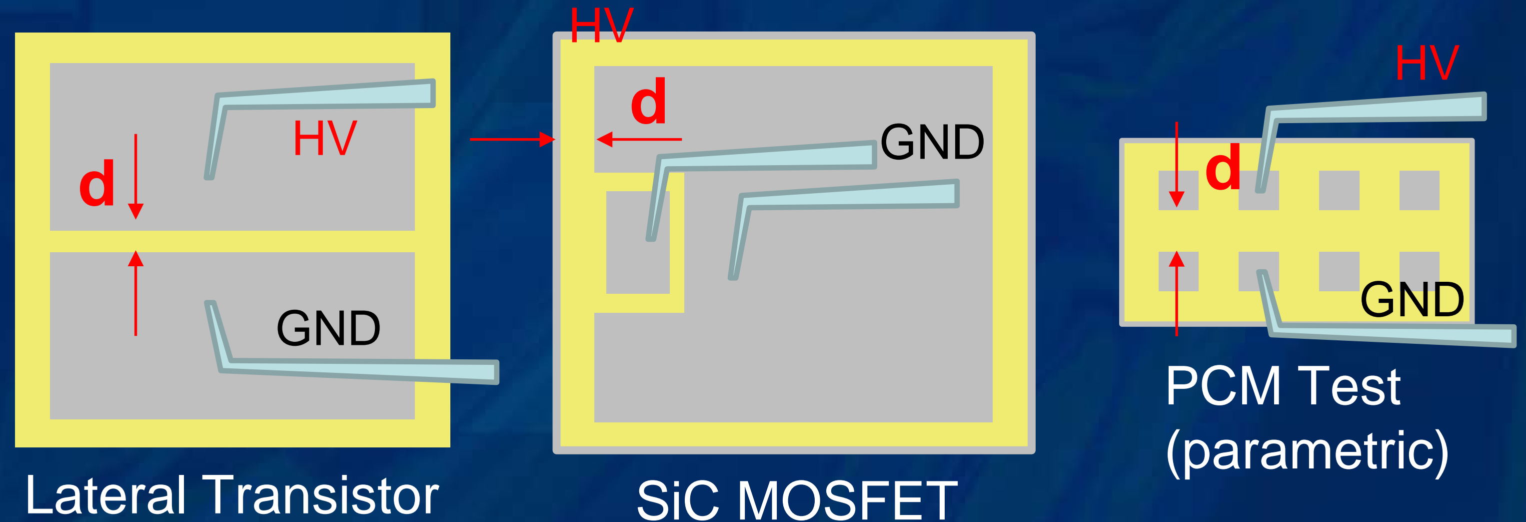
photo courtesy: ABB

- **Why still Si?**
  - extremely robust and well proven: IGBTs, Diodes for automotive and industrial drive trains

# Probing Challenges: High Voltage

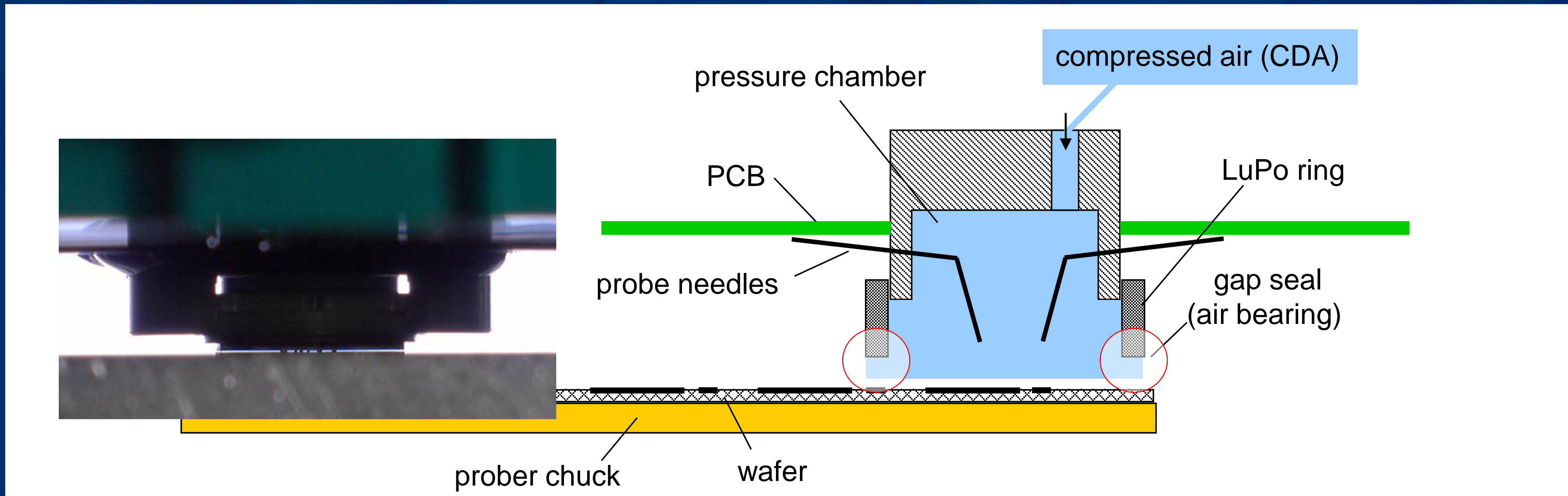
- **High Voltage Arcing**
  - test voltages: several 100 V to several kV
  - SiC and GaN: "wide bandgap" semiconductor material allows for narrow HV structures (distance d) compared to traditional Si devices -> high arcing risk at wafer probing or at KGD test





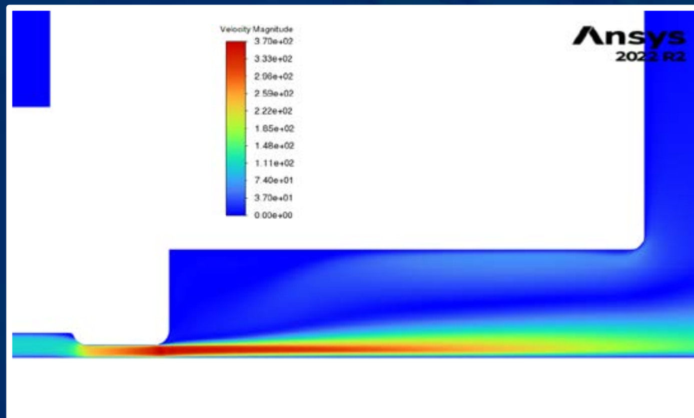
# Arcing Suppression: LuPo technology

- **"Applied Paschen": chip-scale pressure chamber**
  - uses compressed air (CDA) to suppress arcing
  - environmentally "green"
  - low operating cost



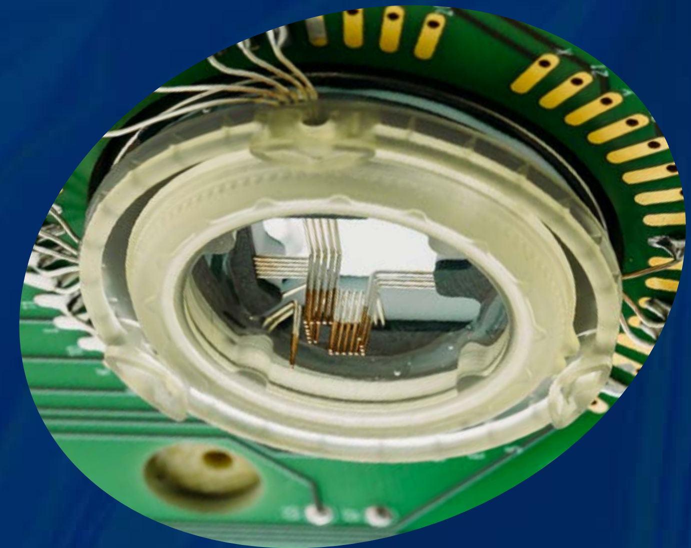
# LuPo Technology – Insights...

- **Air-Bearing-Seal (LuPo-ABS)**
  - LuPo floats on air cushion – NO TOUCH of wafer surface
  - Auto-z align, insensitive to overtravel setting and probe tip wear
  - Latest version "Gen.4" - applied CFD simulation and 3D printing technology: optimized floating and pressure buildup, low noise and CDA consumption, insensitive to wafer-born particle contamination




CFD simulation for the LuPo air bearing structure

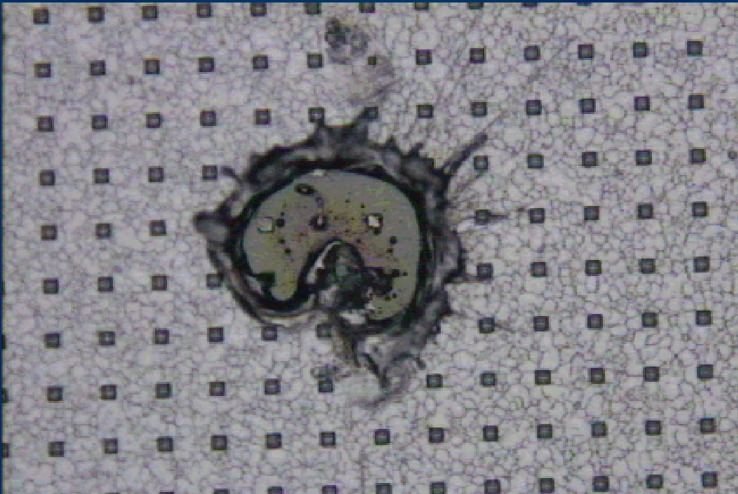
NO TOUCH: LuPo contacting motion



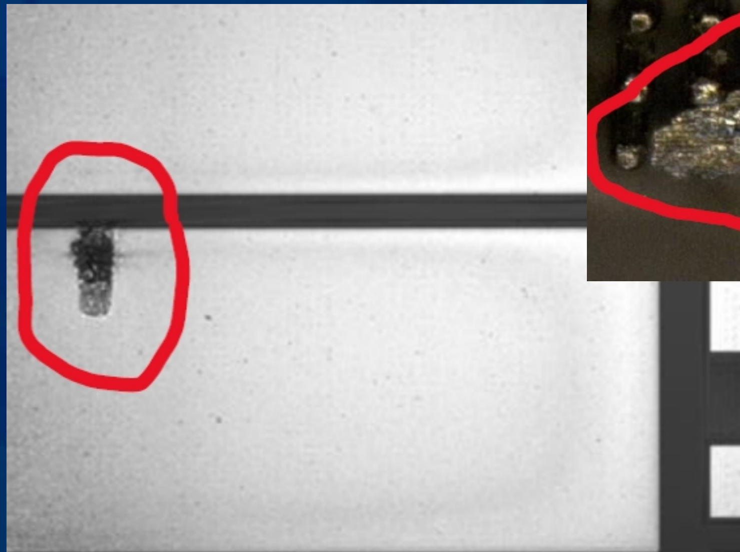
LuPo "Gen.4"

# Probing Challenges: High Current

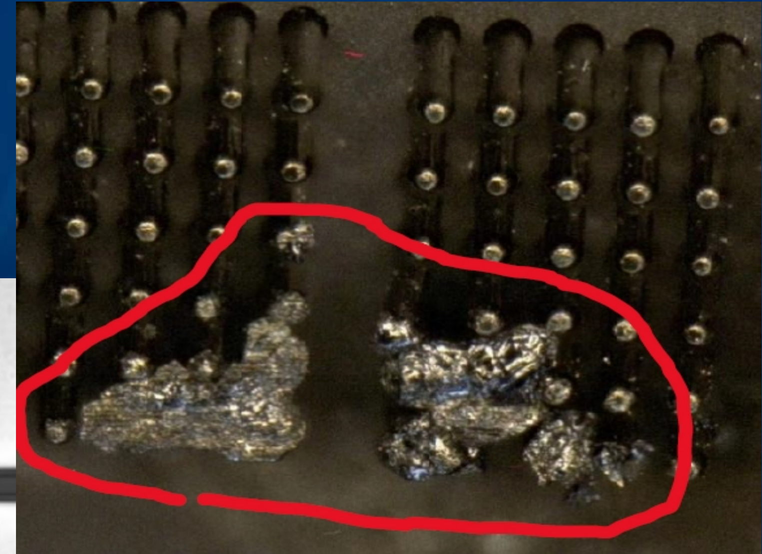
- **"Chip burn", probes damage**
  - test currents: a few A to 3000+ Amps!



molten chip pad on IGBT (wafer test, cantilever probes)



"chip burn" (KGD test)

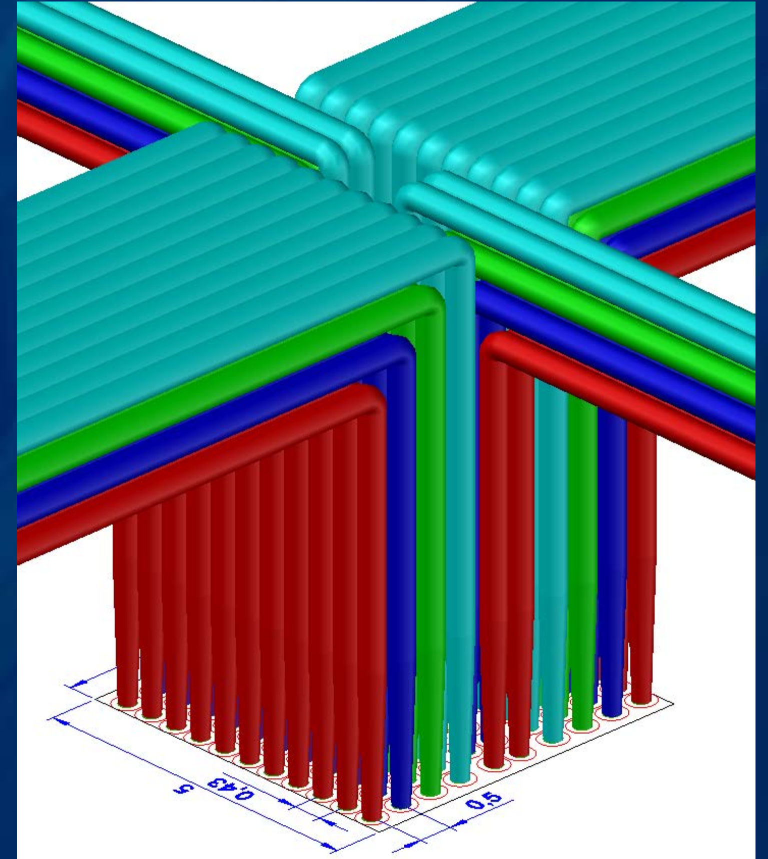


chip metal fused to HC vertical probes (KGD test)

# High Current – Cantilever vs. Vertical (1)

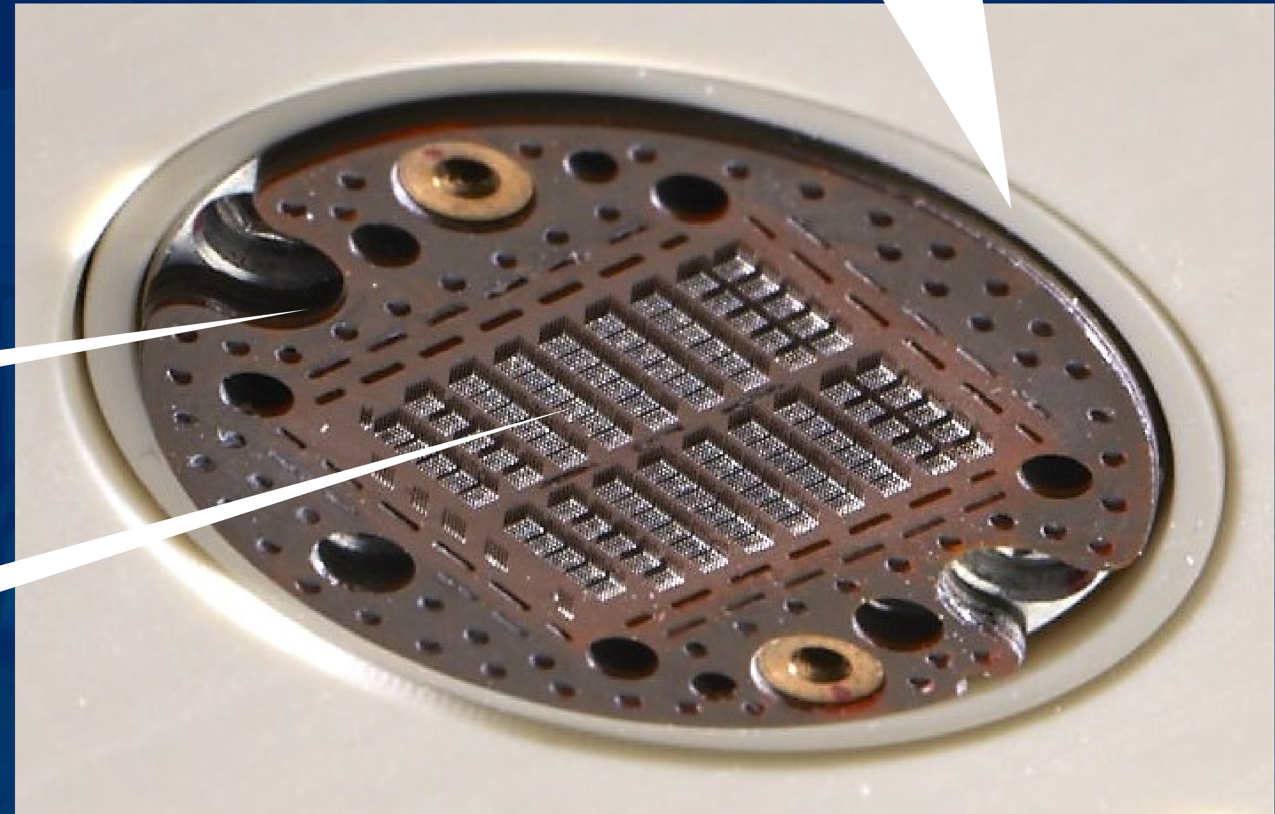
- **Cantilever probes technology: the robust "workhorse"**
  - limited max. current density ~ 40 A/mm$^2$ might be too low for SiC power devices
  - good choice for Si-IGBTs, diodes
  - comparably low cost

1600 A Cantilever probe card for IGBT



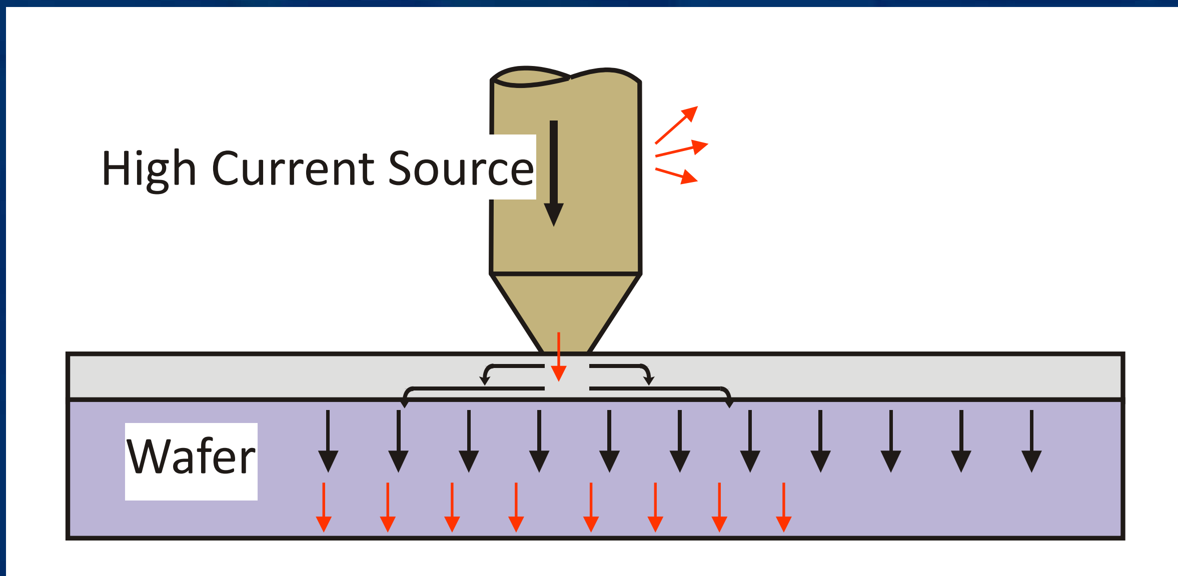
# High Current – Cantilever vs. Vertical

- **Vertical probes technology: highest current densities**
  - highest current density: 80+ A/$mm^2$: SiC, AC tests for KGD
  - very homogeneous current distribution over chip surface
  - small and shallow probe marks
  - well proven "buckling beams"
  - allows for small pad sizes (SiC, GaN based ICs, PCM...)

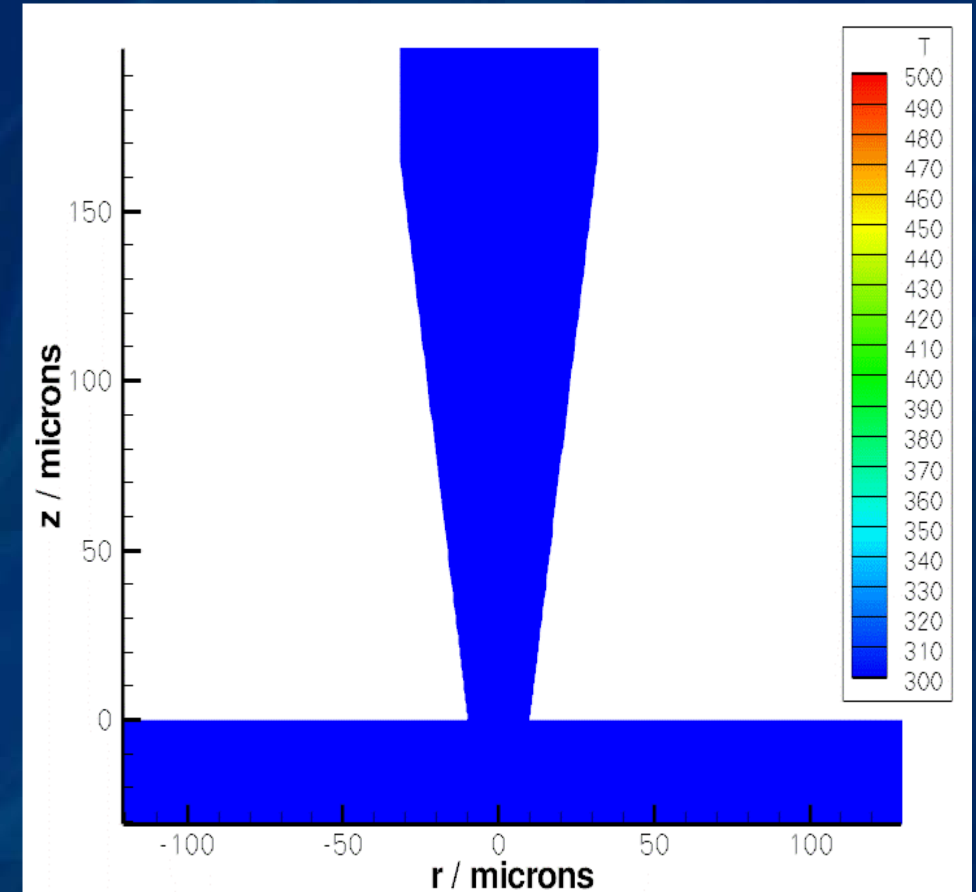


# High Current – "Burn Protection"

- **First steps: knowing what's going on...**
  - electro-thermal simulation of probe-wafer
  - for short high current pulses
  - include contact resistance model (Cres)
  - lab verification

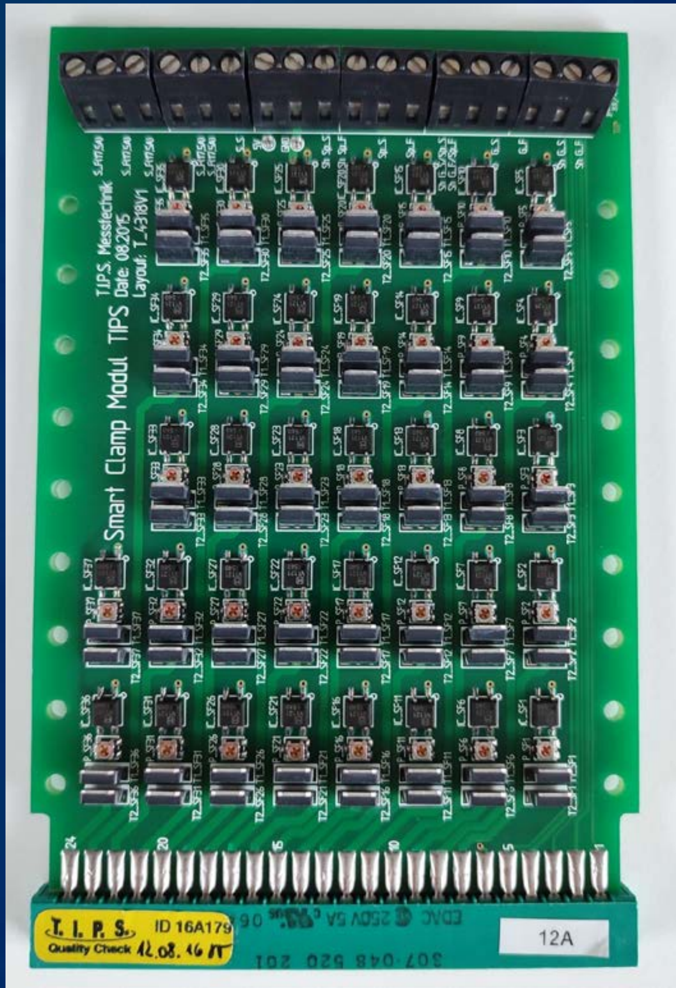



electro-thermal modeling of probe-wafer system



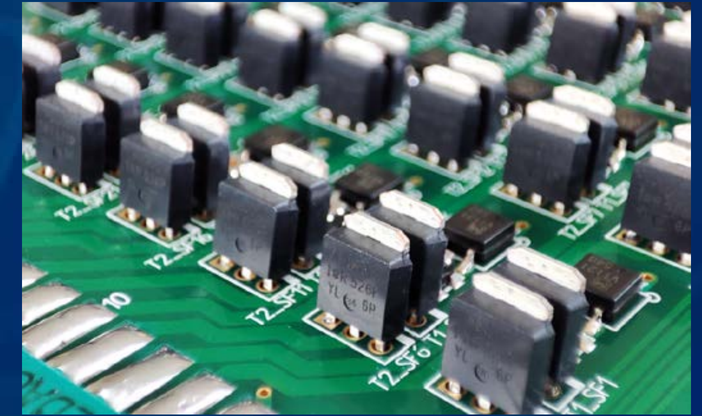

FEM simulation: (vertical beam) probe tip and pad heating
high current pulse train 10x 3 ms / 2A

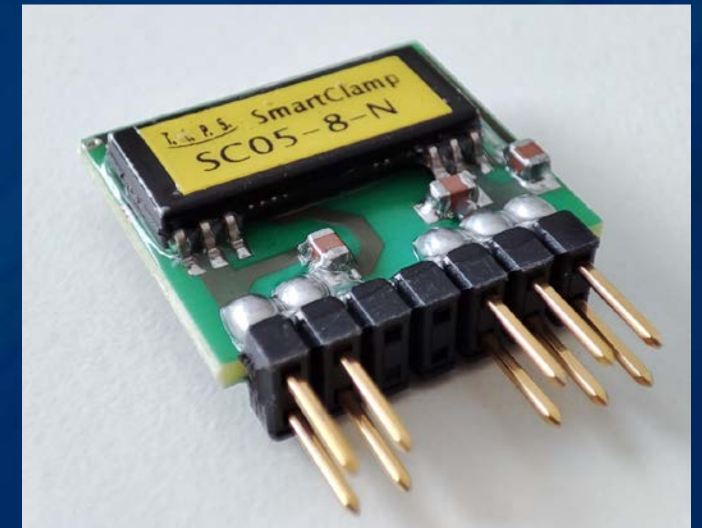
# SmartClamp – Overcurrent Protection




370 A SmartClamp Module

- Probe protection circuitry for TIPS High Current probe cards.
- protects each probe (or groups of probes)
- prevents probe / pad contact current overload caused by imbalanced probe currents or tester overshoot
- Active current balancing
- bi-directional current protection

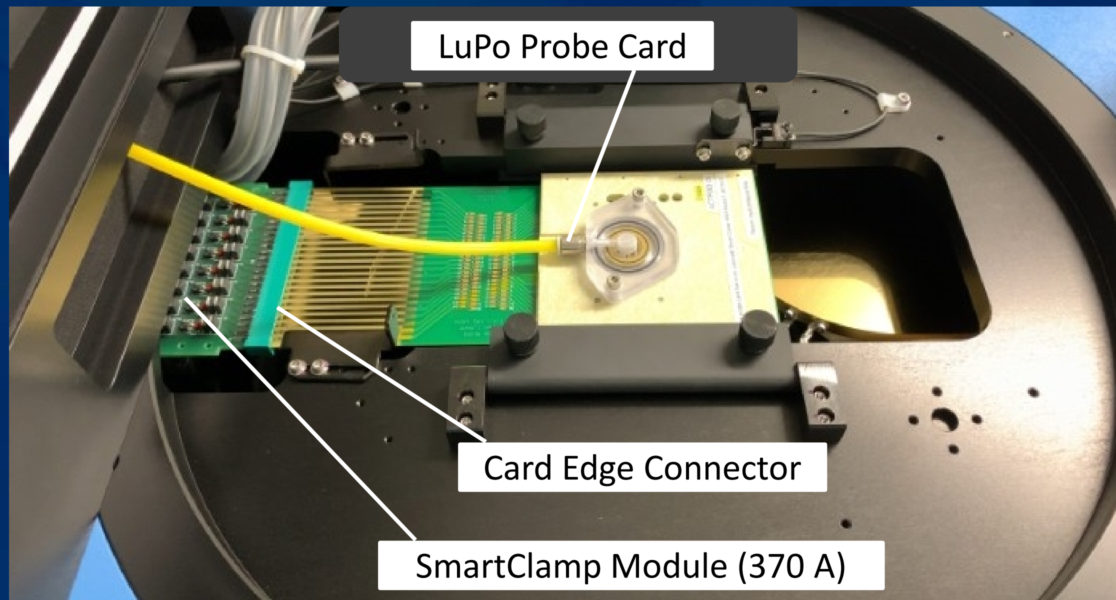




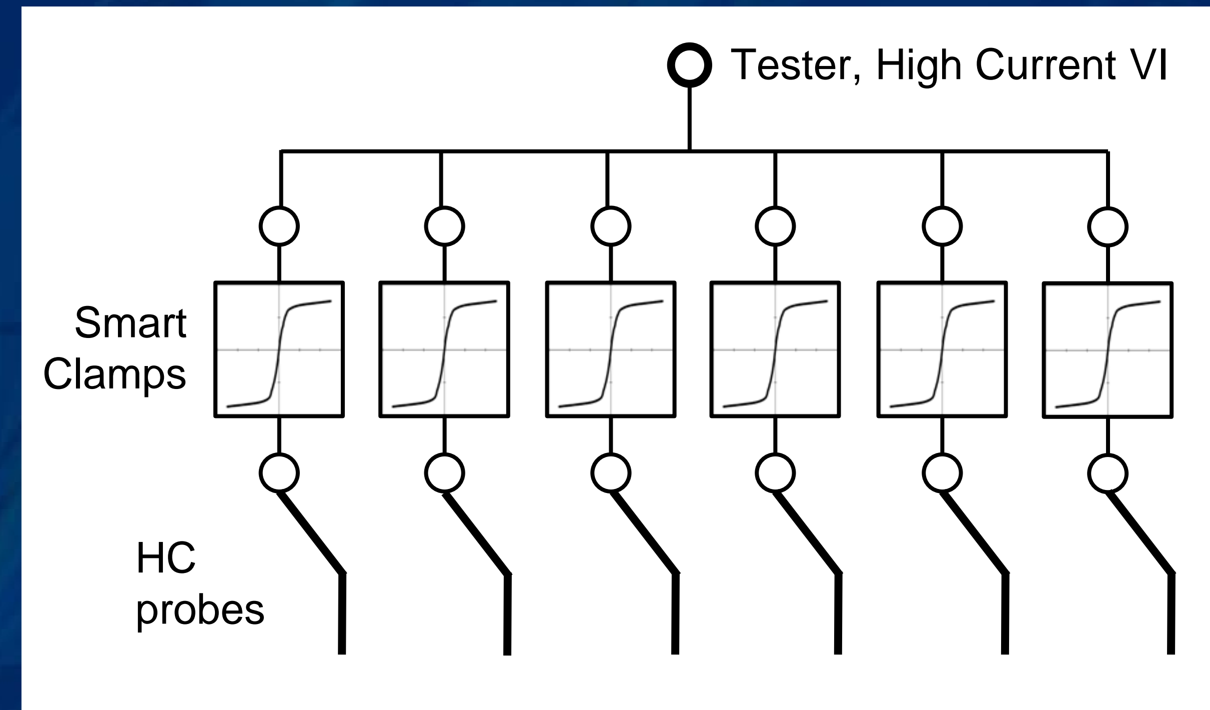

SmartClamp for Load Boards

# SmartClamp – Implementation

- **Probes Protection**
  - connected in series to each probe (Cantilever) or cluster of probes (Vertical)



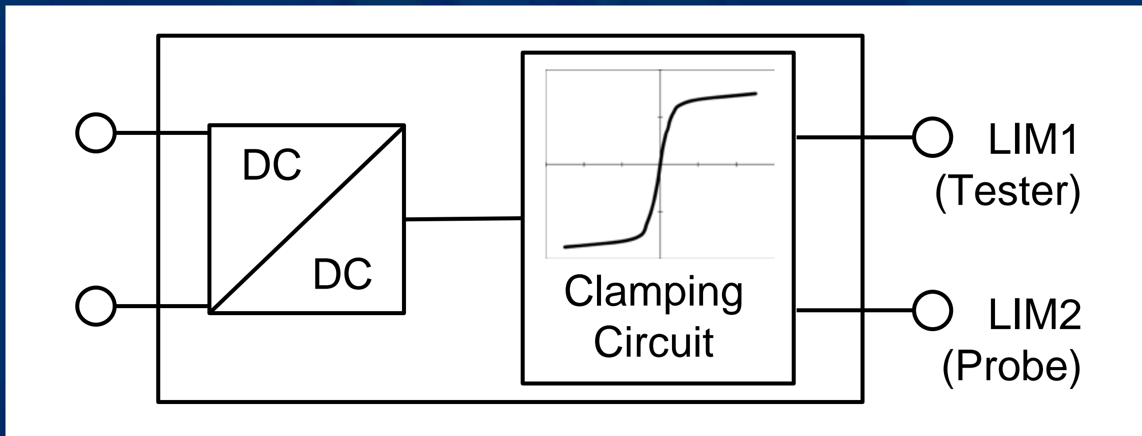

SmartClamp Module 370 A
setup with probe card on Accretech UF2000 prober



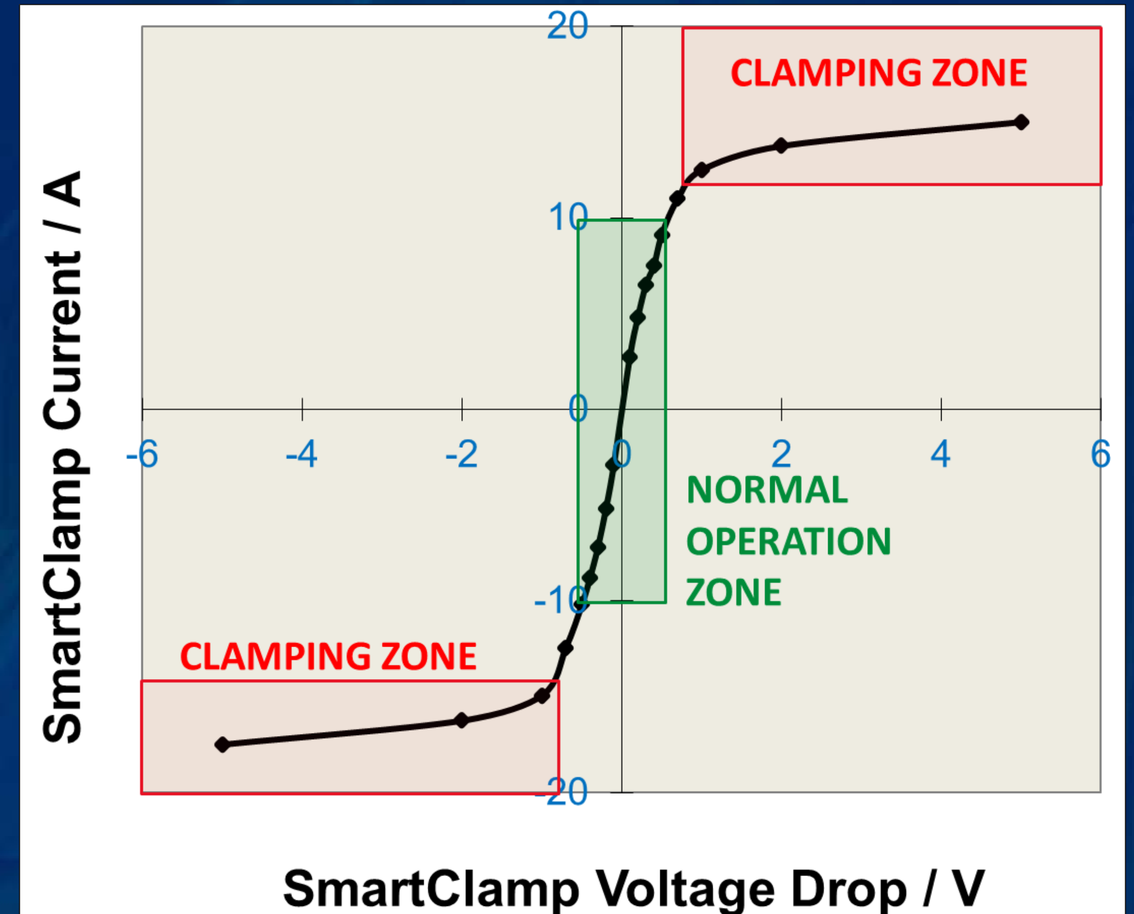

SmartClamp – implementation into test setup

# SmartClamp Technology – Insights...

- **Basic Functionality**
  - low-resistive within safe probe currents
  - limits max. probe current to prevent burn
  - insulated from supply power: easy to integrate into tester setups




SmartClamp – functional schematics




SmartClamp – electrical characteristics

# High Power...Going Multisite

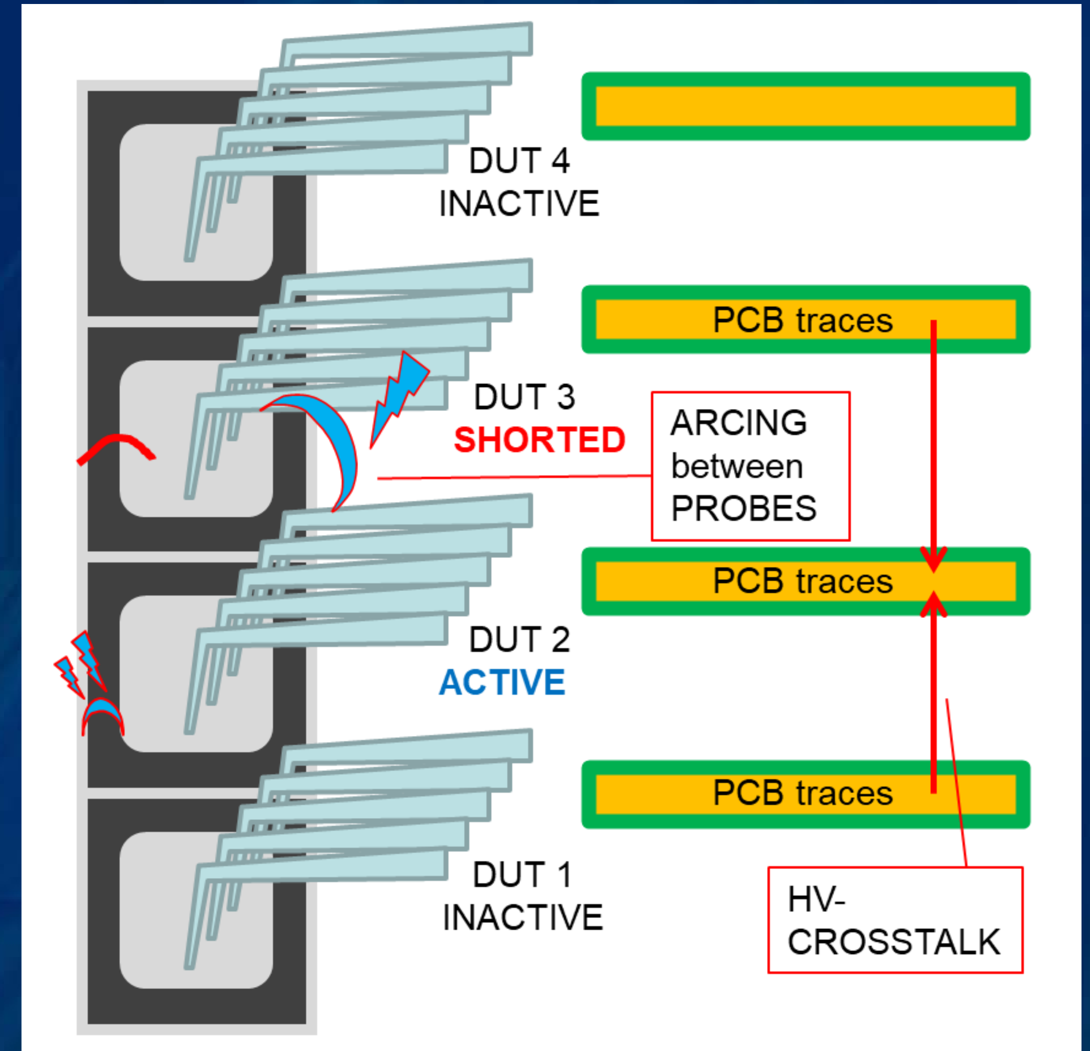
- **Example: <u>HV Power Diode</u> – 4x MULTI**

  **Considerations**

  – Additional arcing path between probes / sites !
  – HV crosstalk from adjacent sites
  – Safety aspects: traces present on probe card PCB might get connected to HV

**-> Can be avoided / minimized by**

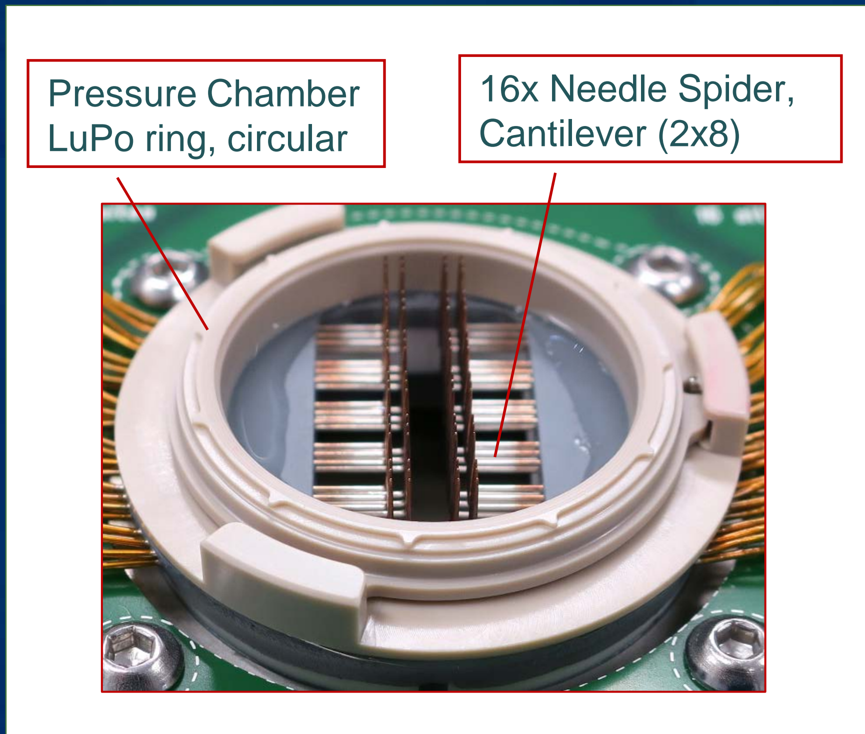
– proper probes layout using HV design rules
– appropriate PCB design techniques
– HV safety enclosure for prober / tester setup



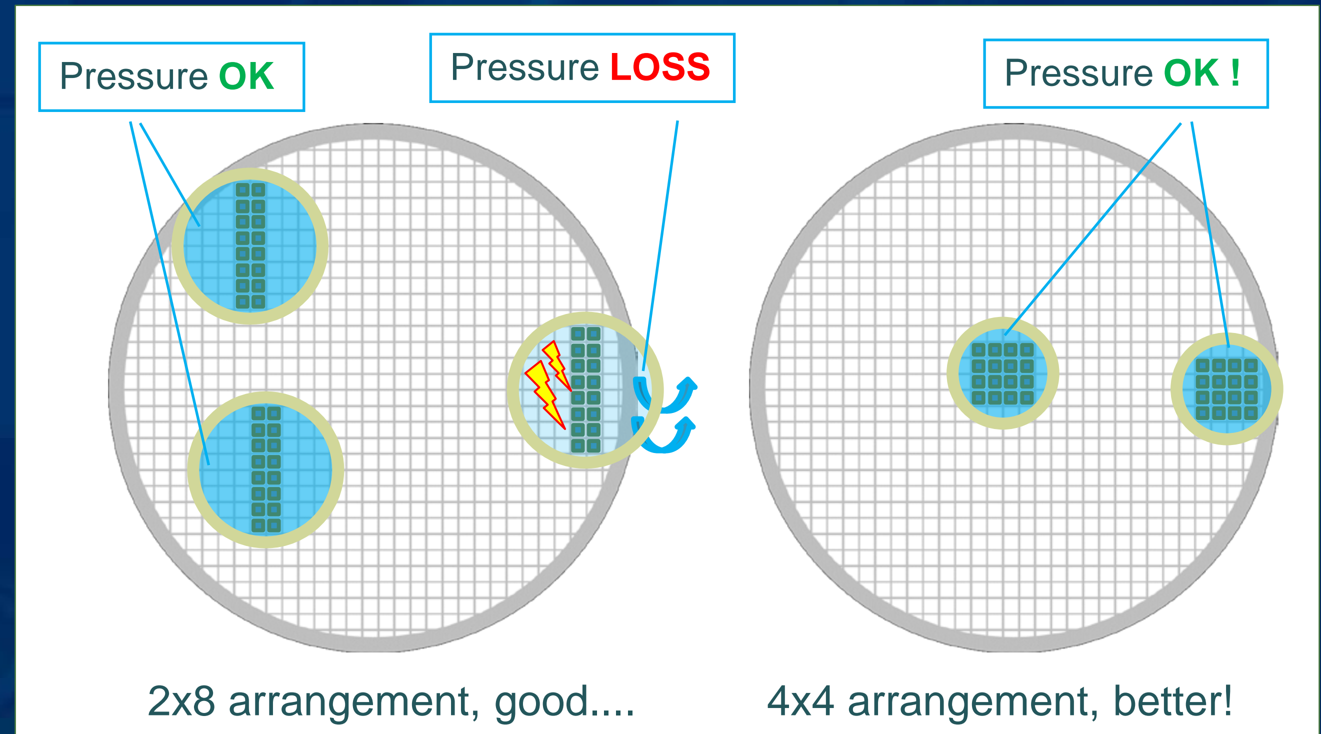

*) For details see conference proceedings SWTest 2023, San Diego

# Multisite Test Coverage ... Design Aspects

- Depending on multi-site DUT arrangement there might be a certain "overhang" of the pressure chamber w.r.t. DUT arrangement - compromising LuPo pressure build-up
- This might lead to non-testable chips near the wafer edge



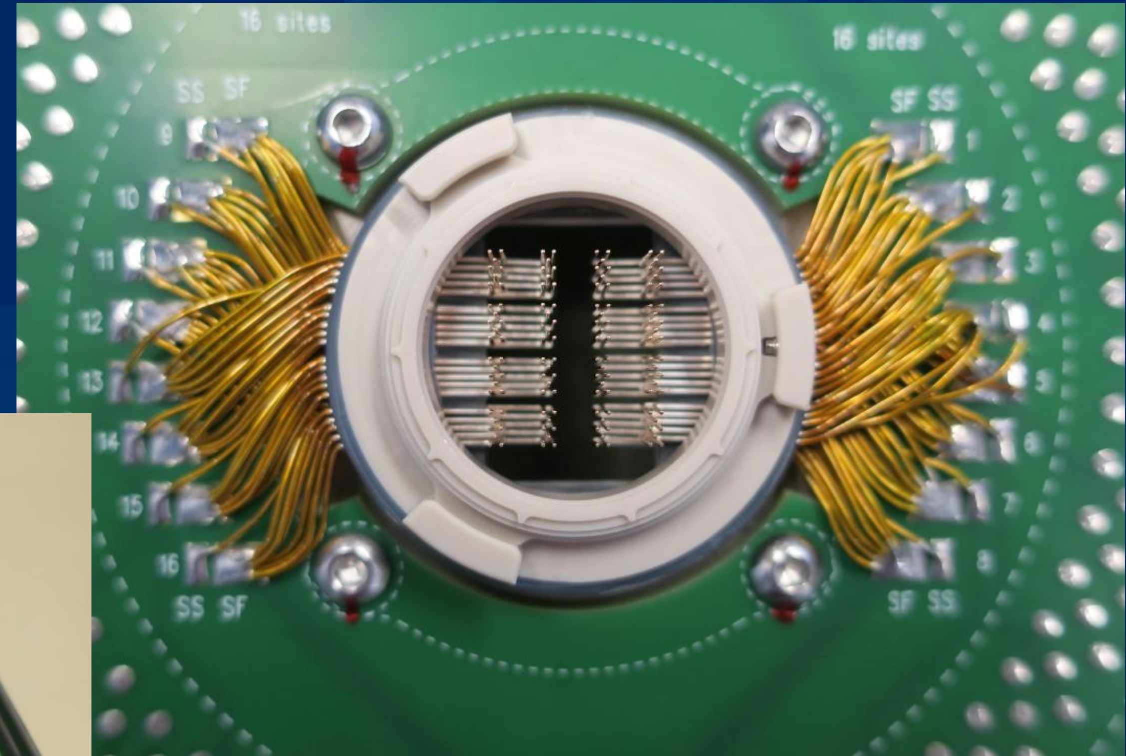

16x LuPo probe card, Cantilever probes

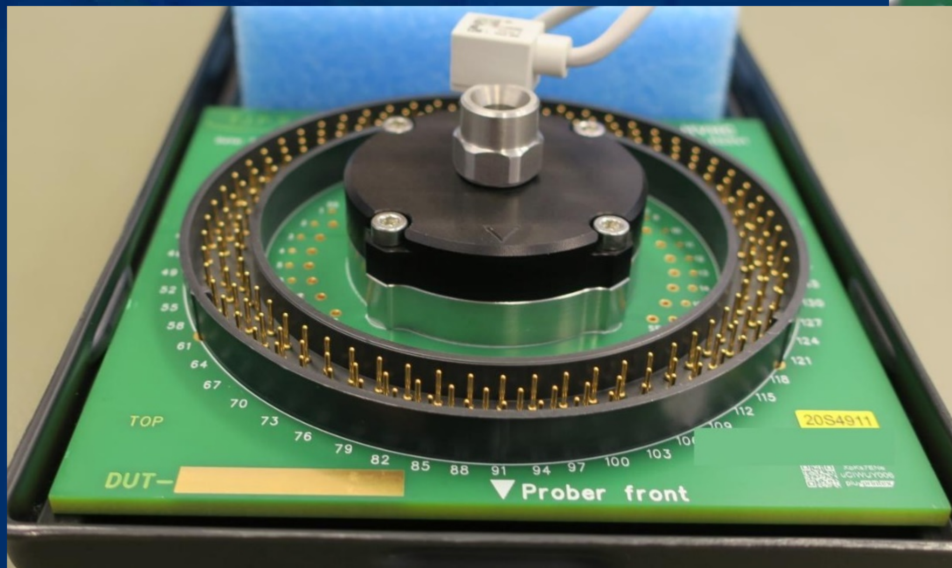



wafer edge contacting and LuPo pressure buildup

# Multisite Probe Cards – Cantilever 16x

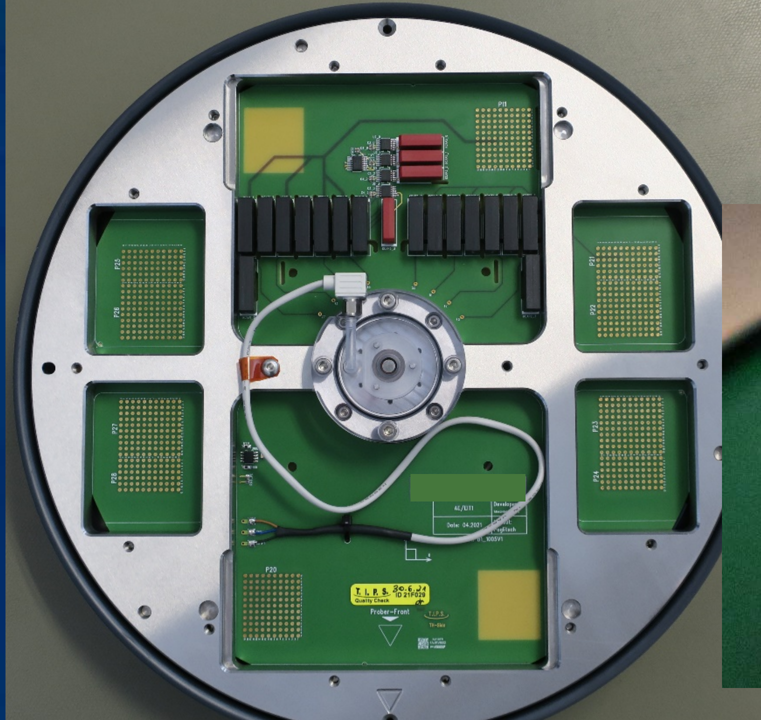
- **SiC diode, 1.6 kV, 45 A**
  - 4x4 arrangement
  - chamber pressure: 2.6 bar
  - auto compressed air docking
  - chamber pressure monitor



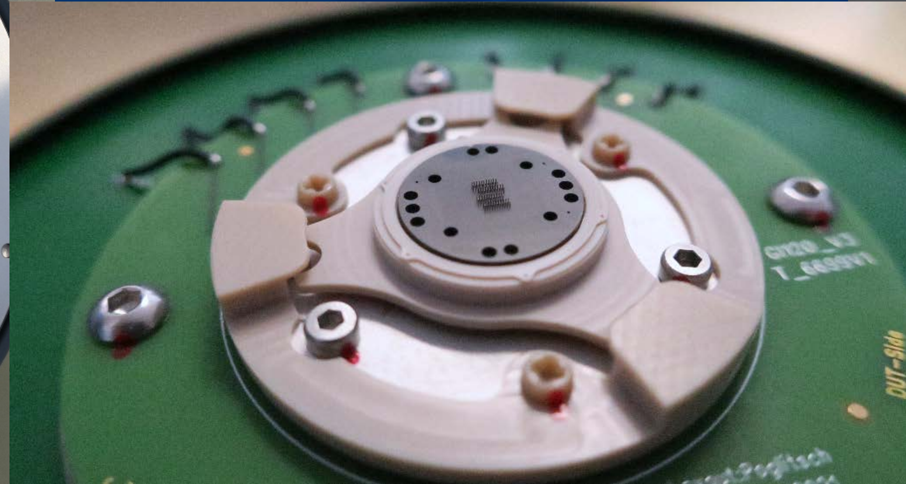



# Multisite Probe Cards – Vertical 4x

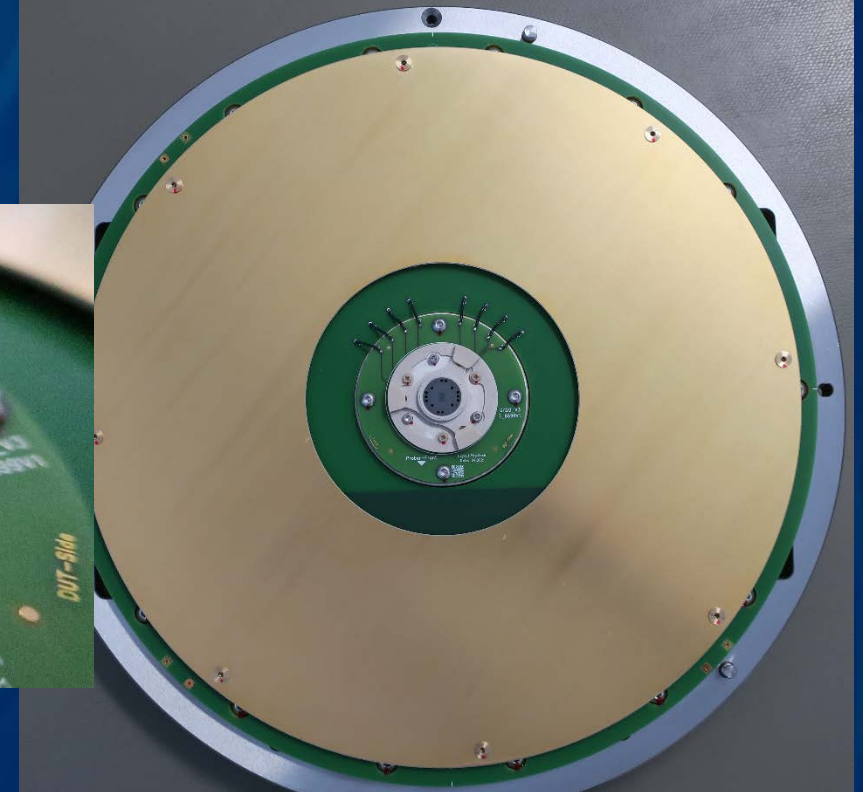
- HV capacitor array, 2.2 kV
- 1x4 arrangement
- chamber pressure: 5 bar
- chamber pressure monitor



4x Vertical LuPo probe card top side



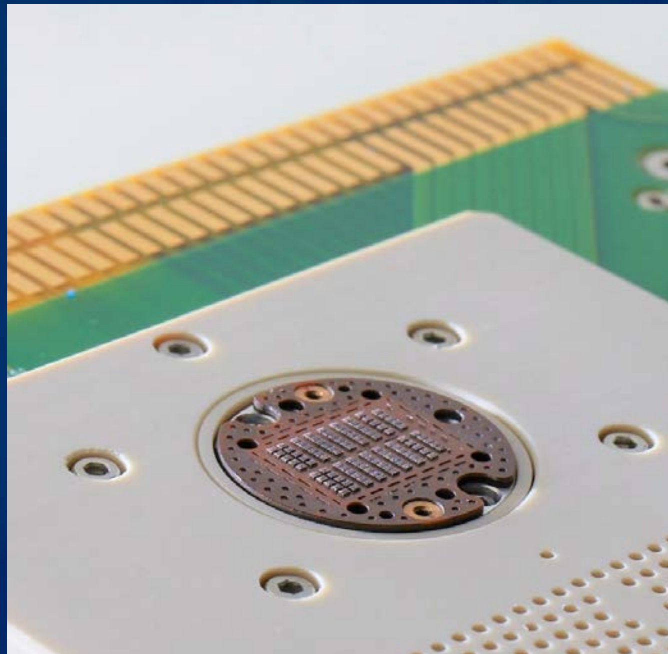

Vertical LuPo probe head buckling beam technology

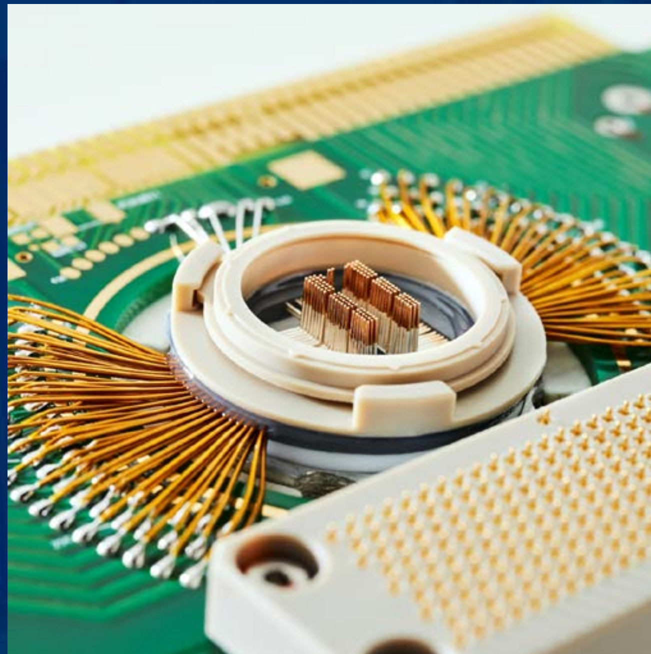


4x Vertical LuPo probe card top side

# Known Good >>POWER<< Die (KGD)

- **Application of wafer test contact technologies to bare chip testing**
  - highest test currents up to 3000A
  - ultra-fast switching: lowest parasitic inductance
  - AC test: both HV and HC present at the same time
  - test on chip handler (instead of wafer prober)





# Summary and Outlook

- various technologies (LuPo, SmartClamp...) developed for arc-free and burn-free power device chip testing
- enhanced for SiC, GaN requirements
- successfully introduced into R&D and high volume production test
- from single-site to multi-site probing for mass production
- highest power densities achieved in KGD test

- **An outlook...**
  - **Gen.4 LuPo** using CFM based design and 3D print technology
  - "**RzBeam Vertical**": new wire superalloy for High Current Vertical probes !!!

**...stay tuned!**

References:

SWTest conference proceedings :
2002: Probing 10 kV and 100A
2011: Aspects of High Power Probing
2017: Known Good >>POWER<< Die
2022: High Power goes Vertical
2023: High Voltage Probing goes Multi-Site
see www.swtest.org/archive
www.tips.co.at/downloads

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Questions please...