

## Application of Contact Resistance in Parametric Testing



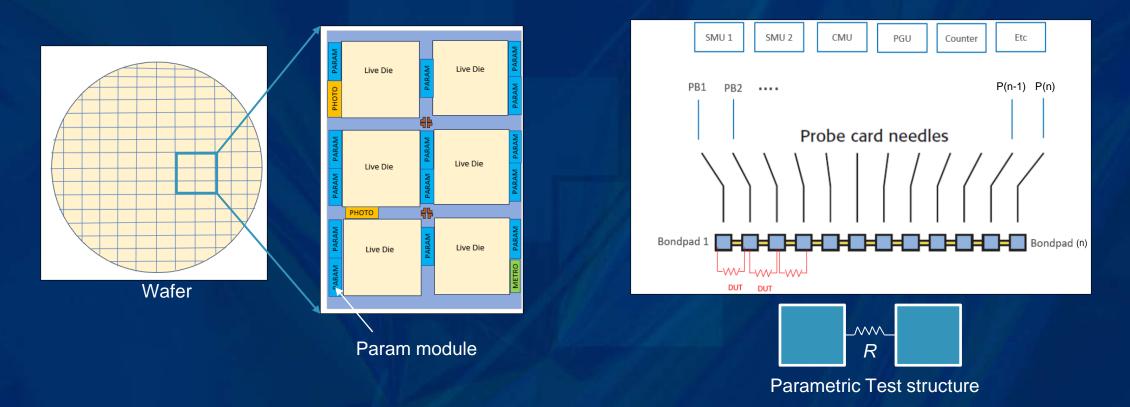
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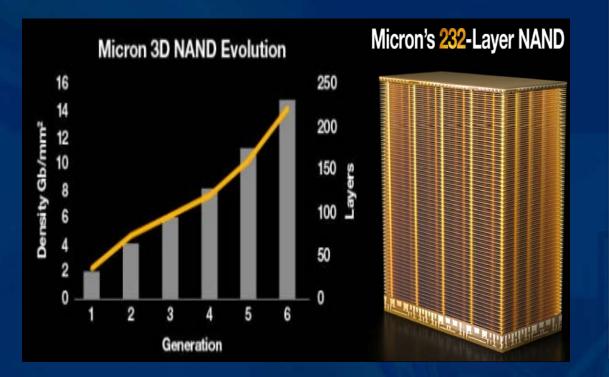
- Parametric Testing in NAND
- 3D NAND Evolution
- Testing 3D NAND Parametric with Multiplexer Module
- Challenges in Troubleshooting MUX Test Fails
- Contact Resistance (CRES) Test as option
- Limitation of CRES and hardware diagnostic
- Summary

# **Parametric Testing in NAND**

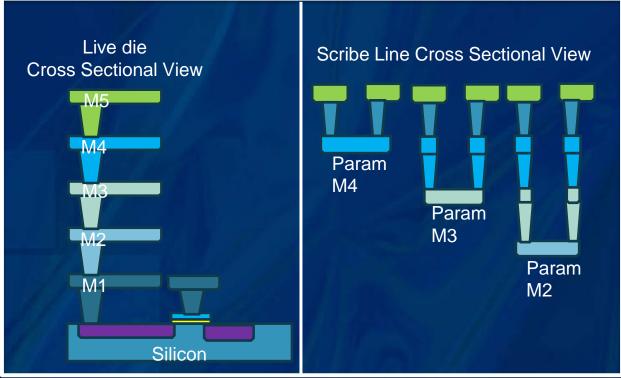
- Functional test is electrical test to check good or bad die.
- Parametric test is electrical test to check internal structures.



## **3D NAND Evolution**



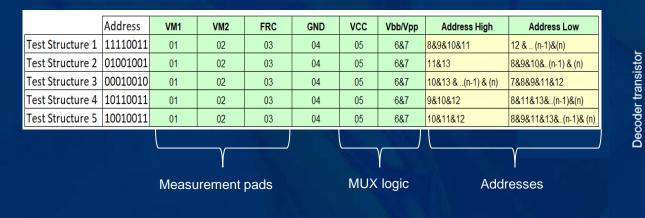
Micron's 3D NAND Evolution: 232-Layer NAND



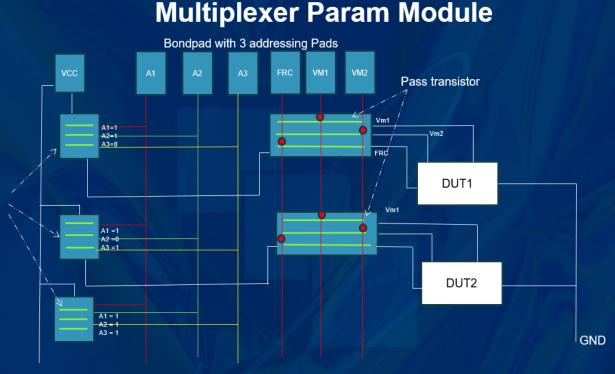
Hypothetical diagram, does not represent Micron design.

## **Testing 3D NAND Parametric with Multiplexer Module**

Param Multiplexer (MUX) module could pack 10X~20X components vs standard module.



Typical Param MUX Module Test Structure Connection Table



Multiple test structures (DUT) connected using transistors to perform signal switching.

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

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# **Problem Statement**

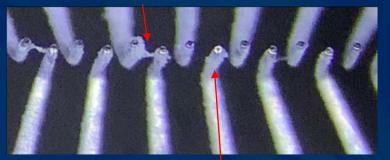
- Param Multiplexer module poses challenge in diagnosing hardware issues.
  - It is not straight forward to isolate faulty hardware.
  - Common issues are highlighted and a technique to isolate is illustrated in this presentation.
- Why couldn't the hardware self diagnose itself?

## **Common Hardware Issues**

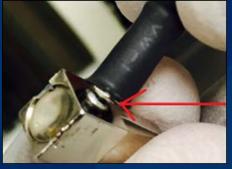
Probe marks misaligned/ out of bond pads



Dirty



Tip chip off



Loose connector



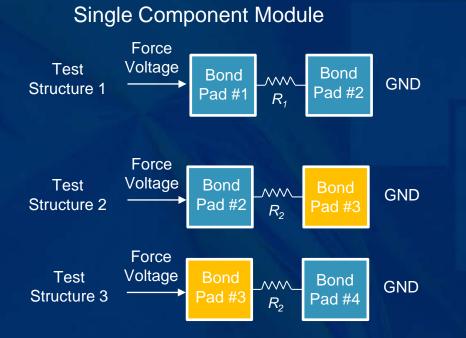


### Faulty Equipment / Probecard

- Mechanical Contact:
- Probe marks misalign/out of pad
- Bent/burnt/deformed tips
- Electrical Contact:
- Tester Board faulty
- Loose / damaged connector

Pictures do not necessarily represent Micron's production condition

## **Challenges in Troubleshooting MUX Test Fails**



- Commonality leads to Pin #3

# Multiplexer MUX ModuleTop ViewBondAnnoBondR<sub>1</sub>... R<sub>3</sub>BondPad #2R<sub>4</sub>... R<sub>6</sub>BondPad #2Pad #2

### Typical Param MUX Test Structure Connection

	Address	VM1	VM2	FRC		GND	VCC	Vbb/Vpp	Address High	Address Low	
Test Structure 1	11110011	01	02		03	04	05	6&7	8&9&10&11	12 & (n-1)&(n)	
Test Structure 2	01001001	01	02		03	04	05	6&7	11&13	8&9&10&(n-1) & (n)	
Test Structure 3	00010010	01	02		03	04	05	6&7	10&13 &(n-1) & (n)	7&8&9&11&12	

- Unable to trace which Pin failing.

## **Contact Resistance Test as option**

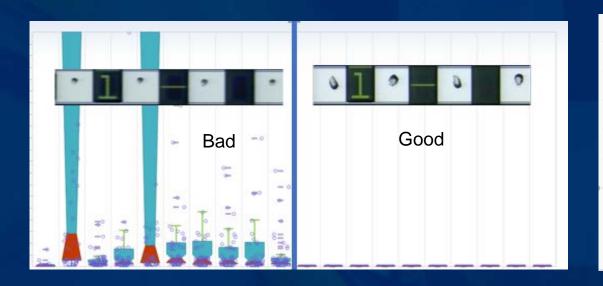
- One way is to use Contact Resistance (CRES).
- What is CRES?
  - Interface resistance between probecard lead tip and bondpad.

### • Why CRES?

- Most Issues are contact related.
- Direct signal path measurement.
- How can it help us?

# **Example of CRES Application**

Pin Board guide pin bent



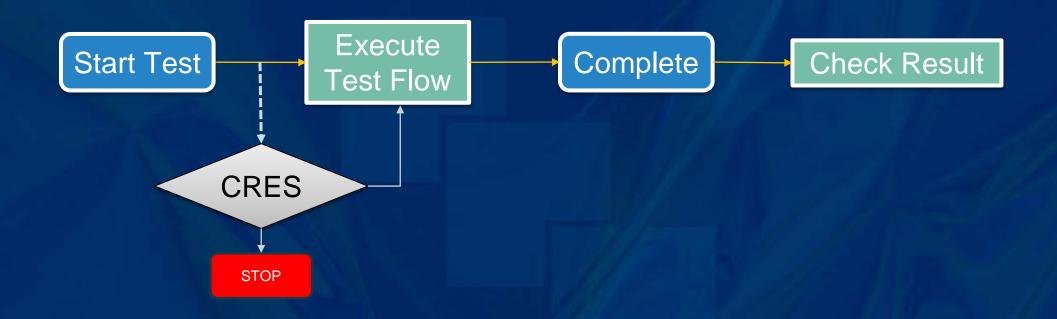
DETECTION

	-			est bod										er B lata			-			
PIN 1 – PIN 20	PIN 2 – PIN 3	PIN 4 – PIN 5	PIN 6- PIN 7	PIN81 – PIN 9	PIN 10 - PIN11	PIN 12 – PIN13	PIN 14 – PIN15	PIN 16 - PIN17	(u) ui – (l-1) – Din (n)	07 NIJ - 1 NIJ tid / PadPairs	PIN 2 – PIN 3	PIN 4 – PIN 5	PIN 6- PIN 7	PIN81 – PIN 9	PIN 10 – PIN11	PIN 12 – PIN13	PIN 14 – PIN15	PIN 16 – PIN17	Pin (n-1) – Pin (n)	

**ISOLATION** 

Examples of Hardware Failure with CRES

## **Shift Left CRES**



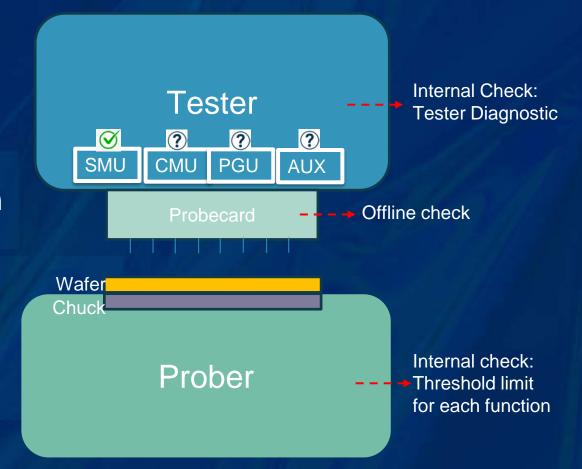
Shift Left / Preventive mindset at every run.

Saving capacity and avoiding bad data generation.

### **Limitation to CRES and Current Hardware Diagnostic**

- **1.** CRES is not covering all tester resources and requires wafer.
- 2. Tester and Prober performed its own individual self-check, not as one single entity.

Need new capability from Industry: <u>Test Cell Integrated Self-Check</u>



# Summary

- Multiplexing param test structures helped overcome scribe line real estate constraints.
- Inadvertently caused challenges in Parametric hardware troubleshooting.
- CRES is viable option but not the perfect solution.
- Future Test Cell need to be integrated, smart to self-diagnostic, always good when needed.

## **THANK YOU!**

 Credits & Acknowledgement: Micron Technology : Dave Peterson, Randy Cleverly, Gary Southern, Salil Mujumdar, Low Kar Loong, Thiam Seng Yip.