Cutting Cost and Resolution Enabled by Novel Photonic Technologies for Next–Generation Probe Cards Manufacturing

Dr. Ksenija Varga, Dr. Thomas Uhrmann
Business Development Management
EV Group

EVG

- EV Group: Company Overview, Novel Photonic Technologies.
- Maskless Exposure Technology: Motivation for Evaluation: Objectives & Goals.
- Methods, Materials, Procedures.
- Key Data & Discussion.
- Newest EVG's Technology: NanoCleave™.
- Summary & Conclusions.

EV Group | Company Overview

EVG

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FORSTINGER

EV Group | Novel Photonic Technologies

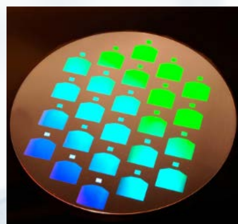
Leading supplier of wafer processing equipment for the MEMS, nanotechnology & semiconductors markets.

Founded in 1980 by DI Erich and Aya Maria Thallner. More than 1300 employees worldwide.

Headquarters in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China, Taiwan & Malaysia.

Advanced Resist Processing EVG®150 Series

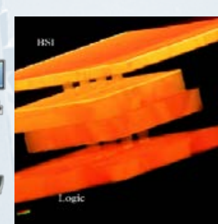
Maskless Exposure Technology LITHOSCALE®



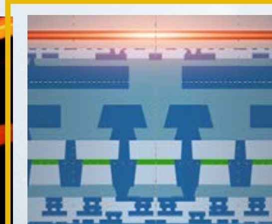
Nanoimprint & S&R Mastering HERCULES®

Wafer Level Optics & Photonics Packaging EVG®7300

METROLOGY



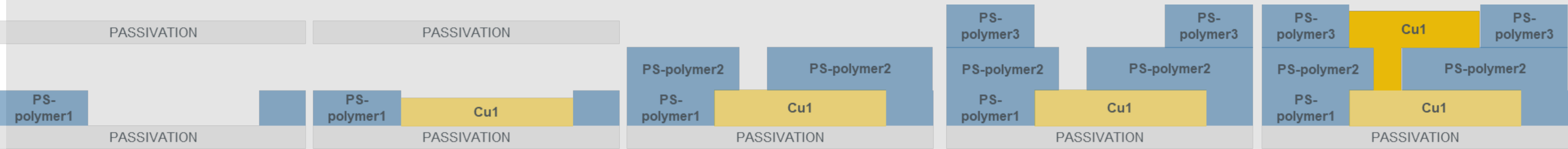
3D Integration & Hybrid Bonding



NanoCleave™ IR Laser Release

INTRODUCTION / BACKGROUND

- Fine pitch probe cards interconnect formation: several lithographic patterning steps.
- Process is connected to high CoO.



PATTERNING PROCESS

METAL1

- **VIA**

1. Coating
2. Expose VIA
3. Development
4. UV-cure
5. Post UV cure bake

- **METAL2**

1. Coating
2. Expose METAL2
3. Development
4. UV–cure
5. Post UV cure bake
6. Oven cure as normal
7. Descum

Development of cost–efficient processes.

Cutting costs by reduction of the lithographic steps.

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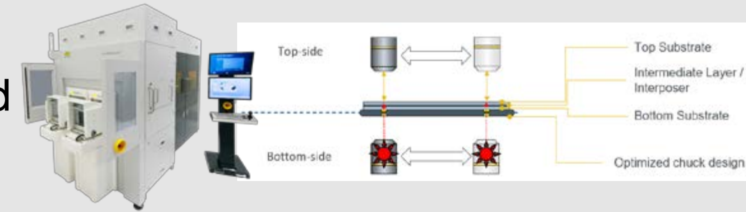
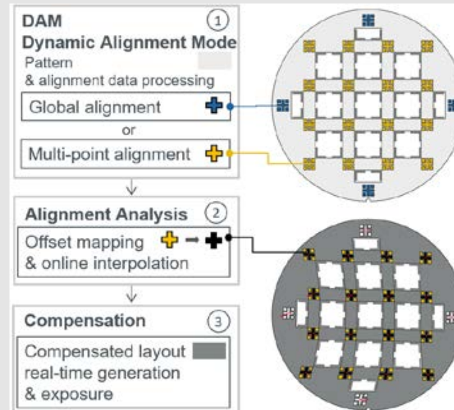
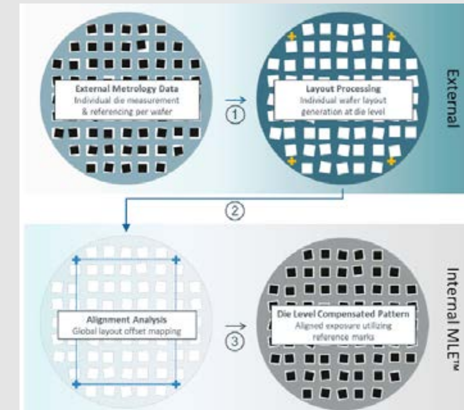
EQUIPEMENT

- VIS top–side alignment & backside alignment.
- Advanced Distortion Function: crucial for advanced packaging.
- High autofocus ±50 µm, high dept of focus ±12 µm.
- Die annotation feature.



PARAMETER	SPECIFICATION
Exposure Source	HP UV – Laser Diode (LD)
Exposure Spectrum [nm]	375, 405 and every mix
CD L/S [µm]	< 2
Substrate Sizes [inch]	6“ – 12“
Wafer Layout [format]	GDS II (standard) Gerber, OASIS, ODB++ (optional)



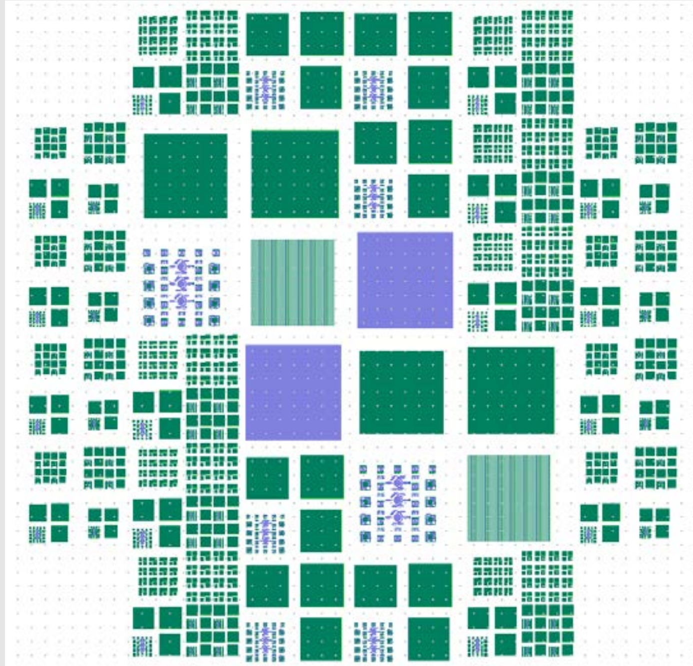


Die-level compensation schematic process flow

MLE^{TM} | Methods, Materials, Procedures

TEST LAYOUT

- Containing various test fields scaled up/down to different sizes written on 1 wafer.

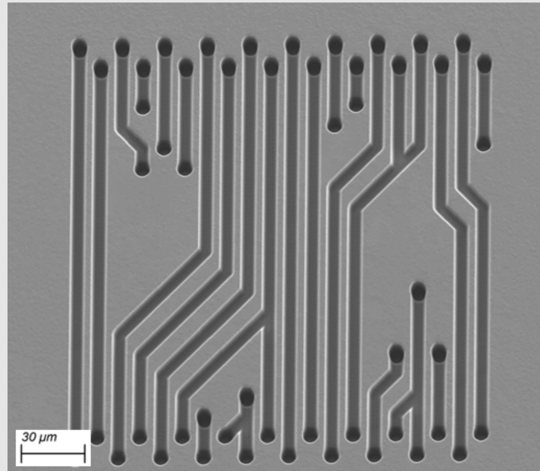


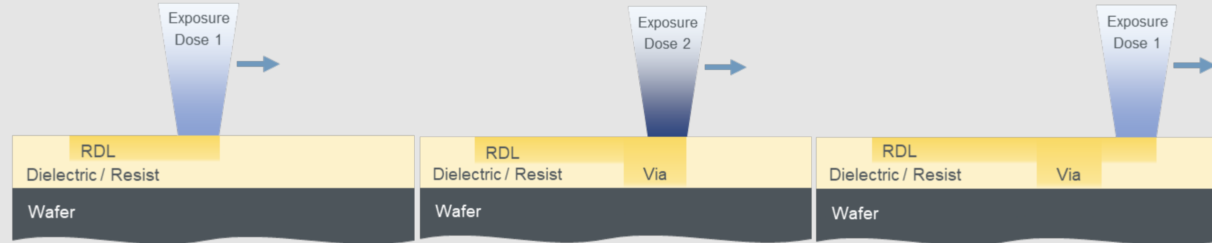
EFFICIENT PROCESS EVALUATION & OPTIMIZATION!

MLE™ | Methods, Materials, Procedures

EXPERIMENTAL SETUP

- Evaluated dose range: 10–450 mJ/cm^2.
- TOK resist, positive tone.





Design layout with dense RDL and VIAs connections

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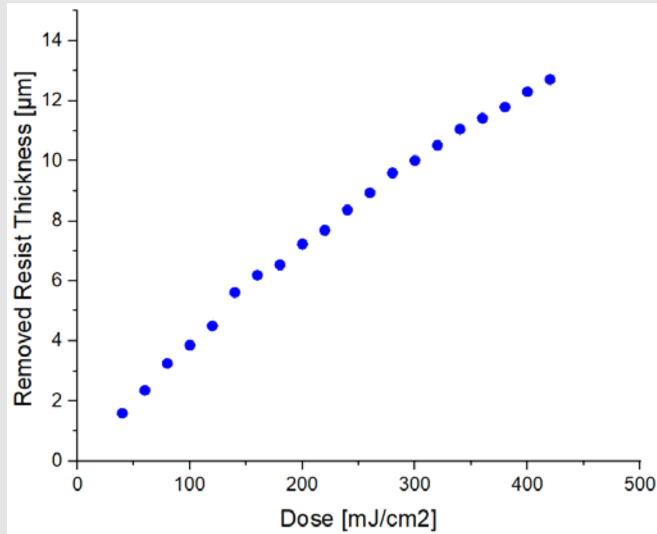
CONTRST CURVE

- To optimize the multi–level exposure an understanding of dose dependency on the penetration depth is required.
- Matrix where dose/wavelength/focus can be adjusted via recipe.



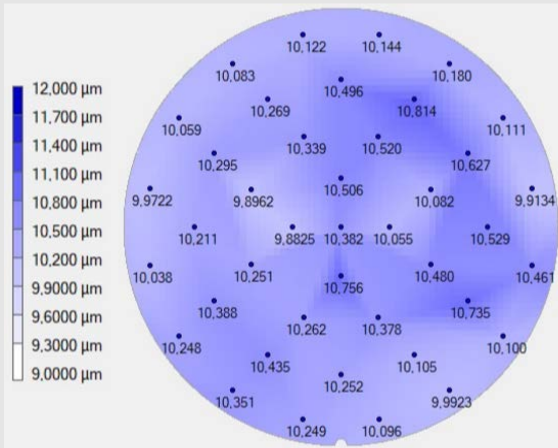
Minimum exposure dose required to initiate reaction.

Linear behavior at higher exposure dose

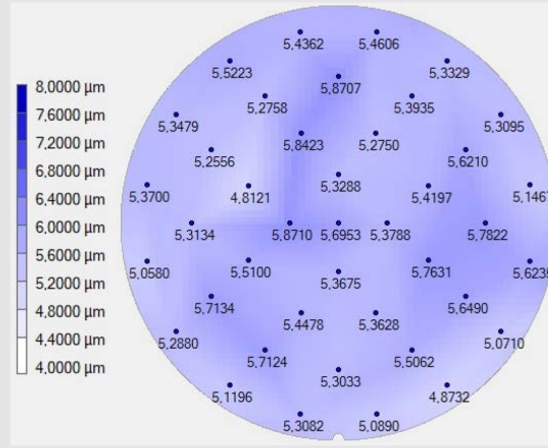
MLE™ | Key Data & Discussion

SPECTRAL REFLECTANCE IMAGES

- Estimation of the FT nonuniformity.



Nonuniformity measurement after spin–coating process.



Nonuniformity measurement after exposure with a defined penetration depth & resist development.

Resist surfaces generated via multi–level exposure is not significantly deviating from the original spin–coated surface.

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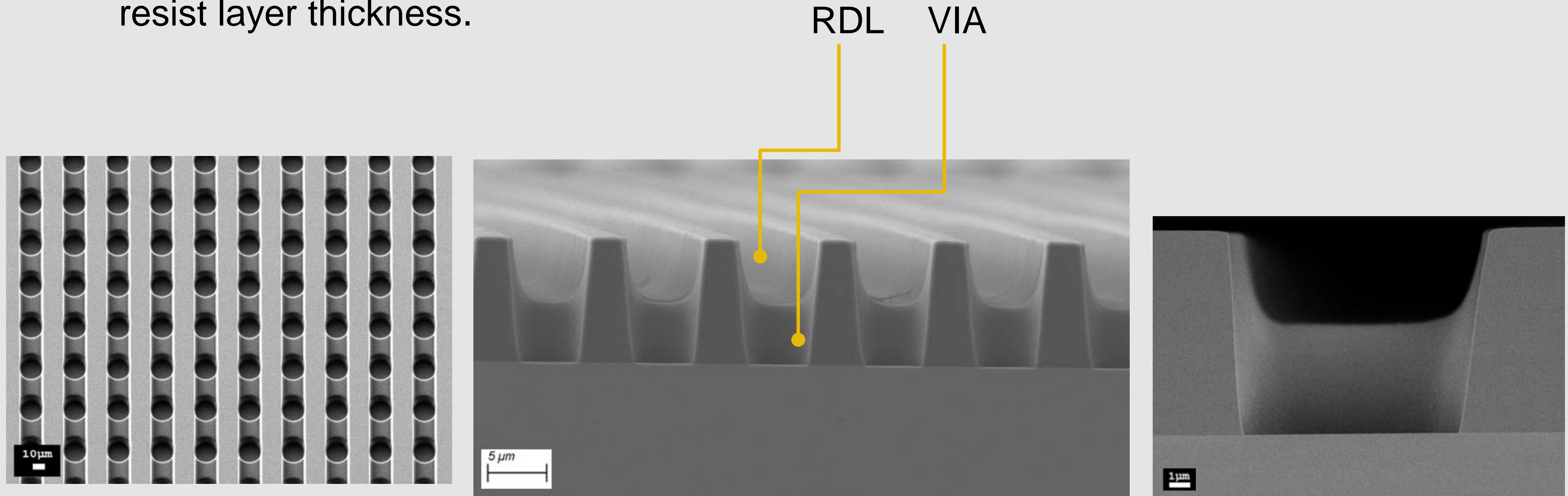
SEM IMAGES of DUAL–LAYERS

- High dept–of–focus allows good control of sidewall profile and resolution throughout the resist layer thickness.

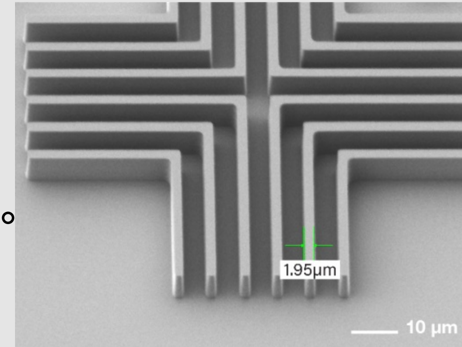


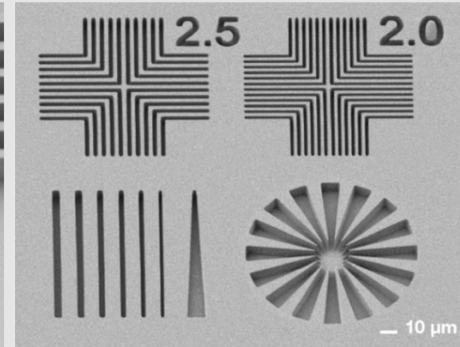
RDL traces with vias (width: 5 µm, gap: 3 µm)

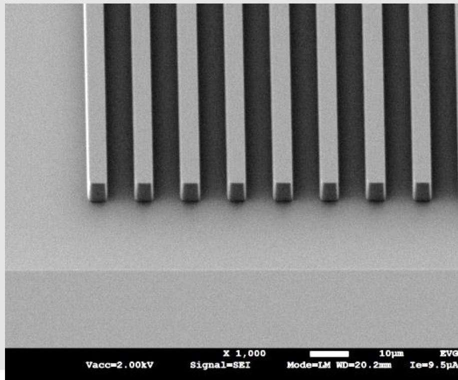
MLE™ | Key Data & Discussion

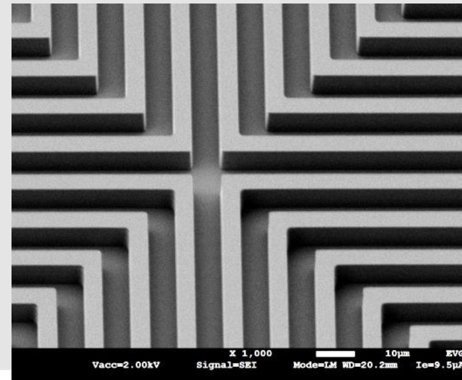
SEM IMAGES

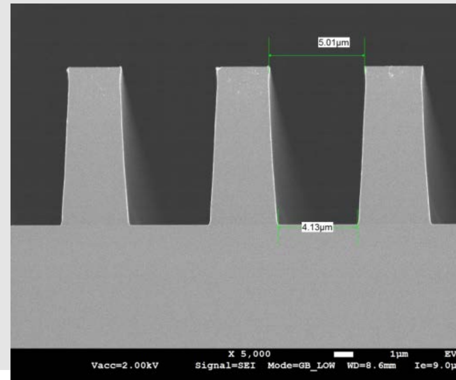
- Baseline evaluation of line–space variation patterning performance.
- Pos. TOK P–W1000T
- Layer thickness: 8 µm
- Aspect ratio 4:1, sidewall angle up to 87°

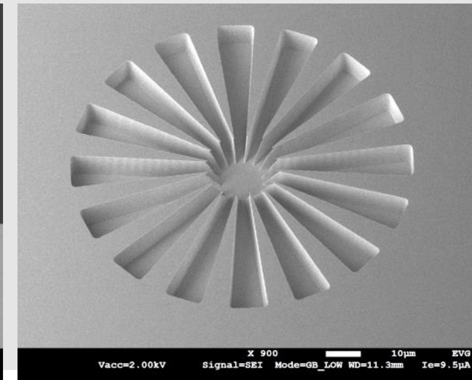








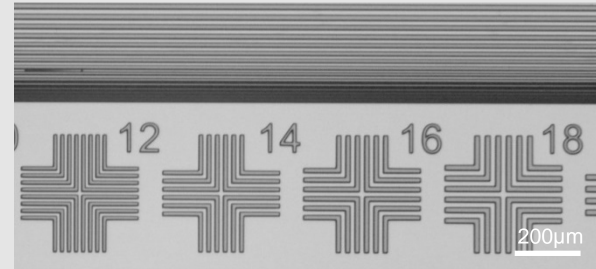


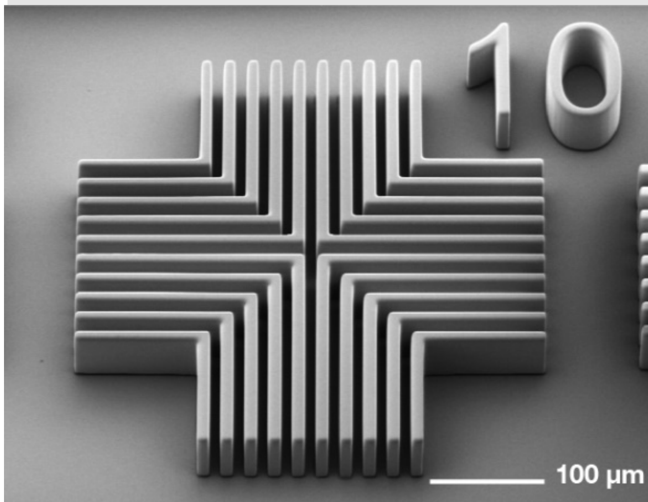


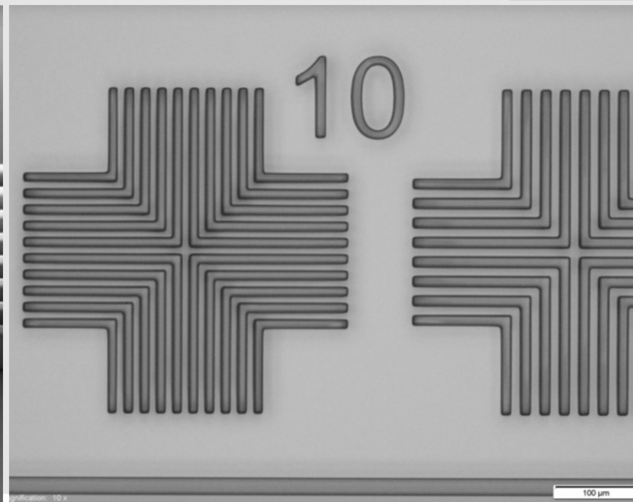
MLE™ | Key Data & Discussion

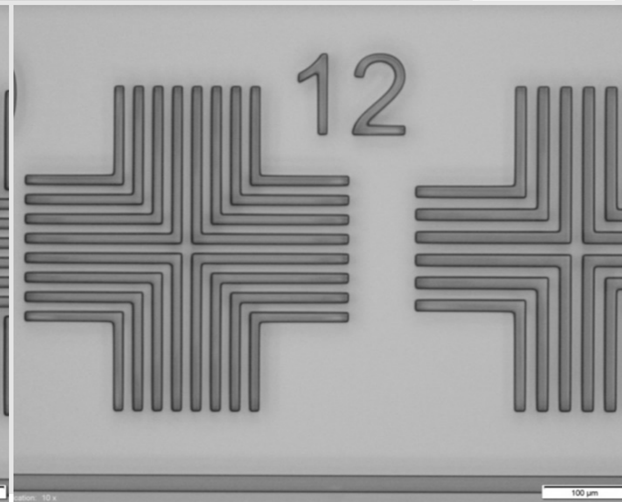
SEM IMAGES

- Thick resist applications.
- JSR THB 151N, negative tone.
- Layer thickness: 50 µm, AR 5:1





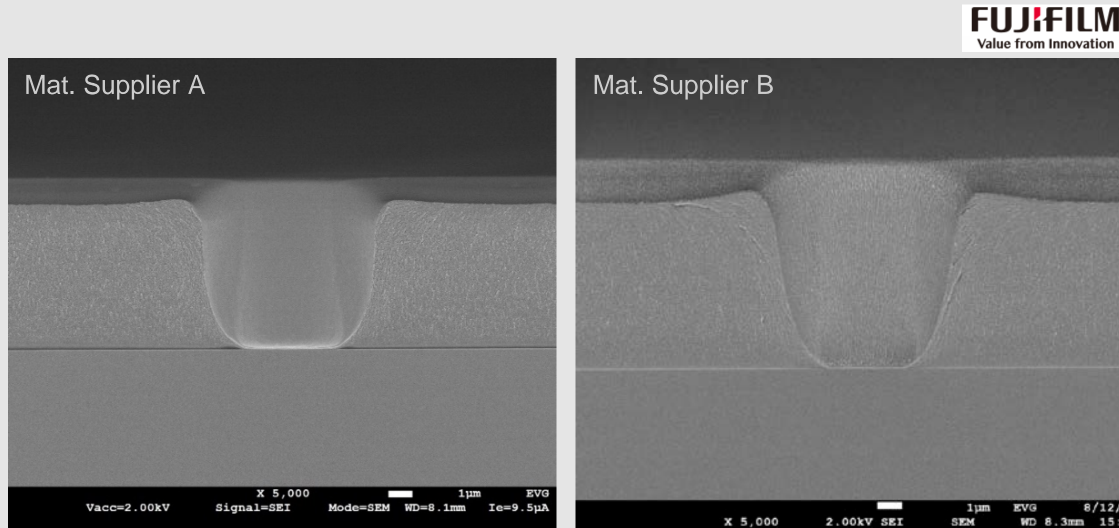




MLE™ | Key Data & Discussion

SEM IMAGES

- NEW DEVELOPMENT: negative tone dielectrics for fine pitch probe cards RDL patterning.
- Layer Thickness: 7 – 8 µm (after soft bake), AR: > 2:1



3.5 µm via resolved in ~7 µm LT   3 µm via resolved in ~8.5 µm LT

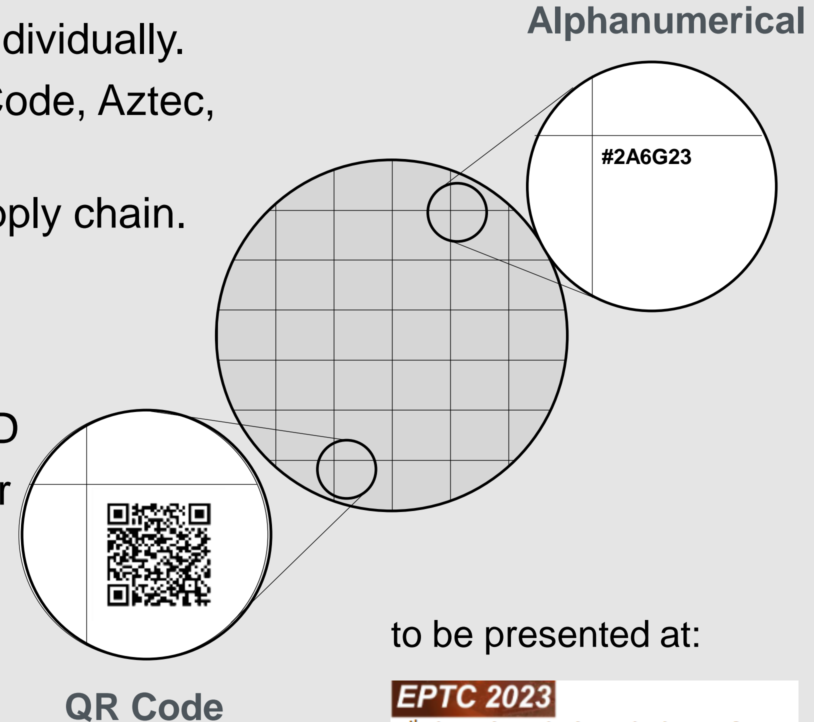
MLE™ | Follow–Up Work

DIE ANNOTATION FEATURE

- Data generation "on–the–fly" for each wafer individually.
- Available Annotation Types: DataMatrix, QR Code, Aztec, PDF417 etc.
- Important for traceability in semiconductor supply chain.

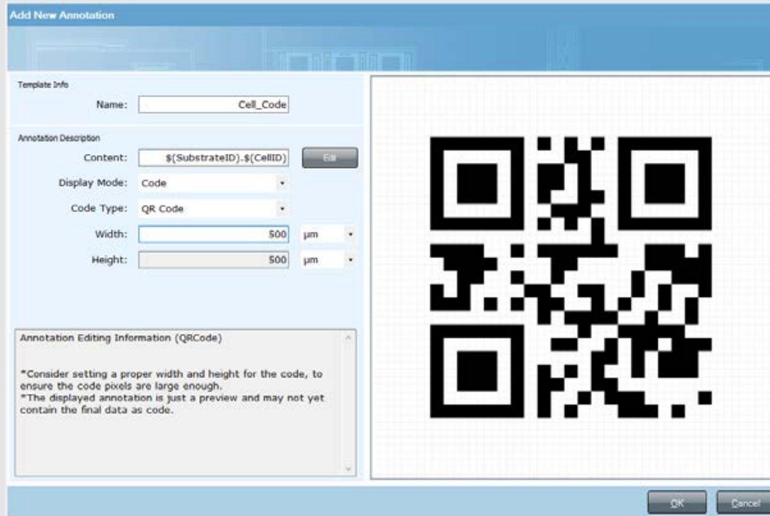
VARIABLES USED

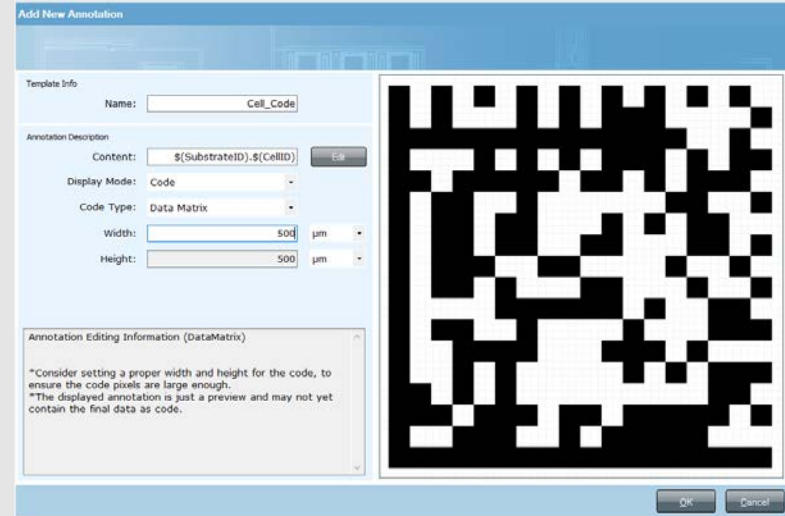
- LotID, SubstrateID, SubstrateAquiredID, CellID
- EquipmentName, ModuleName, SerialNumber
- RecipeName, RecipeNamespace
- ProcessJobID, ControllJobID



MLE™ | Follow–Up Work

Annotations are created as templates on LITHOSCALE® and can be used in various recipes.





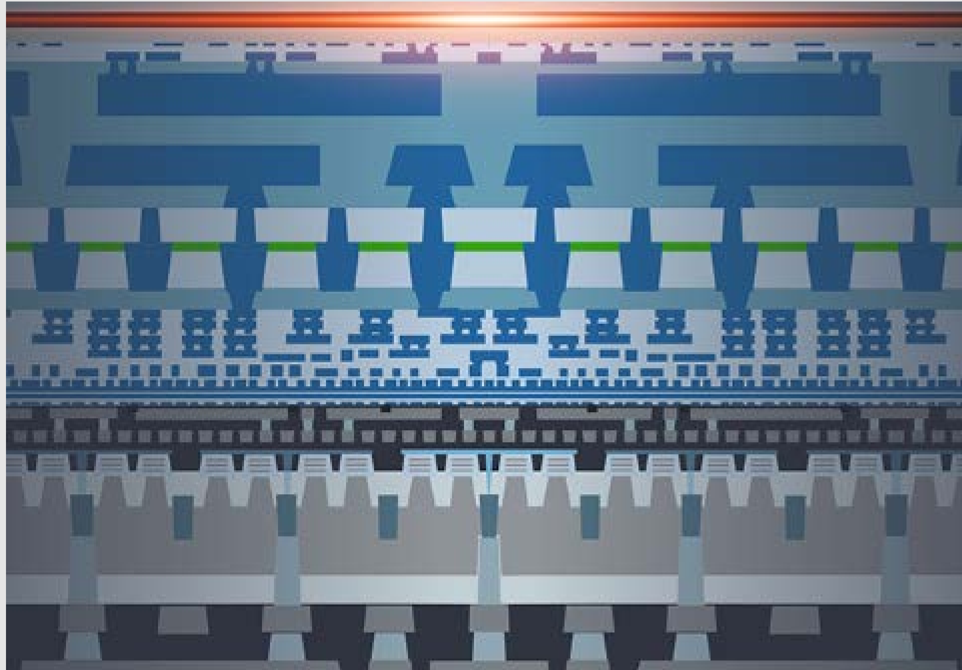
QR CODE

DATA MATRIX

NanoCleave™ | IR Laser Release

IR laser–initiated release of any ultra–thin film or layer from silicon carriers with nanometer precision.

Revolutionizing 3D & heterogenous integration as well as material transfer.



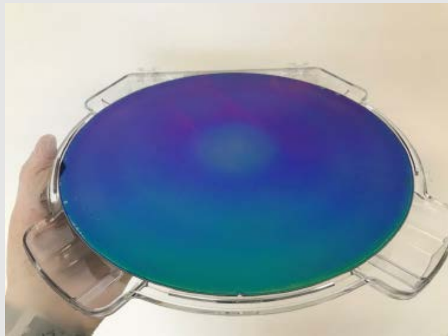
Front–end compatible carrier technology for further integration of fusion and hybrid bonding processes.

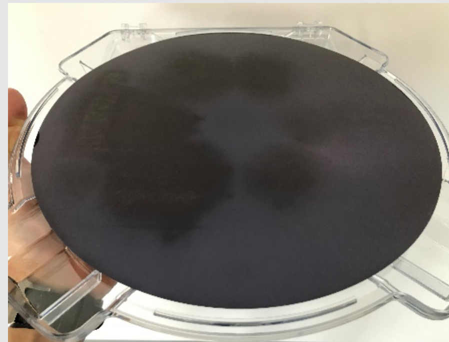
Enabling silicon carrier wafers in advance packaging processes such as FoWLP & 3D SIC.

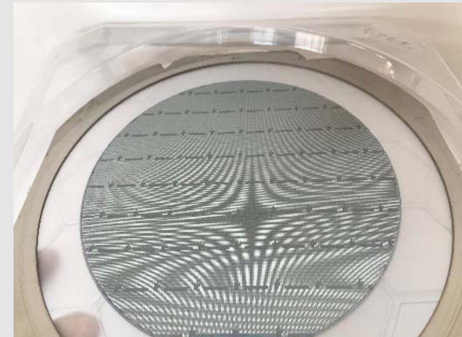
NanoCleave^{TM} | IR Laser Release

INTRODUCTION

- Technology utilizes IR laser & inorganic release materials to enable laser debonding on Si.
- This eliminates the need for glass substrates in advanced packaging.
- Temperature & glass carrier compatibility issues are avoided.
- Ability to transfer ultra–thin layers via carriers in front–end processing is enabled.


300 mm fusion bonded wafers release


300 mm molded wafer release


200 mm temporary bonded thin device wafer release

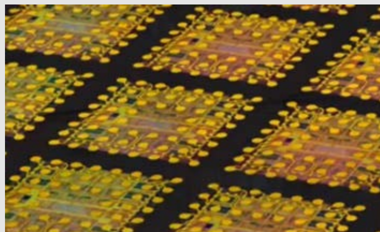
NanoCleave™ | IR Laser Release

INTRODUCTION

- The nanometer–precision of new process supports advanced semiconductor device roadmaps calling for thinner device layers & packages.

APPLICATION in FO WLP

- Release for “RDL first”.
- Temporary bonding for warpage control for “chip first” enables thinning & backside processing.



Source: Brewer Science

EVG's Photonic Technologies | Summary & Conclusions

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MASKLESS MANUFACTURING ACCOMPLISHES:

TECHNOLOGY SCALING for FINE PITCH PROBE CARDS

- High resolution patterning achieving <2 µm L/S

DESIGN FLEXIBILITY

- Layout independent from chip size
- Multi–die architectures, die–level patterning

MARKET LEADERSHIP

- Fast tape–out
- Adaptation to customer needs

EVG's Photonic Technologies | Summary & Conclusions

EVG

MASKLESS MANUFACTURING ACCOMPLISHES:

ECONOMICAL BENEFITS

- By dual–layer exposure of resists by cutting the lithographic steps.

SUSTAINABLE INDUSTRY

- Short supply chain contributes to low ecological footprint

Recently launched IR Laser Release Technology

- Enables cutting the costs through thin layer transfer & elimination of needed glass substrates.

Thank you for your attention!

K.Varga@EVGroup.com

Wafer is coated with black resist and world map is patterned on LITHOSCALE®

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