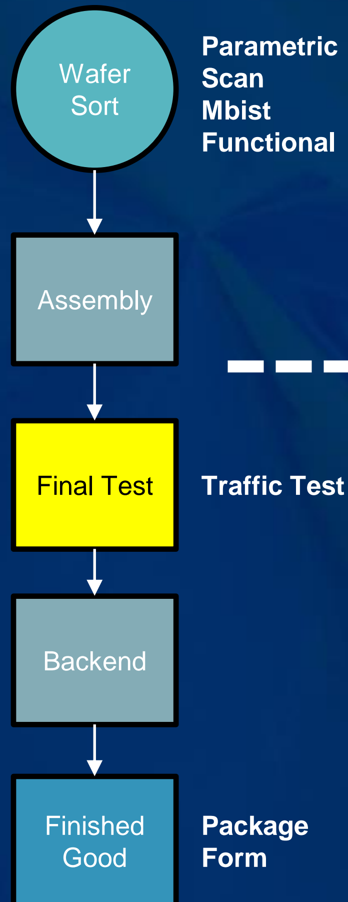
KGD 56G PAM4 HIGH SPEED TESTING FOR DATA CENTER PRODUCT – SETUP STABILITY IMPROVEMENT AT WAFER SORT

Wilson Yap
Principal Product Engineer
Marvell Technology Inc.

Agenda

- Overview in Wafer Sort High Speed Testing
- KGD Testing Hardware Overview
- Manufacturing Issues and Challenges
- Resolutions and Results

Overview in WS High Speed KGD Testing



- KGD (Known Good Die) - a form factor that eliminates assembly cost; at the same time optimizes Chip on Board (COB) module assembly process
- The twinning solution (HSIO card cage + Multilane Module) was introduced to enable high speed testing in wafer sort
- Applicable to products that require high speed testing at wafer sort with limited external loopback testing capability

KGD Test Hardware Overview

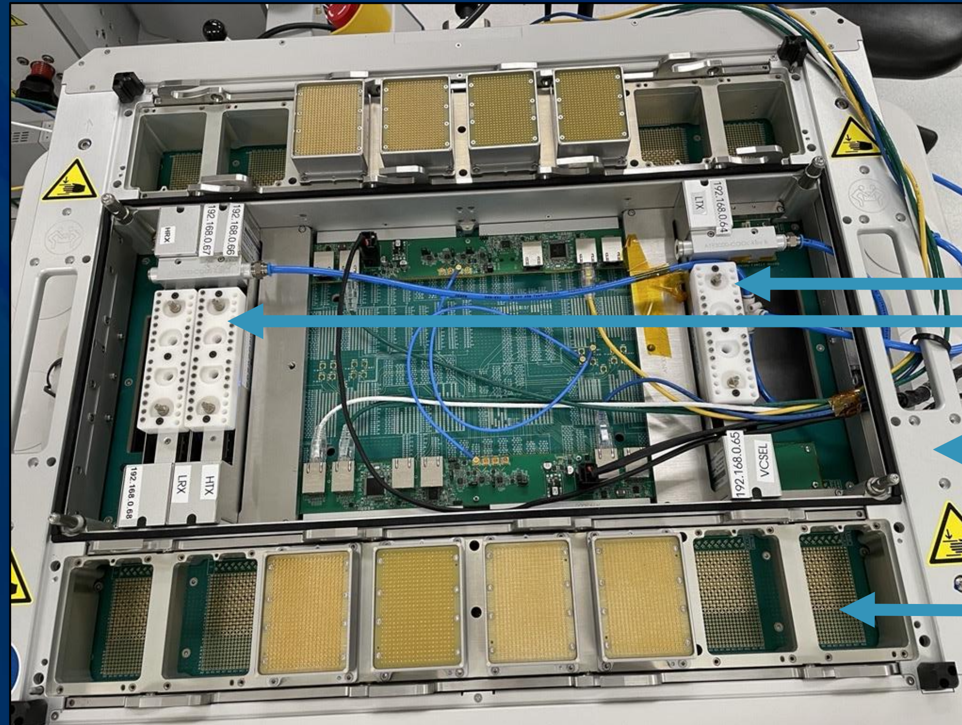
ATE
HP93K
PS1600

Prober

Twinning Frame

Multilane Modules

Probe Card

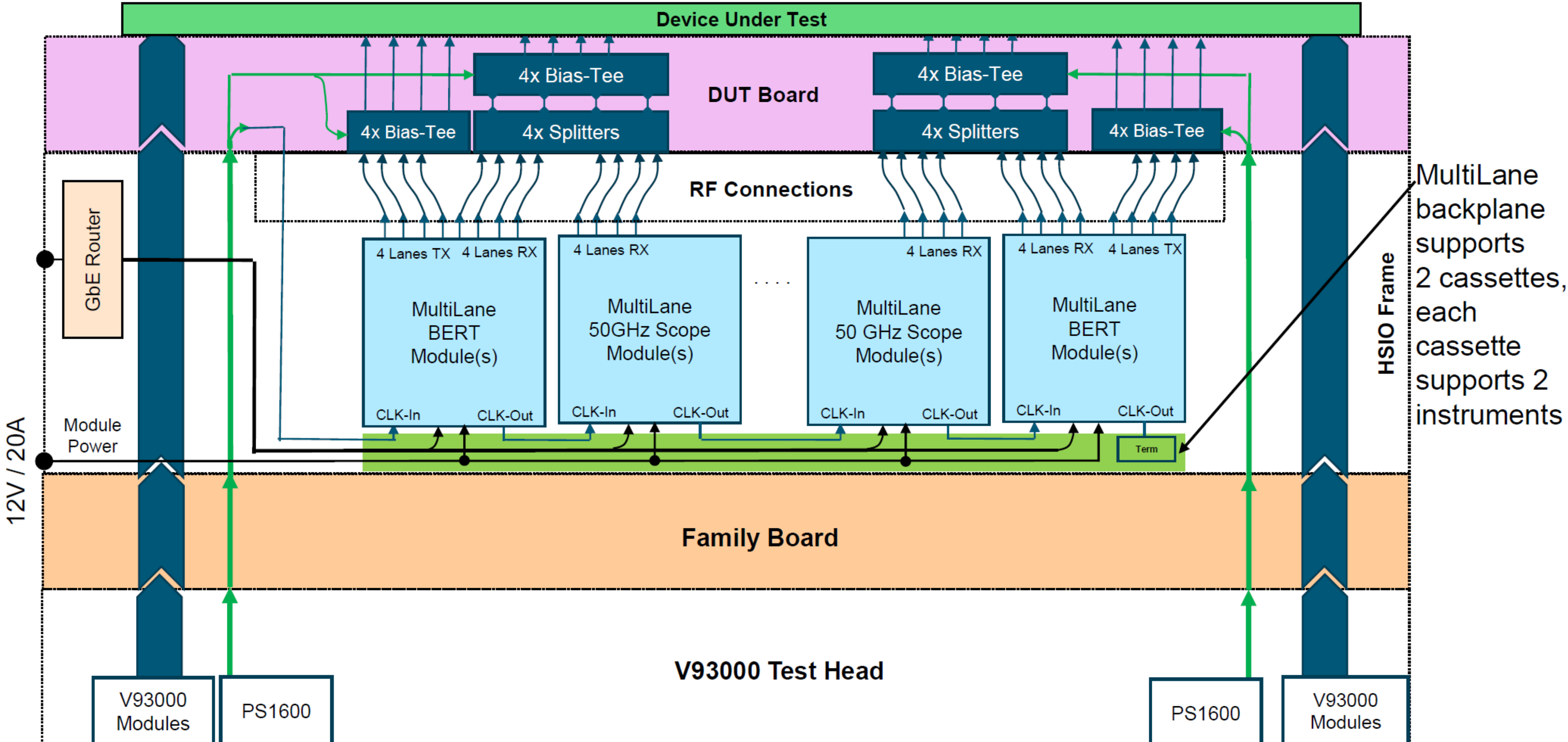


Multilane Modules:
DSO (Digital Sampling Oscilloscope)
Bert (Bit Error Rate Tester)

Twinning Frame

Family Board

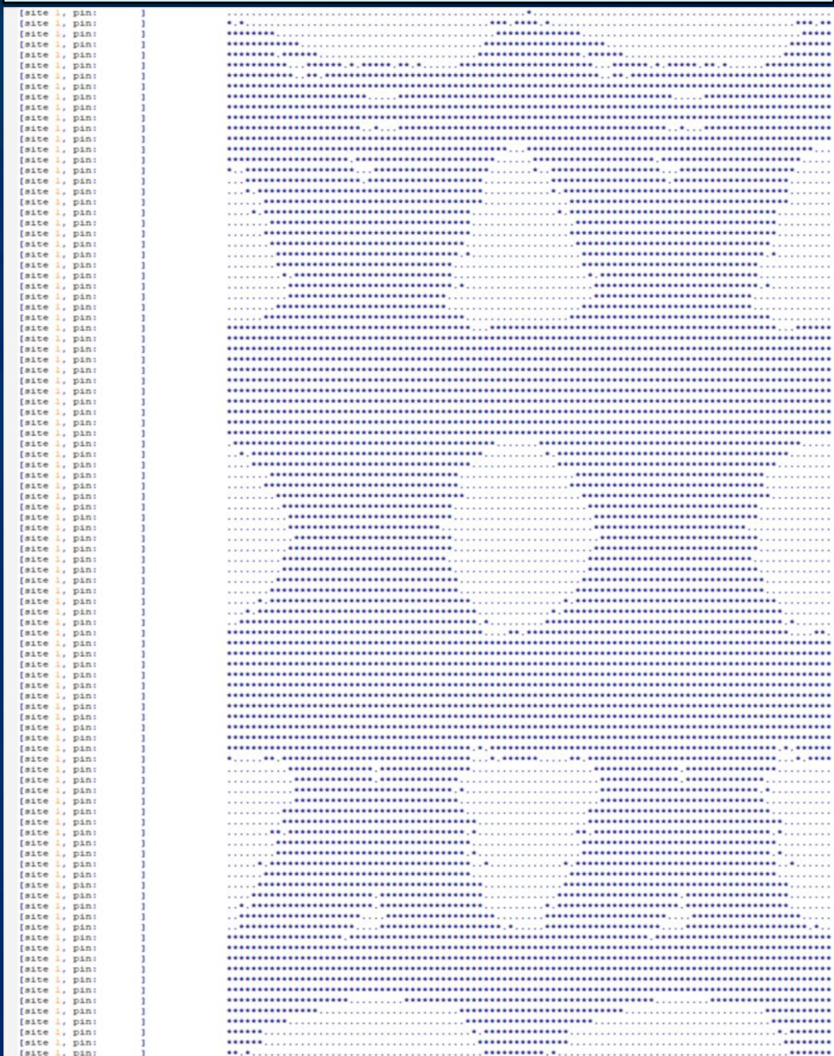
KGD High Speed Testing Configuration



Source: Advantest

ATE Output Sample

Example of Eye Diagram on ATE UI Report



Example of Output Format on ATE UI Window

```
[site 2, pin: '   '] Level2 (10)                       [mV]     :
[site 2, pin: '   '] Level3 (11)                       [mV]     :
[site 2, pin: '   '] Level1 (01)                       [mV]     :
[site 2, pin: '   '] Level0 (00)                       [mV]     :
[site 2, pin: '   '] Max                               [mV]     :
[site 2, pin: '   '] Min                               [mV]     :
[site 2, pin: '   '] Peak To Peak                      [mV]     :
[site 2, pin: '   '] Lower Eye Amplitude (AVlow)       [mV]     :
[site 2, pin: '   '] Middle Eye Amplitude (AVmid)      [mV]     :
[site 2, pin: '   '] Upper Eye Amplitude (AVupp)       [mV]     :
[site 2, pin: '   '] VEC                               [mV]     :
[site 2, pin: '   '] Lower Eye Height (Vlow)           [mV]     :
[site 2, pin: '   '] Lower Eye Top (VlowTop)           [mV]     :
[site 2, pin: '   '] Lower Eye Base (VlowBase)         [mV]     :
[site 2, pin: '   '] Middle Eye height (Vmid)          [mV]     :
[site 2, pin: '   '] Middle Eye Top (VmidTop)          [mV]     :
[site 2, pin: '   '] Middle Eye Base (VmidBase)        [mV]     :
[site 2, pin: '   '] Upper Eye Height (Vupp)           [mV]     :
[site 2, pin: '   '] Upper Eye Top (VuppTop)           [mV]     :
[site 2, pin: '   '] Upper Eye Base (VuppBase)         [mV]     :
[site 2, pin: '   '] Lower Eye Width (Hlow)            [ps]     :
[site 2, pin: '   '] Middle Eye Width (Hmid)           [ps]     :
[site 2, pin: '   '] Upper Eye Width (Hupp)            [ps]     :
[site 2, pin: '   '] Lower Eye skew (LowEyeSkew)       [ps]     :
[site 2, pin: '   '] Middle Eye skew (MidEyeSkew)      [ps]     :
[site 2, pin: '   '] Upper Eye skew (UpperEyeSkew)     [ps]     :
[site 2, pin: '   '] Vrms                              [mV]     :
```

- The communications between ATE and Multilane Modules were established via the LAN
- Customized library was used
- Measurement results were logged, and the eye diagram can be displayed over the UI window

Manufacturing Challenges – High Speed Sort

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Setup Stability

Manufacturing Challenges – High Speed Sort

Setup Stability

Probe Card Technology

Manufacturing Challenges – High Speed Sort

Setup Stability

- **Full system setup involves multiple vendors**
-

Probe Card Technology

Manufacturing Challenges – High Speed Sort

Setup Stability

- Full system setup involves multiple vendors
- Poor planarity which can't be addressed by conventional setup check

Probe Card Technology

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- No established / reference S.O.P

Probe Card Technology

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Probe Card Technology

- Light / weak probe marks on RF pins

Manufacturing Challenges – High Speed Sort

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Probe Card Technology

- Light / weak probe marks on RF pins
- Probe mark uniformity issue

Manufacturing Challenges – High Speed Sort

Setup Stability

- Full system setup involves multiple vendors
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Probe Card Technology

- Light / weak probe marks on RF pins
- Probe mark uniformity issue
- IR drop induced failures

Manufacturing Challenges – High Speed Sort

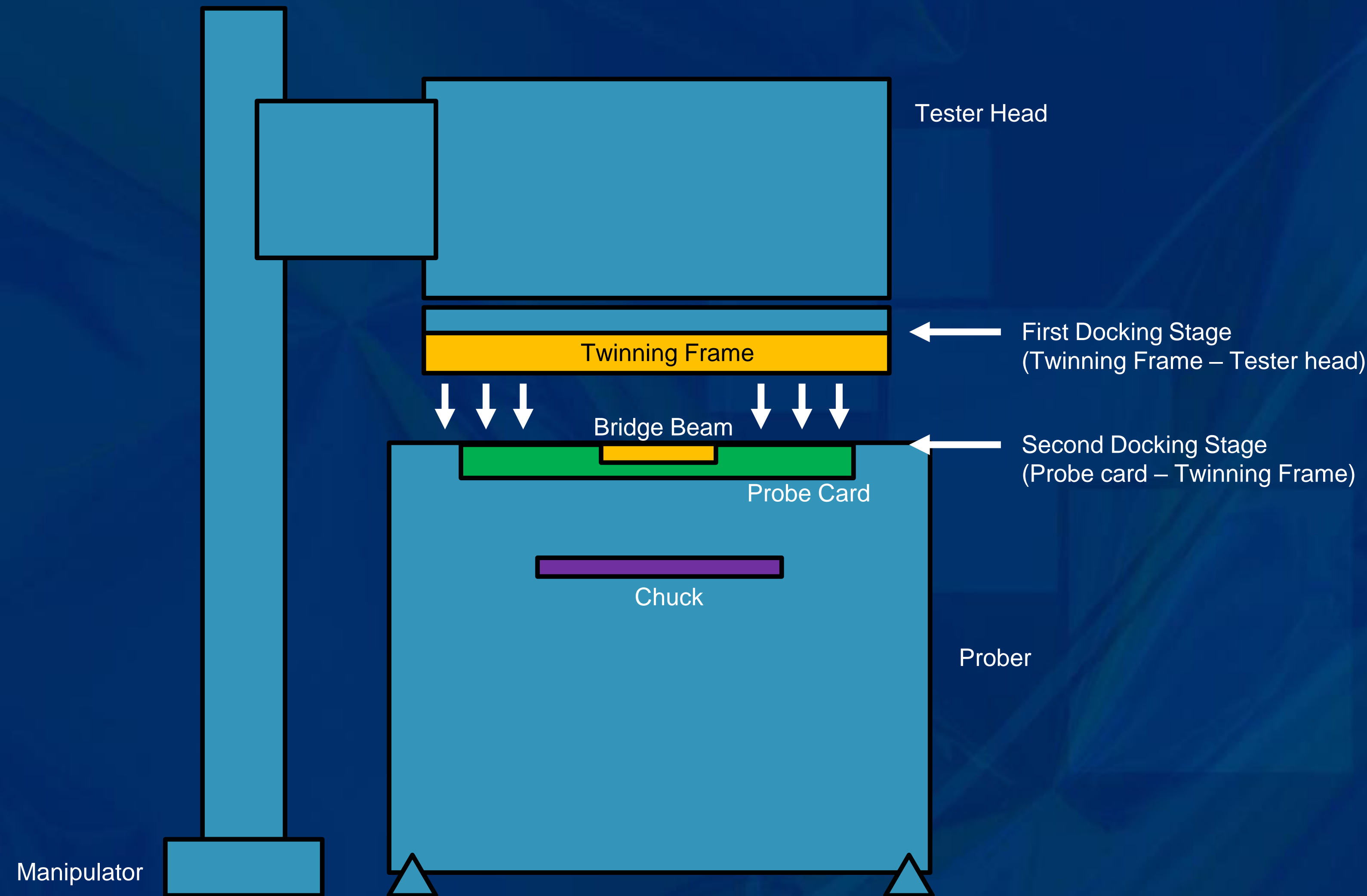
Setup Stability

- Full system setup involves multiple vendors
- Poor planarity which can't be addressed by conventional setup check
- No established / reference S.O.P

Probe Card Technology

- Light / weak probe marks on RF pins
- Probe mark uniformity issue
- IR drop induced failures
- Low yield after "x" touchdown

KGD Wafer Sort Setup - Twinning Frame



First Docking Stage
(Twinning Frame – Tester head)

Second Docking Stage
(Probe card – Twinning Frame)

KGD Wafer Sort Setup - Twinning Frame

Tester Head

Twinning Frame

Bridge Beam

Probe Card

Chuck

Prober

Manipulator

First Docking Stage
(Twinning Frame – Tester head)

Second Docking Stage
(Probe card – Twinning Frame)

Source: Advantest

KGD Wafer Sort Setup - Twinning Frame

Tester Head

Twinning Frame

Bridge Beam

Probe Card

Chuck

Prober

Manipulator

First Docking Stage
(Twinning Frame – Tester head)

Second Docking Stage
(Probe card – Twinning Frame)

Tester Head

Twinning Frame

Prober

Tester Head

Twinning Frame

Prober

Source: Advantest

KGD Wafer Sort Setup - Twinning Frame

Tester Head

Twinning Frame

First Docking Stage
(Twinning Frame – Tester head)

Bridge Beam

Second Docking Stage
(Probe card – Twinning Frame)

Probe Card

Chuck

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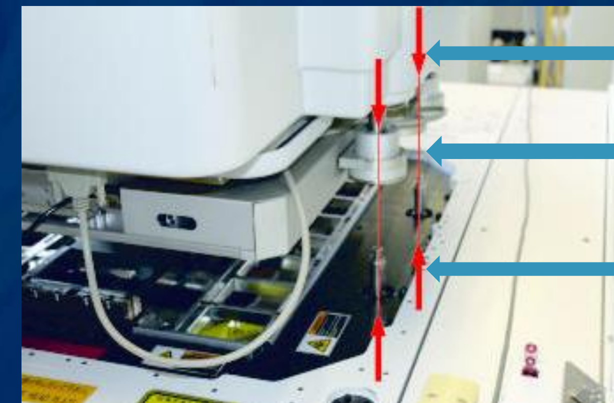
Tester Head

Twinning Frame

Prober



Tester Head

Twinning Frame

Prober

Source: Advantest

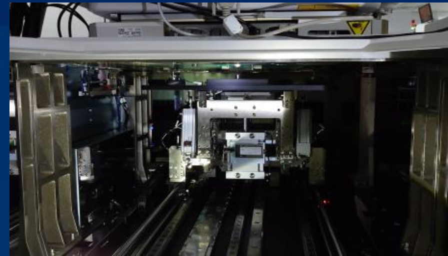
Setup Planarization Issue – Example of Failure

Poor Planarity After Docking

Each pin tolerance information
X: 20 Y: 50 Z: 20
Highest pin : -7483
Lowest pin : -7539
P/C Flatness : 56
(Unit: um)

No.	Status	Diff. X	Diff. Y	Diff. Z	Height	Group	Area
0	PASS	0	0	1	-7483	0	N/A
1	PASS	-1	0	-3	-7539	1	N/A
2	PASS	0	-1	0	-7535	2	N/A
3	PASS	1	0	-3	-7495	3	N/A

Hardware Damages:

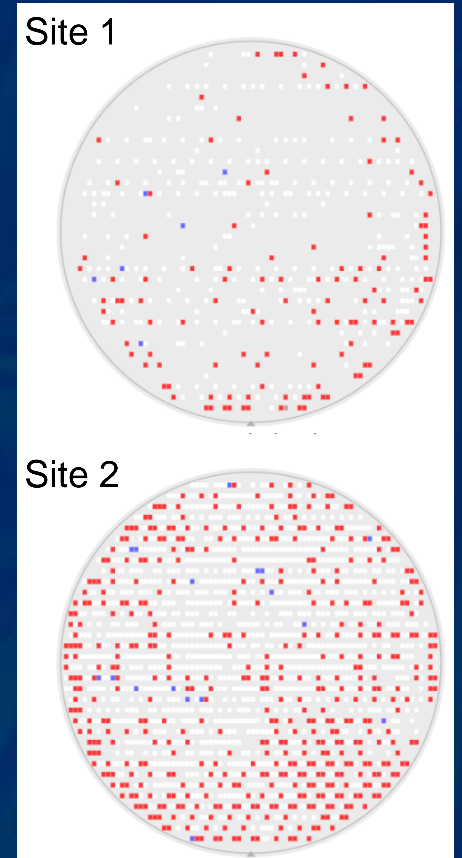


Probe Card Stuck

Damaged SMPM Connectors

Damaged Probe Card

Low Yield & High Site-to Site Variation



Setup Planarization Issue Overview

Before Docking

Prober / Chuck Planarization

Tester Head Leveling

Tester Manipulator Adjustment

Setup Planarization Issue Overview

Before Docking

Prober / Chuck Planarization

Tester Head Leveling

Tester Manipulator Adjustment

After Docking

Setup Planarization Issue Overview

Before Docking

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After Docking

Twinning Frame?

Probe Card?

Prober?

Manipulator?

Tester?

Setup Planarization Issue Overview

Before Docking

Prober / Chuck Planarization

Tester Head Leveling

Tester Manipulator Adjustment

After Docking

Tester Vendor
Module Vendor

Twinning Frame?

Probe Card Vendor

Probe Card?

Prober?

Manipulator?

OSAT
Prober Vendor

OSAT
Tester Vendor

Tester?

OSAT
Tester Vendor

Setup Planarization Issue Overview

Before Docking

Prober / Chuck Planarization

Tester Head Leveling

Tester Manipulator Adjustment

After Docking

Tester Vendor
Module Vendor

Twinning Frame?

Probe Card Vendor

Probe Card?

Prober?

Manipulator?

OSAT
Prober Vendor

OSAT
Tester Vendor

Tester?

OSAT
Tester Vendor

Who is responsible ?

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
- Tester Head Leveling
- Tester Manipulator Adjustment

Setup Planarization Issue Resolution

Before Docking

Prober Planarization

Tester Head Leveling

Tester Manipulator Adjustment

Unlock Tester Head

Guide Pins Height Standardization

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
- Tester Head Leveling
- Tester Manipulator Adjustment
- Unlock Tester Head
- Guide Pins Height Standardization

After Docking

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
- Tester Head Leveling
- Tester Manipulator Adjustment
- Unlock Tester Head
- Guide Pins Height Standardization

After Docking

- Planarity
- VPG
- Probe Card loading SOP

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
- Tester Head Leveling
- Tester Manipulator Adjustment
- Unlock Tester Head
- Guide Pins Height Standardization

After Docking

Planarity → VPG → Probe Card loading SOP → Planarity

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
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After Docking

Planarity → VPG → Probe Card loading SOP → Planarity → Probe Card

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
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- Unlock Tester Head
- Guide Pins Height Standardization

After Docking

Planarity → VPG → Probe Card loading SOP

Probe Card loading SOP → Planarity → Probe Card

Probe Card loading SOP → Low Yield

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
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- Tester Manipulator Adjustment
- Unlock Tester Head
- Guide Pins Height Standardization

After Docking

Planarity → VPG → Probe Card loading SOP

→ Planarity → Probe Card

→ Low Yield

Probe Card | Multilane | Material

Setup Planarization Issue Resolution

Before Docking

- Prober Planarization
- Tester Head Leveling
- Tester Manipulator Adjustment
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- Guide Pins Height Standardization

After Docking

Planarity

VPG

Probe Card loading SOP

Planarity

Probe Card

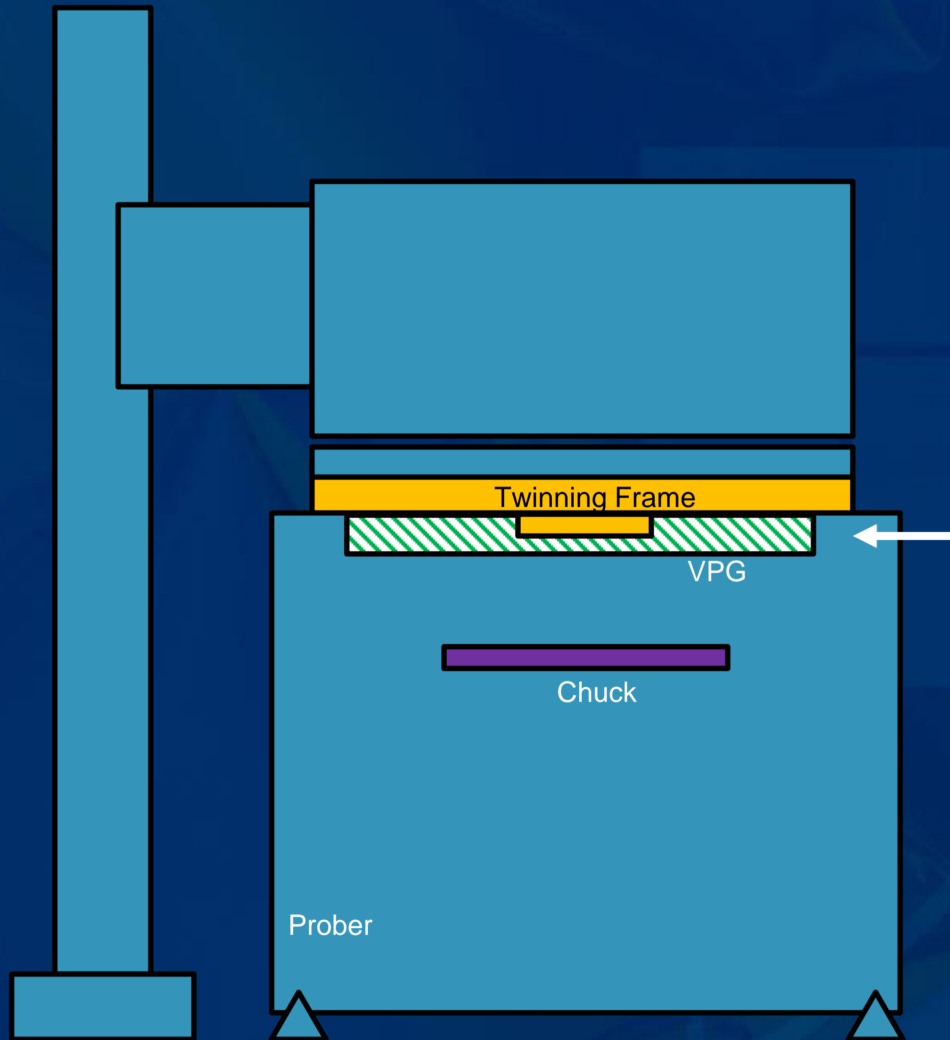
Low Yield

Probe Card

Multilane

Material

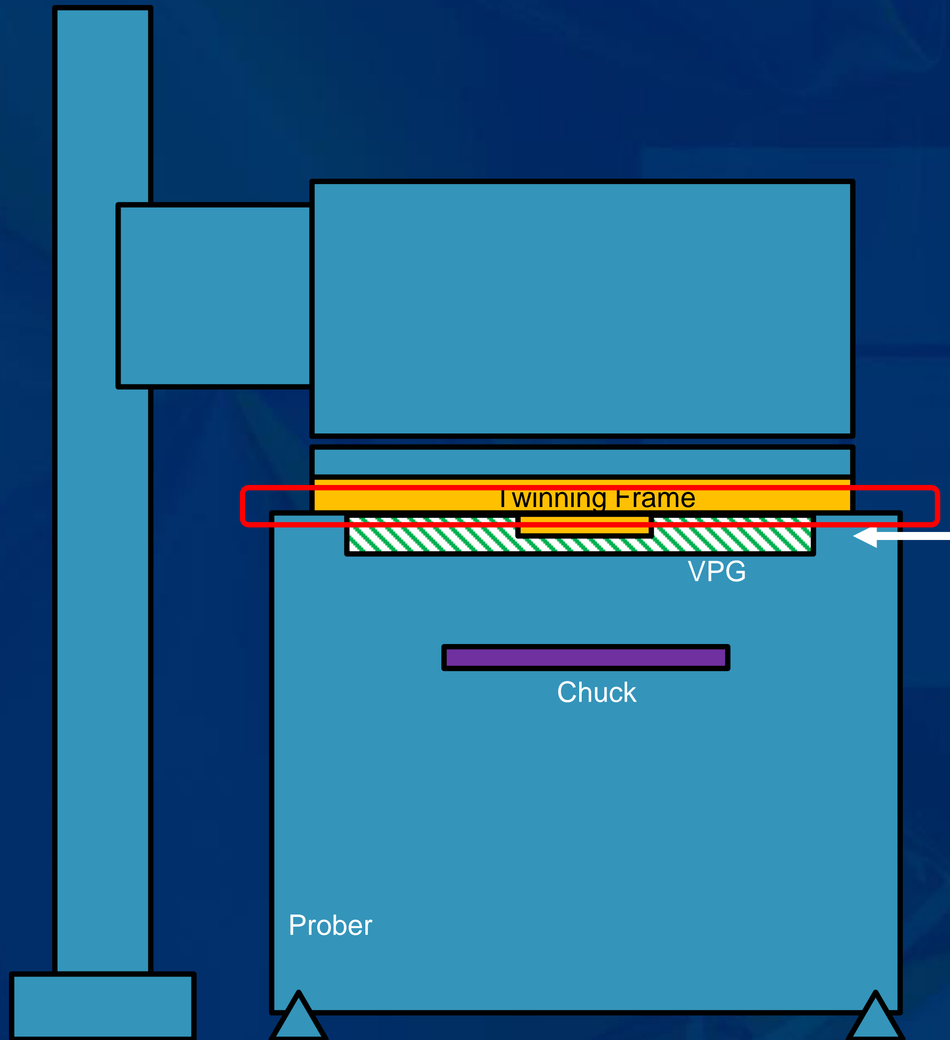
VPG – Verigy Planarization Gauge



- Very effective for prober without auto leveling feature
- Allows minor adjustment to be done on tester head rest planarity
- Reflects the actual planarity on a fully docked system

- Designed and calibrated by Advantest
- Adjustment was done based on 5 calibrated points on VPG unit to meet the expected planarity

VPG – Verigy Planarization Gauge



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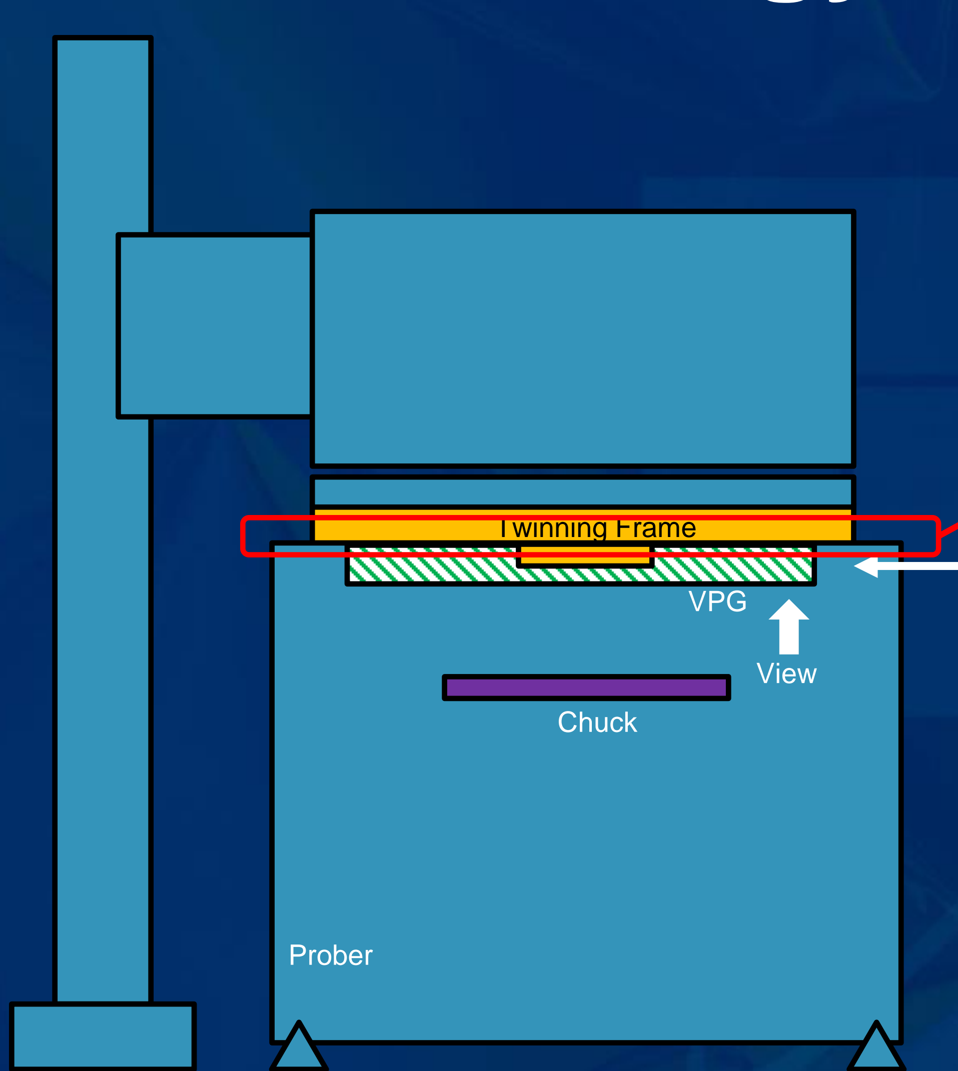

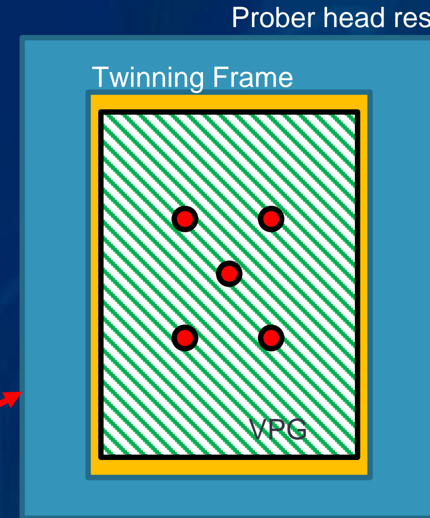

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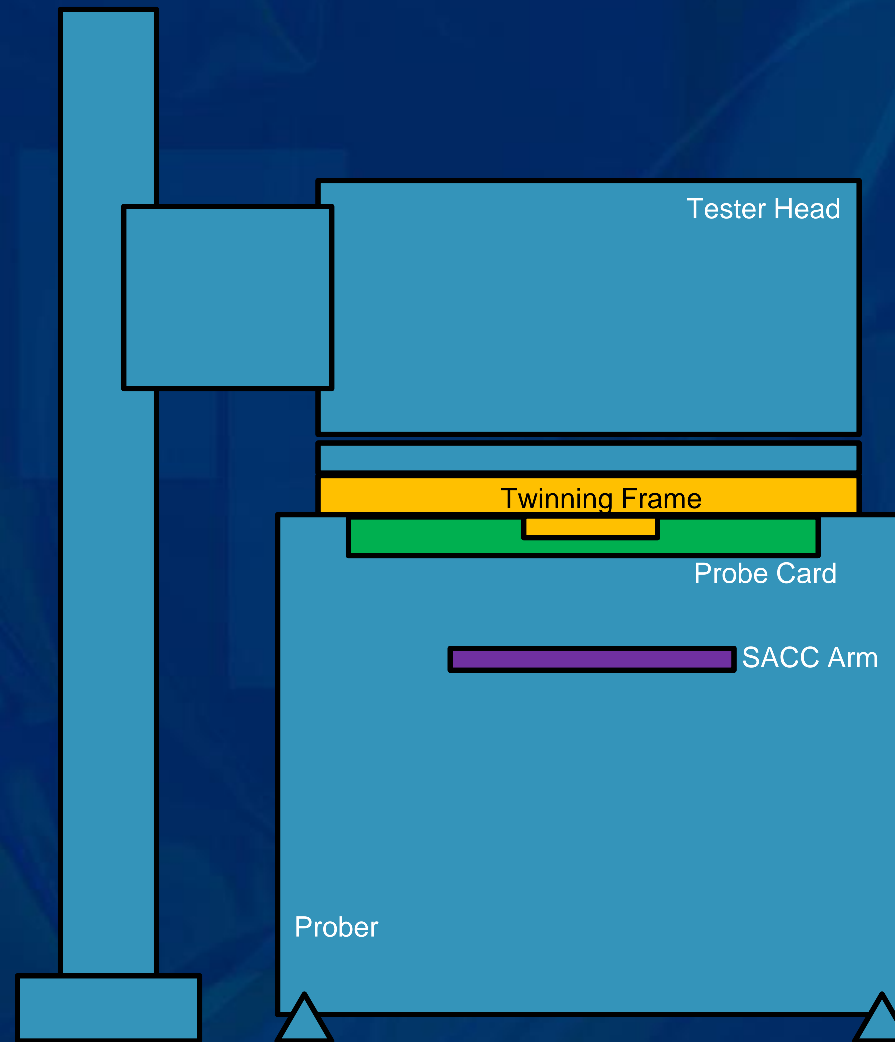
KGD System Setup and Probe Card Loading SOP



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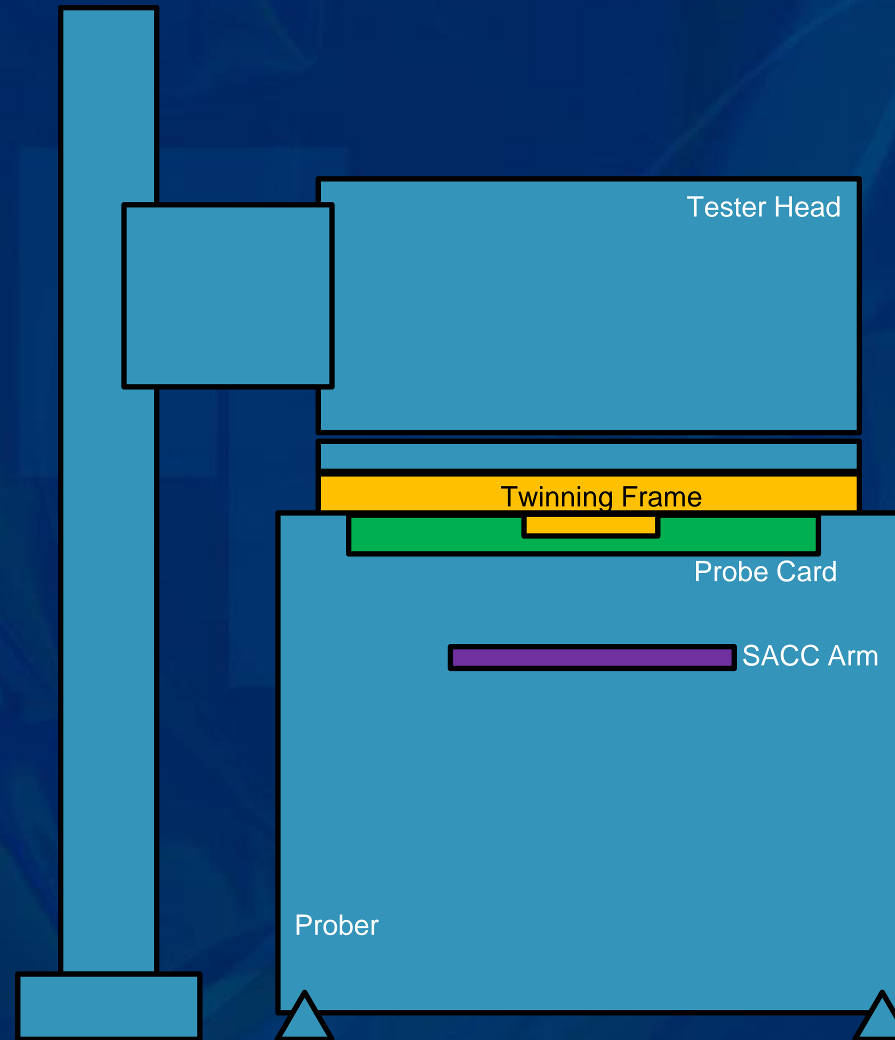
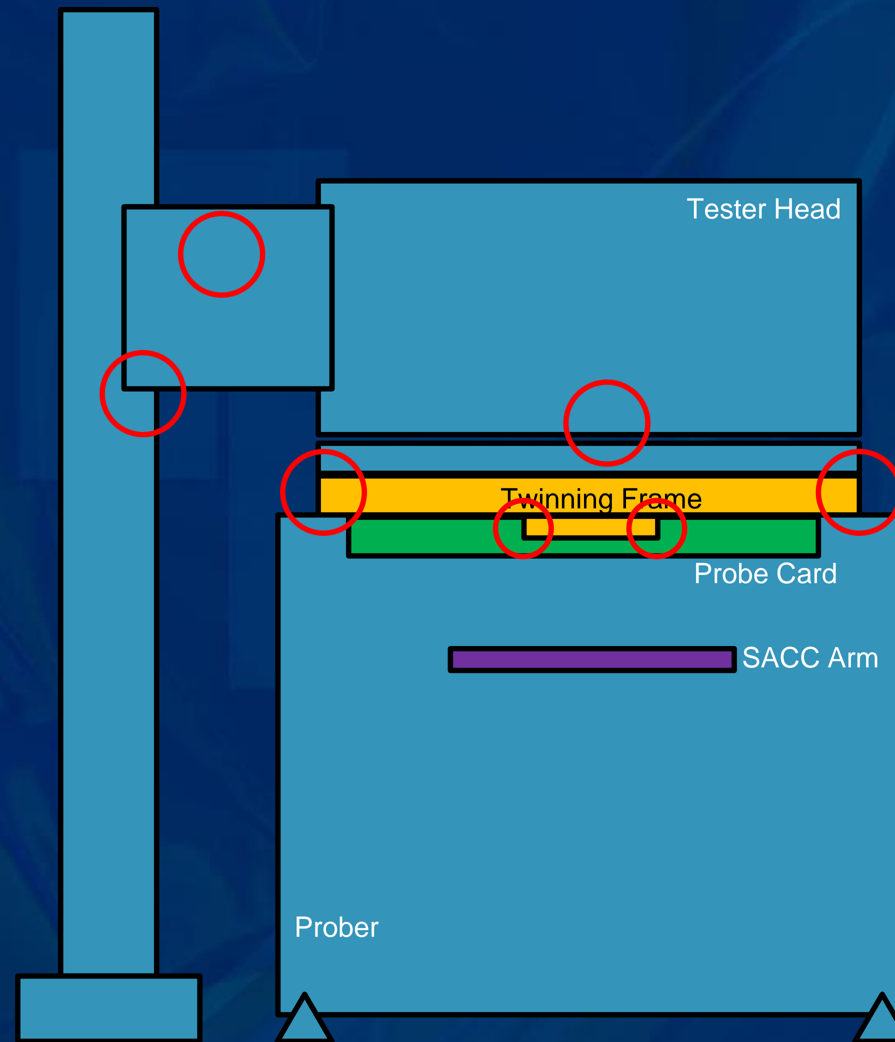


- Multiple external forces / vectors are acting to the probe card during docking process
- These vectors came from various component ie. Tester head, prober , twinning frame, bridge beam, and probe cards

KGD System Setup and Probe Card Loading SOP



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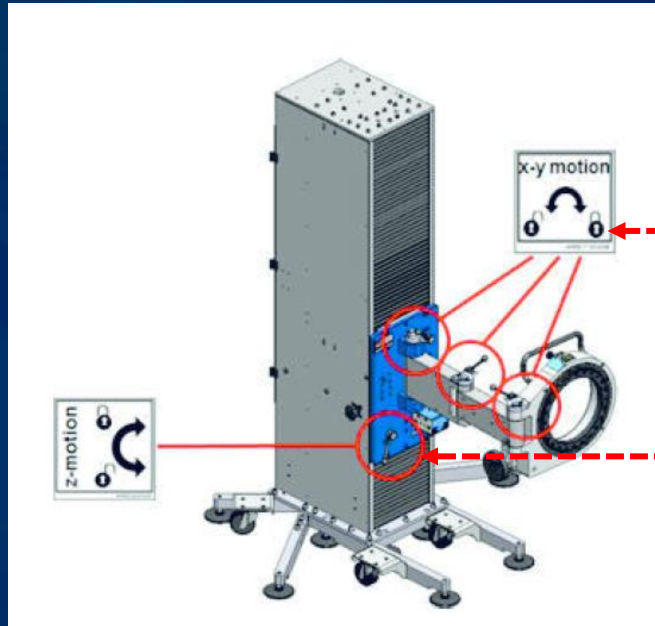
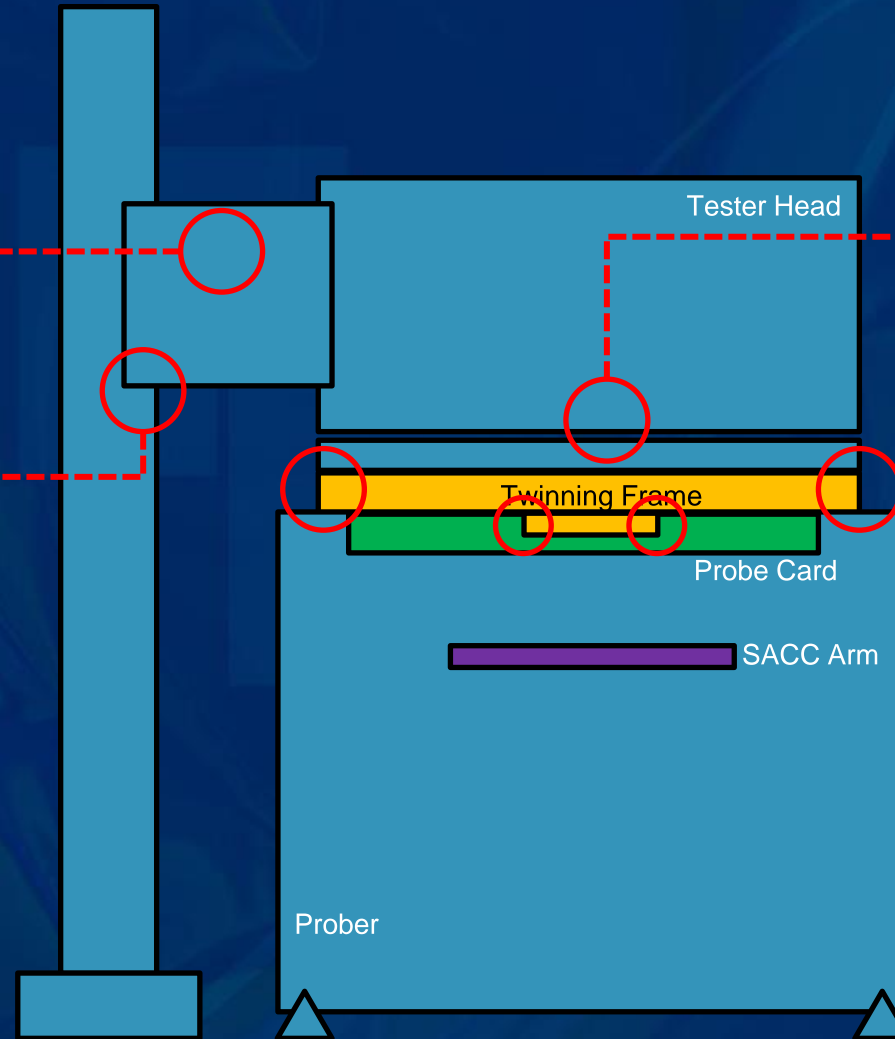
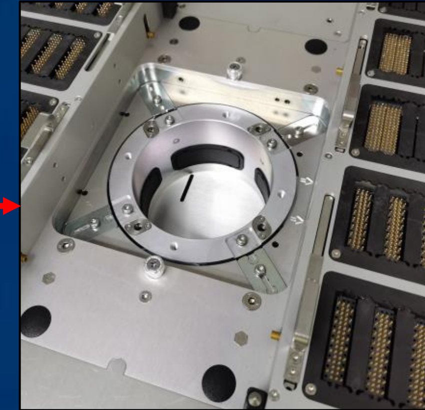


Source: Advantest





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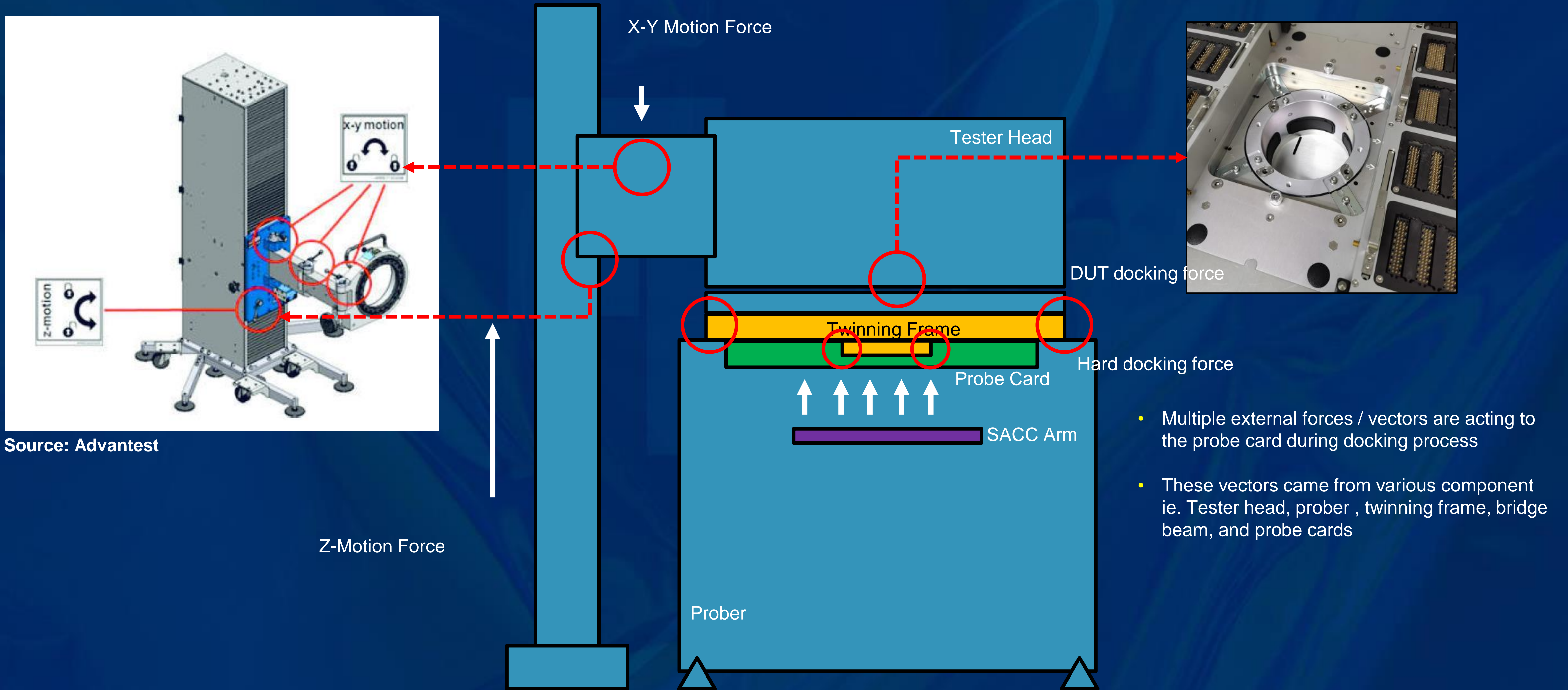

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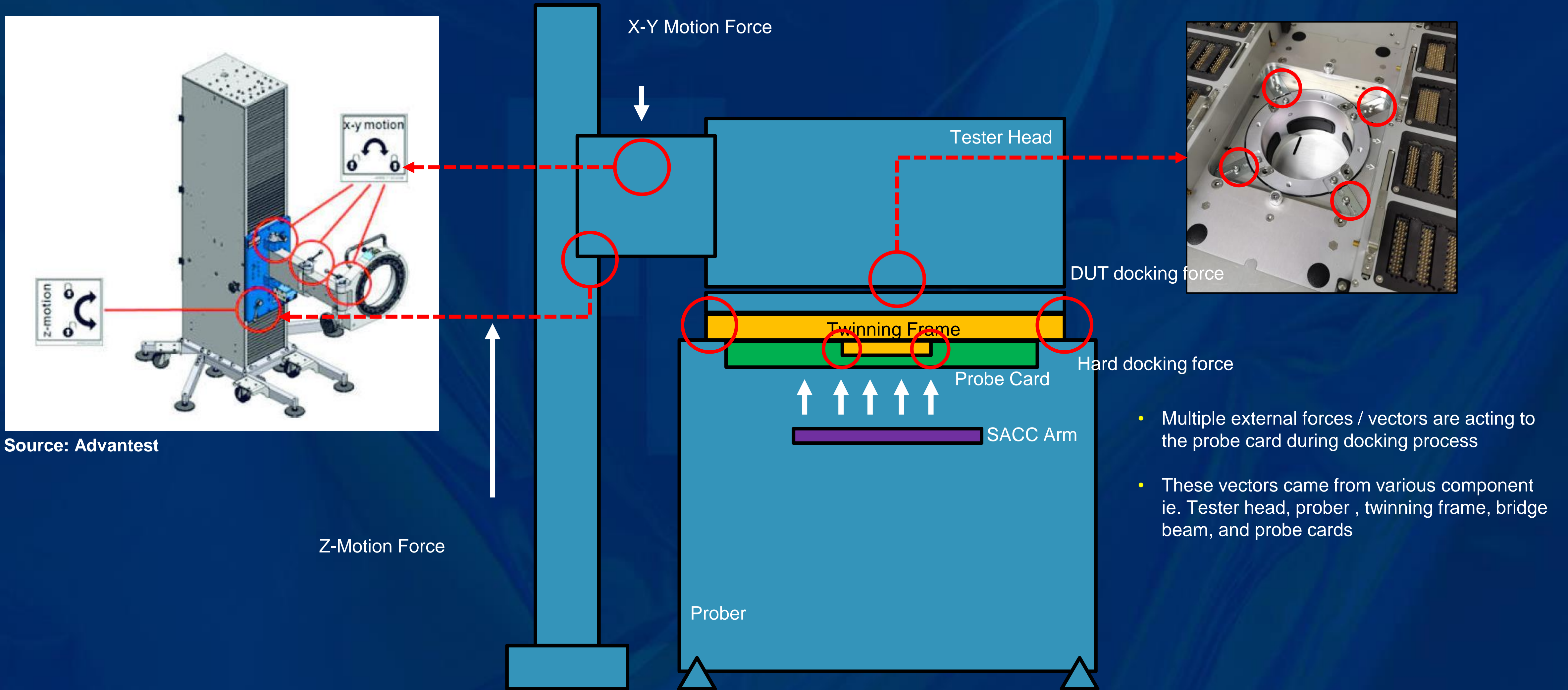

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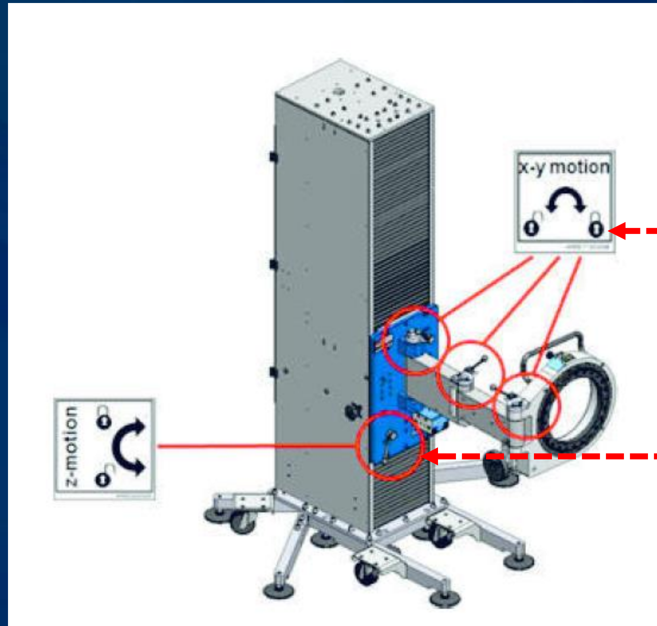

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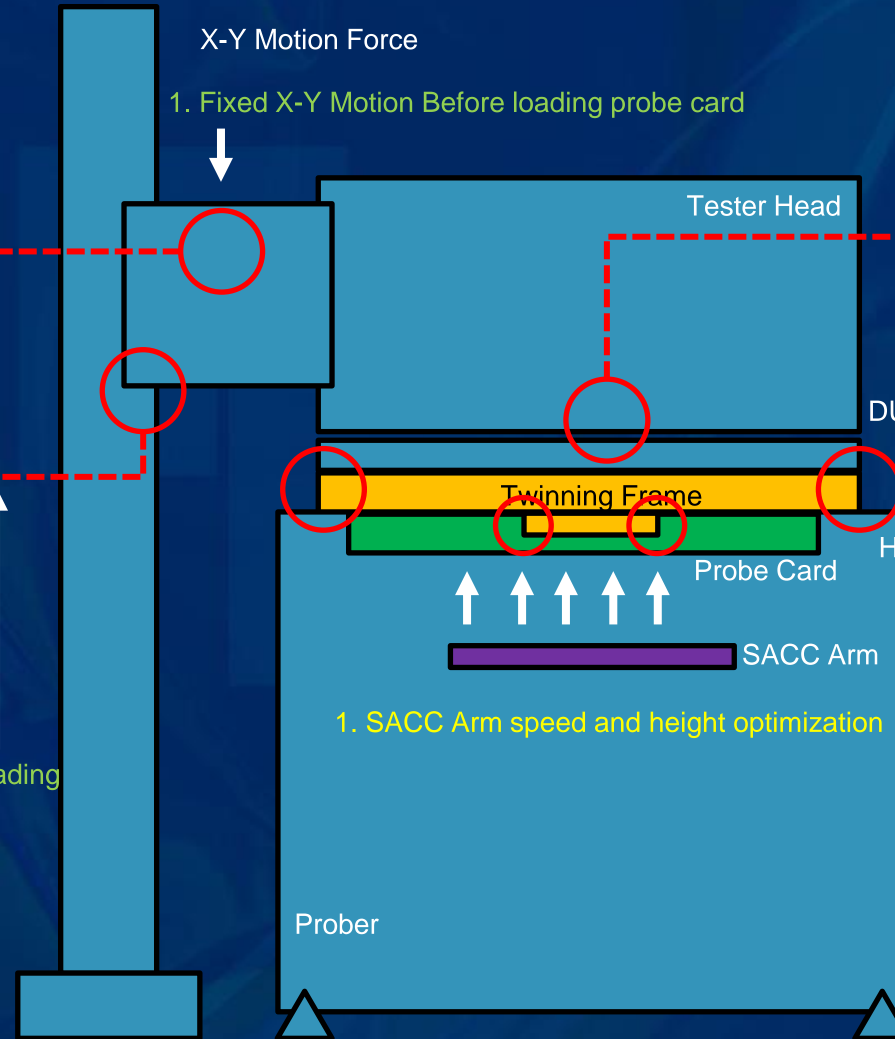

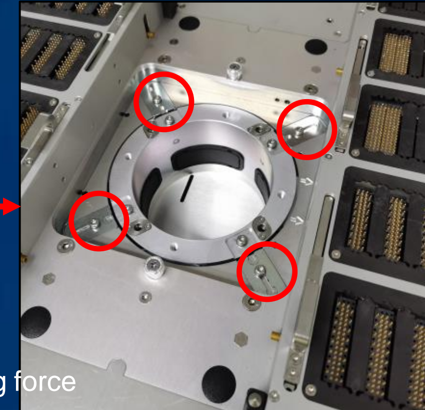

2. Release tester head – allowing better tolerance to external forces

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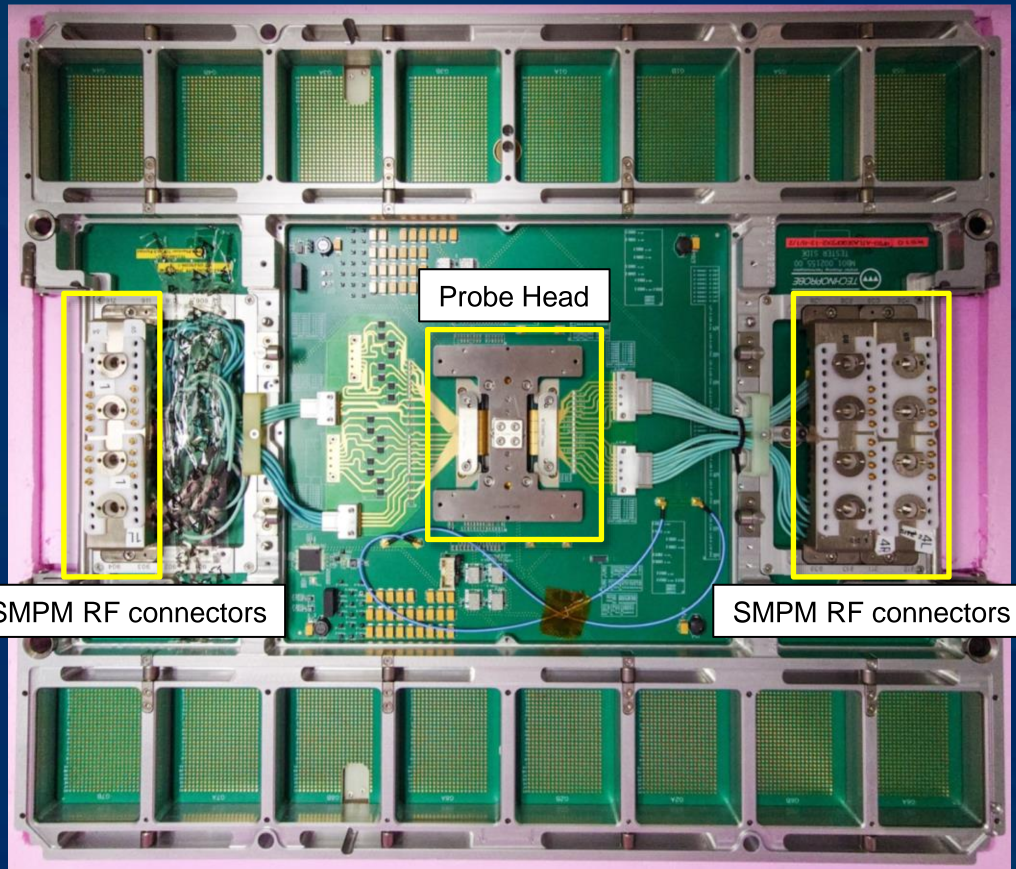
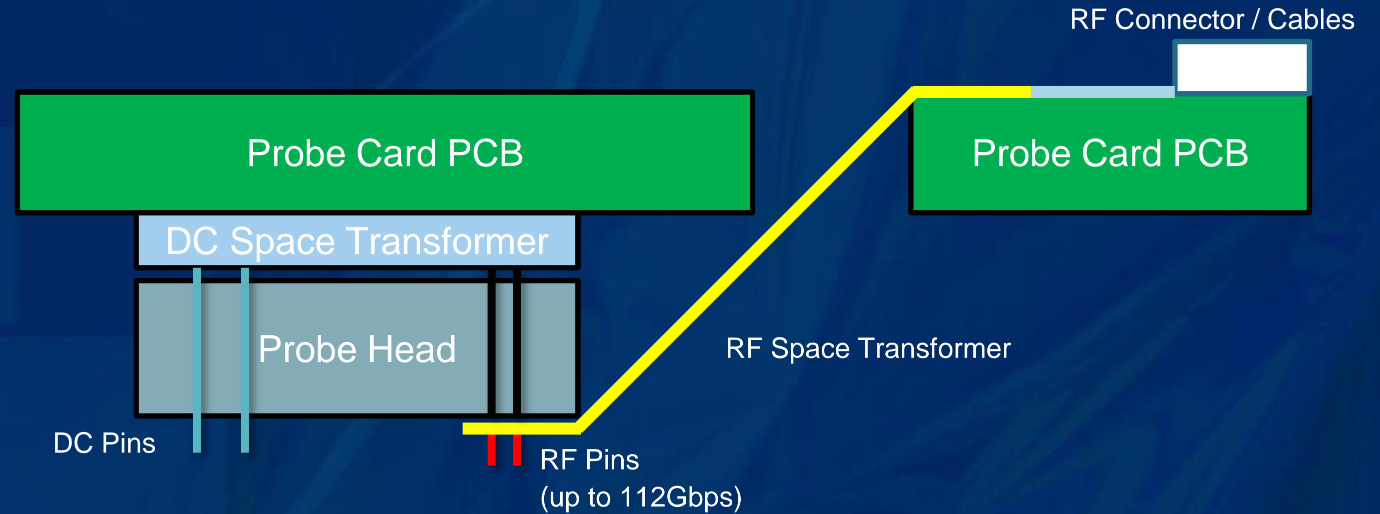
Probe Card Overview





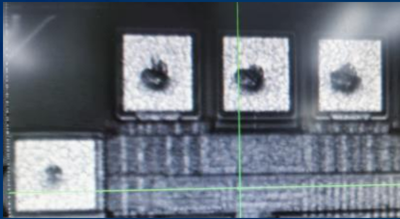
Source: Technoprobe

Probe Card Issue and Challenges

- Probe Needle Planarity
- Long setup time
- Irregular Probe marks
- High Working OD
- Contact Issue
- Needle's IR drop
- Performance degradation over time
- Handling / Sustaining
- Cleaning Activation Routine

Probe Needles' Planarity

- Unoptimized alignment
- Risk of probing at edges of pad



- Uniformity issue
- Poor contact
- High overtravel
- Inconsistent overtravel across probe cards
- Risk of damaging circuit under pad

Probe Needles' Planarity

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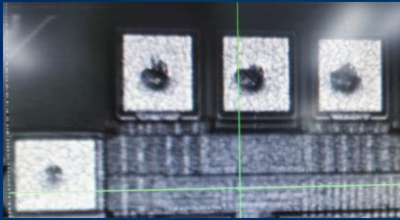

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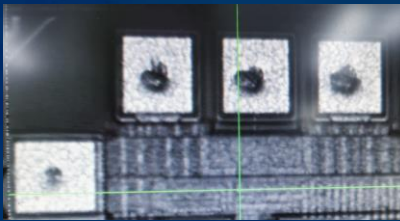
Gen 1
- Lower gram force
- High delta between OD1 and OD2
- Aggressive WOD required to get stable contact
- Inconsistent WOD across different probe cards

Probe Needles' Planarity

- Unoptimized alignment
- Risk of probing at edges of pad



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<u>Gen 1</u>

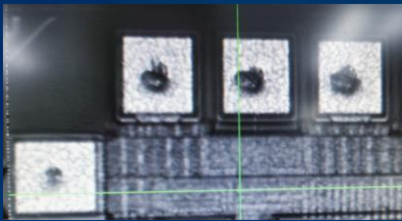
- Lower gram force
- High delta between OD1 and OD2
- Aggressive WOD required to get stable contact
- Inconsistent WOD across different probe cards

<u>Gen 2</u>

- Lower gram force
- High delta between OD1 and OD2
- Next generation of guide plate was introduced to strengthen probing
- Less aggressive WOD
- Inconsistent WOD across different probe cards

Probe Needles' Planarity

- Unoptimized alignment
- Risk of probing at edges of pad



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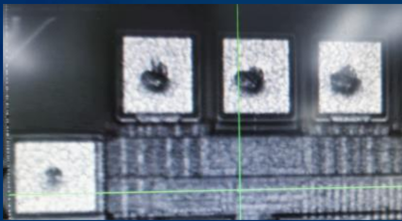
Gen 2
- Lower gram force
- High delta between OD1 and OD2
- Next generation of guide plate was introduced to strengthen probing
- Less aggressive WOD
- Inconsistent WOD across different probe cards

→

Gen 3
- Higher gram force
- Small delta between OD1 and OD2
- Consistent WOD recipe can be applied
- Higher pin resistivity causing IR drop on power pins (40% higher)

Probe Needles' Planarity

- Unoptimized alignment
- Risk of probing at edges of pad



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→

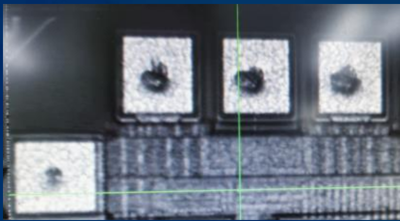
Gen 3
- Higher gram force
- Small delta between OD1 and OD2
- Consistent WOD recipe can be applied
- Higher pin resistivity causing IR drop on power pins (40% higher)

→

Gen 4
- Higher gram force
- Small delta between OD1 and OD2
- Consistent WOD recipe can be applied
- Lower pin resistivity

Probe Needles’ Planarity

- Unoptimized alignment
- Risk of probing at edges of pad



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- High delta between OD1 and OD2
- Aggressive WOD required to get stable contact
- Inconsistent WOD across different probe cards

→

Gen 2
- Lower gram force
- High delta between OD1 and OD2
- Next generation of guide plate was introduced to strengthen probing
- Less aggressive WOD
- Inconsistent WOD across different probe cards

→

Gen 3
- Higher gram force
- Small delta between OD1 and OD2
- Consistent WOD recipe can be applied
- Higher pin resistivity causing IR drop on power pins (40% higher)

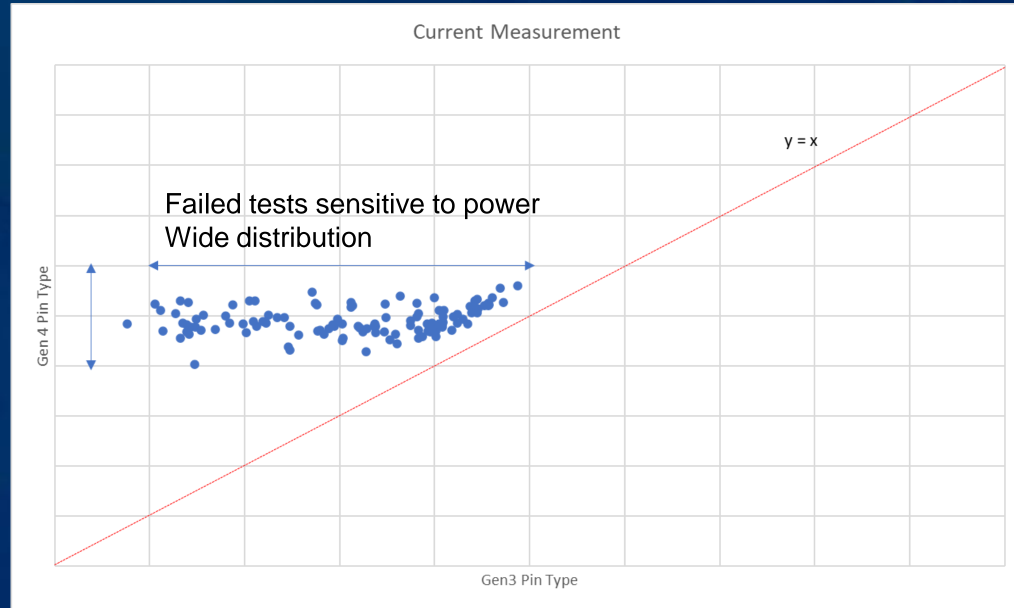
→

Gen 4
- Higher gram force
- Small delta between OD1 and OD2
- Consistent WOD recipe can be applied
- Lower pin resistivity

→

Gen 5
- Thicker gold plating being introduced to further reduce overall resistivity on DC power pins

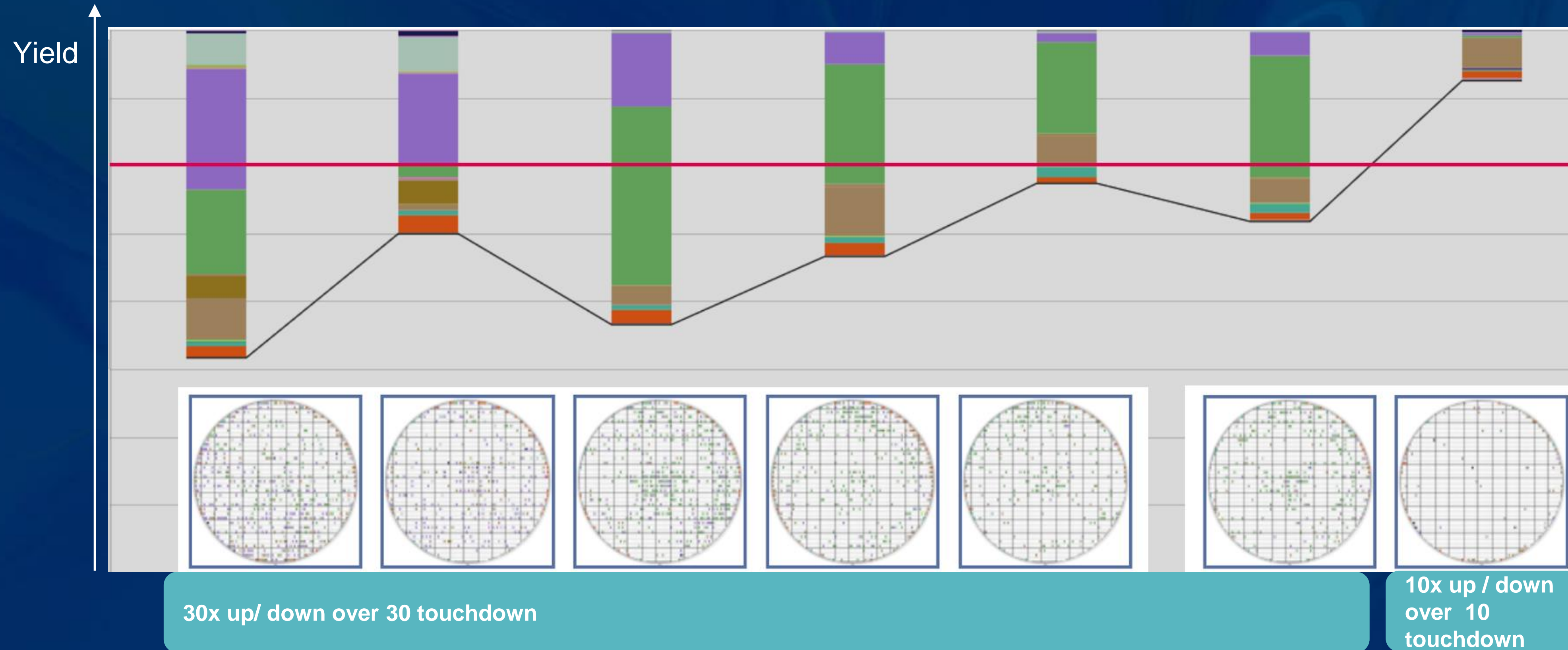
IR Drop Issue



- **Current measurement of Gen3 (x-axis) vs Gen4 (y-axis) pin type on same samples**

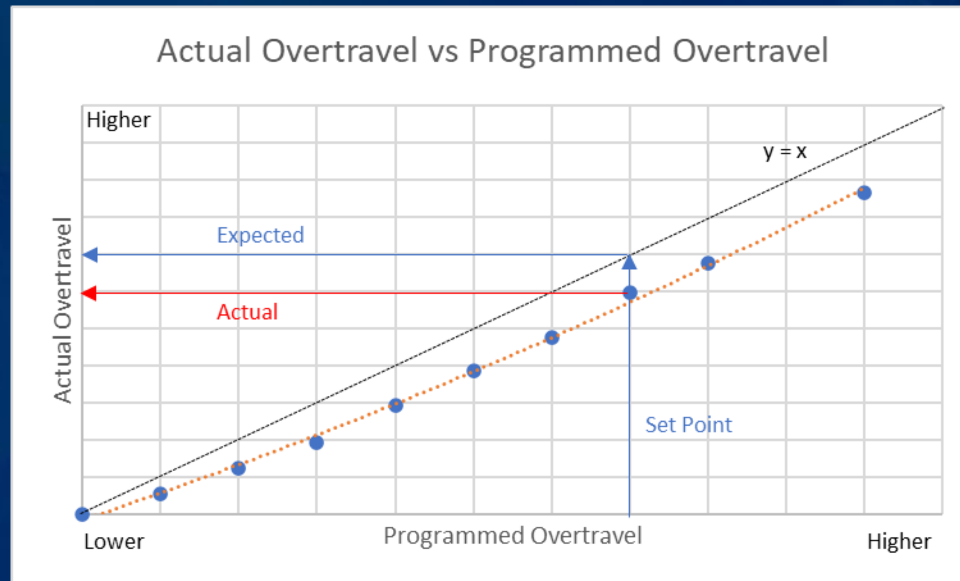
- **IR Drop is contributed by**
  - Probe needles' characteristic (Resistivity) – addressed with lower resistivity needle type
    - Historical data revealed yield loss on voltage sensitive tests reduced from > 40% to <5%
  - Poor Contact – requires optimized cleaning recipe
    - Cumulated particles over time
    - Oxidation

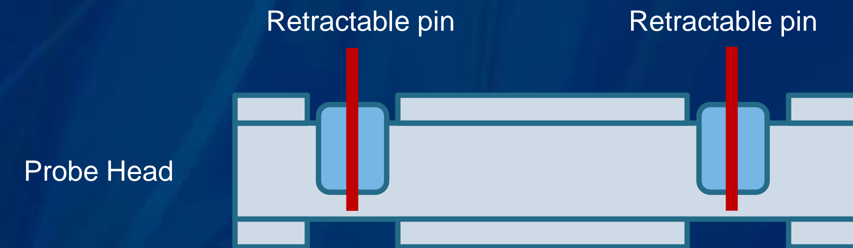
Probe Card - Sustaining and Handling



- **Aggressive cleaning resulted in better yield with the trade off over the needles' life span**

Contact Issue – Actual Overtravel vs Programmed Overtravel





Configuration for AOT vs POT characterization

Source: Technoprobe

- **Programmed Overtravel: setting on prober UI**
- **Actual Overtravel: Resultant overtravel considering the deflection of the system (Prober, Bridge Beam, Probe Card Load)**
- **The study provides additional margin in POT, helps in achieving better contact, lower contact resistance. Improving yield on contact sensitive tests.**

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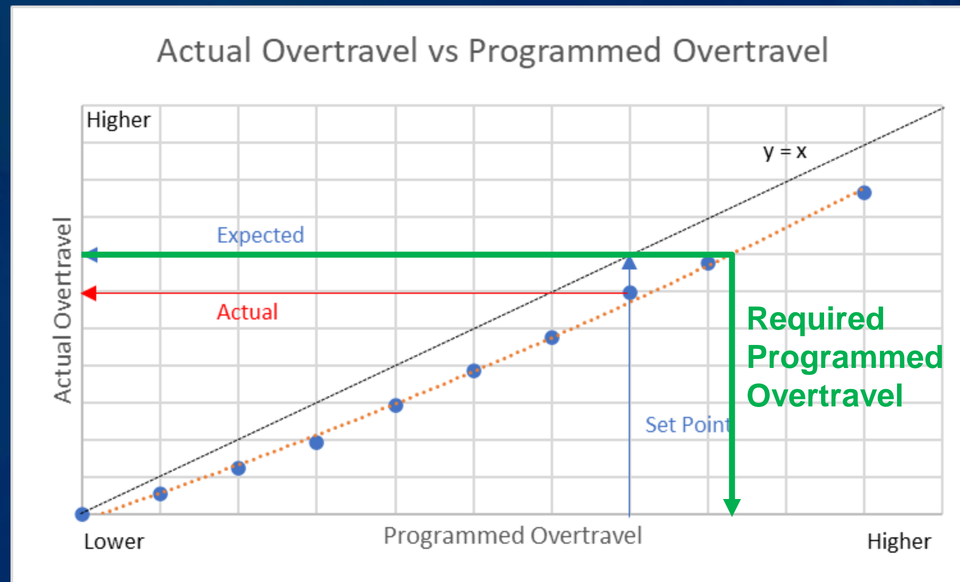

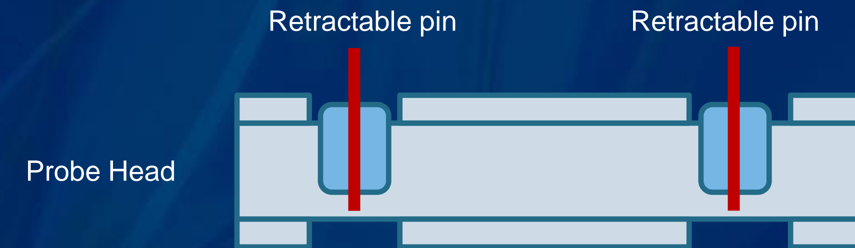

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Conclusions

- **Wafer sort setup with twinning options is a solution to high-speed testing for KGD products with limited loopback capability**
- **Stable high-volume manufacturing setups are achievable via:**
  - Studying the root cause and narrowing down the components leading to setup planarity issue
  - Establishing new S.O.P governing the initial setup and regular production routine
  - Continue collaboration with vendors in exploring existing and new technology to optimize product yield