HOW TO ALIGN 3D ICs FOR TESTING AT DIE LEVEL

Using AMT5000 & HBM as an Example

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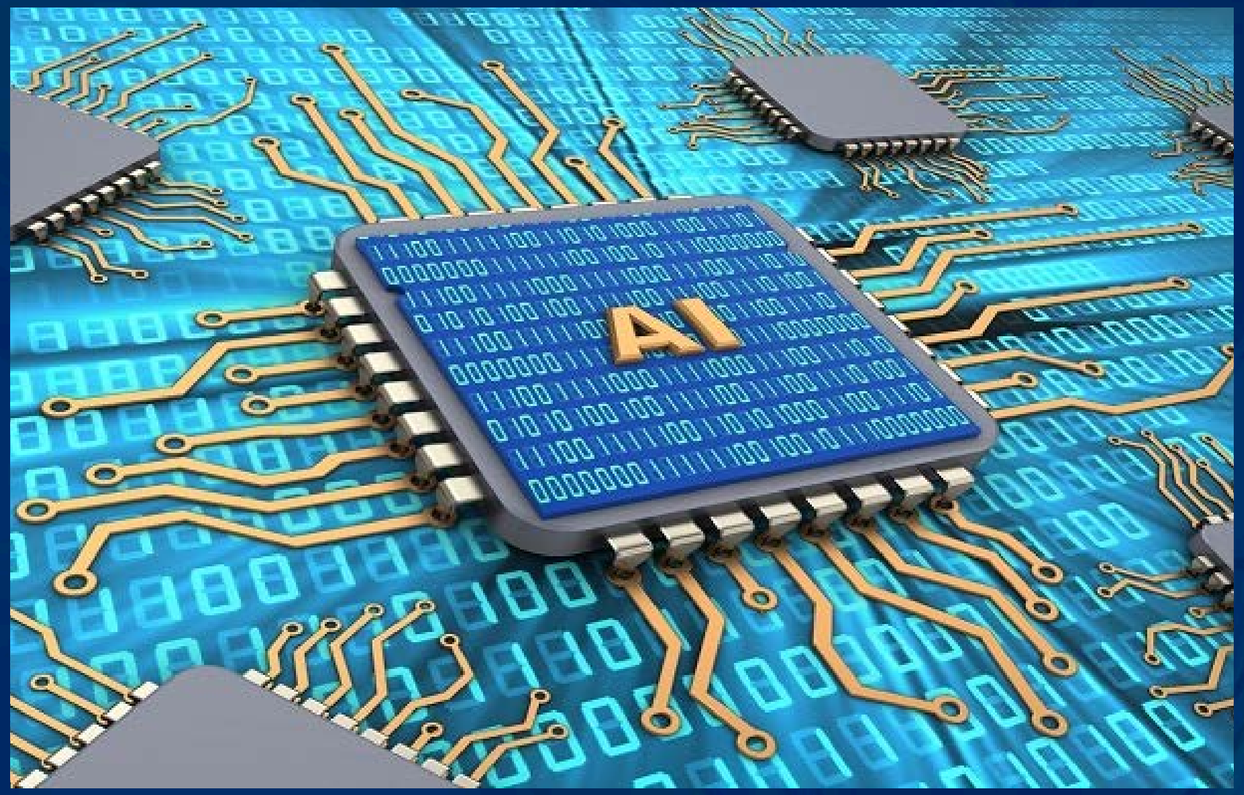
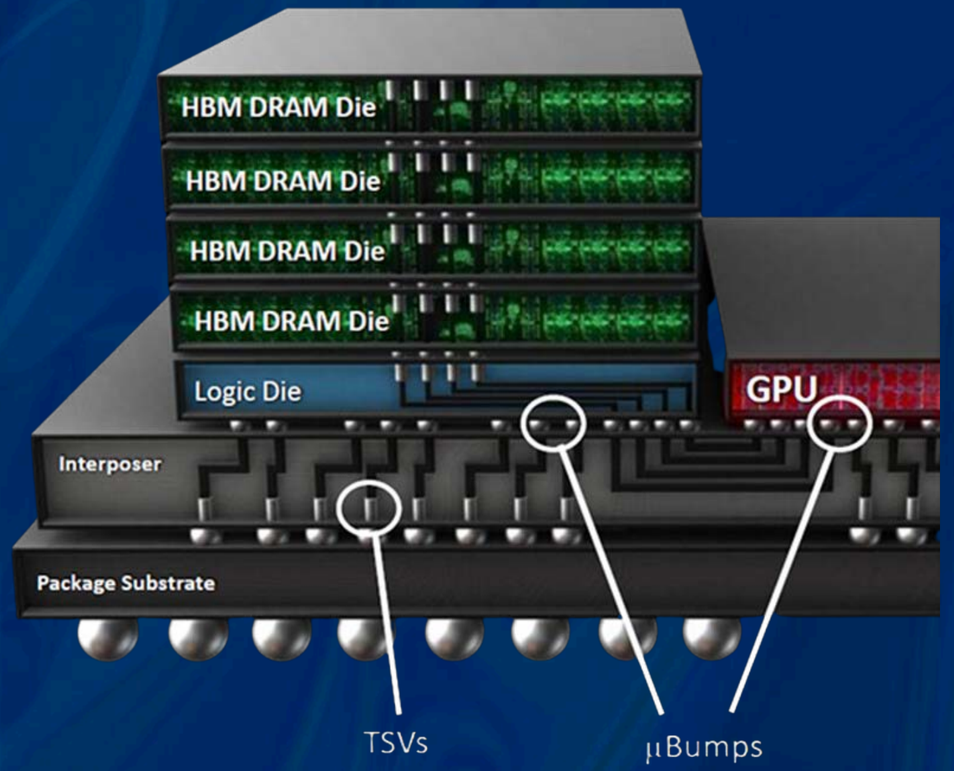
4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

Overview

- Advent of 3D “Stacked” ICs
- The Architecture of 3D ICs – HBM
- Current Testing Methods for HBM – Wafer Level Testing
- Importance of Die Level Testing
- Challenges in Testing HBMs at Die Level
- How to Perform Die Level Test for HBMs
- AMT5000 - Design Parameters & Considerations
- AMT 5000 Die Alignment Precision Measurement Method
- AMT 5000 Die Alignment Precision Test Result
- AMT5000 - Technical Capabilities
- Summary

Advent of 3D “Stacked” ICs



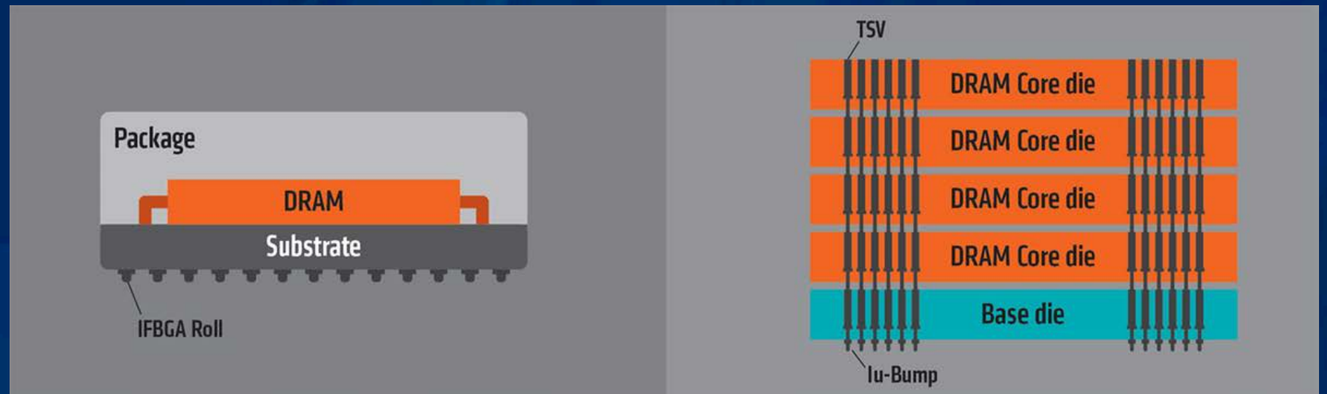


3D IC architecture is the new standard in memory chip design

An explosion of market demand for HBM chips – e.g., AI Accelerators

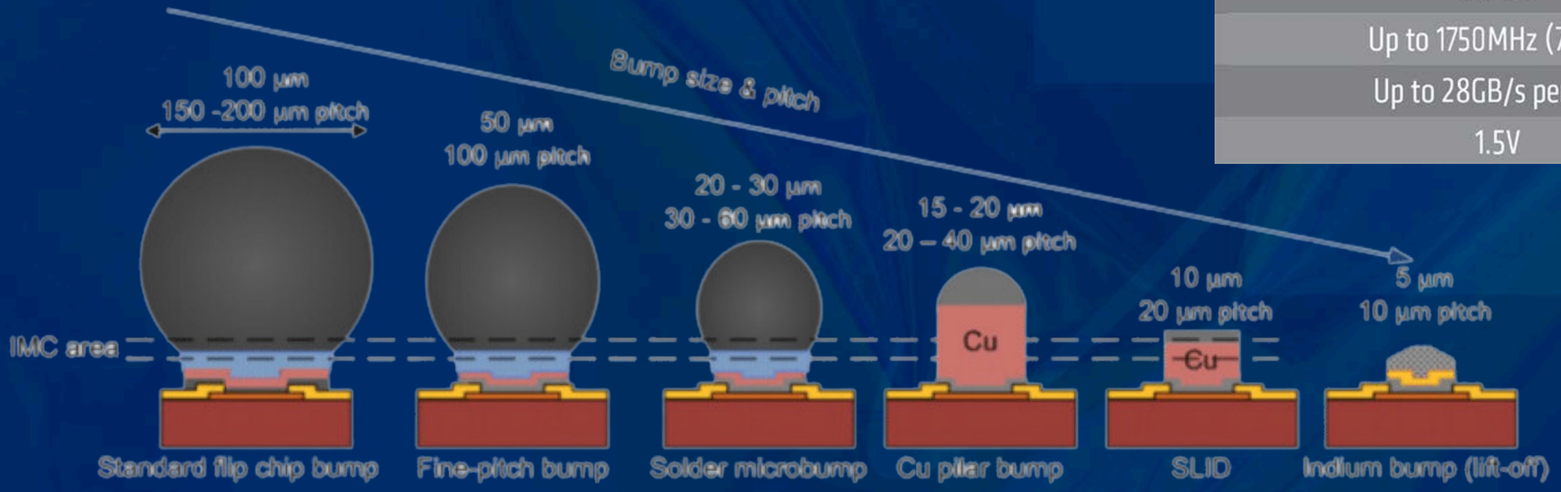
Architecture of 3D “Stacked” ICs - HBM

The “stacked” architecture necessitated ultra-fine pitch between I/O connectors.



GDDR5	Per Package	HBM
32-bit	Bus Width	1024-bit
Up to 1750MHz (7GBps)	Clock Speed	Up to 500MHz (1GBps)
Up to 28GB/s per chip	Bandwidth	>100GB/s per stack
1.5V	Voltage	1.3V

Declining size of the contact pads



32 I/O vs. 1024 I/O

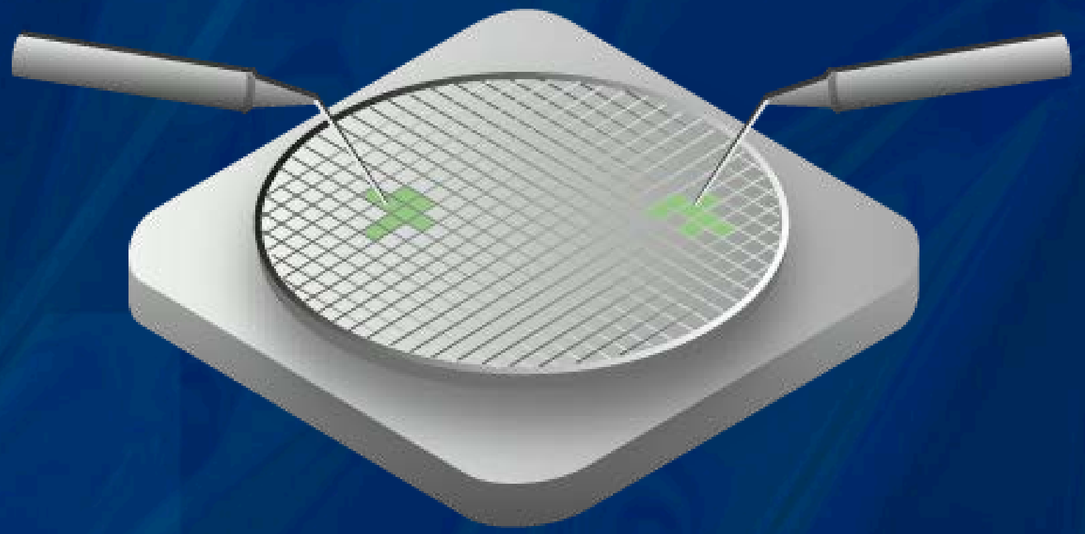
28GB vs. +100GB

Current Testing Methods for HBM

Wafer Level Probing

The small pitch between the bumps in HBM chips present a challenge for testing:

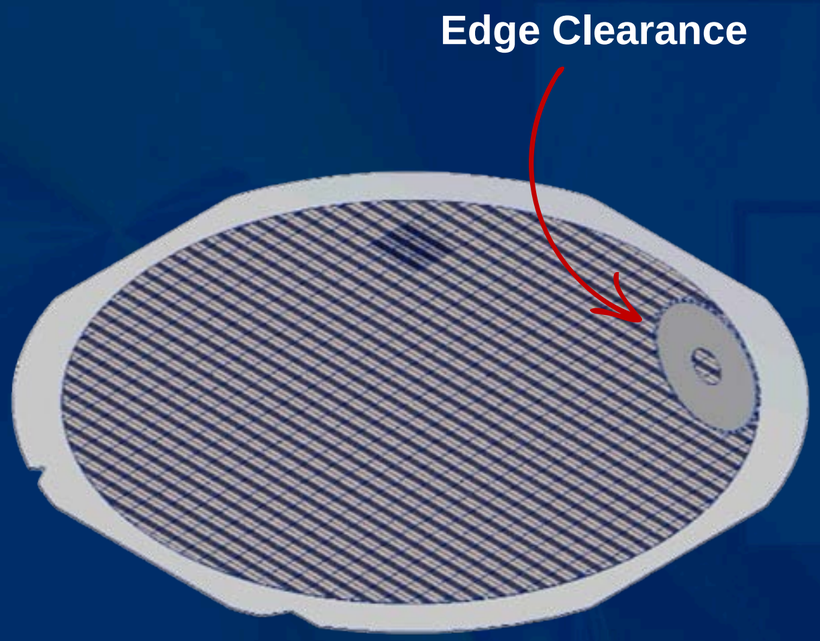
- **difficult access to individual bumps for testing**
- **increases the risk of crosstalk or interference between signals.**

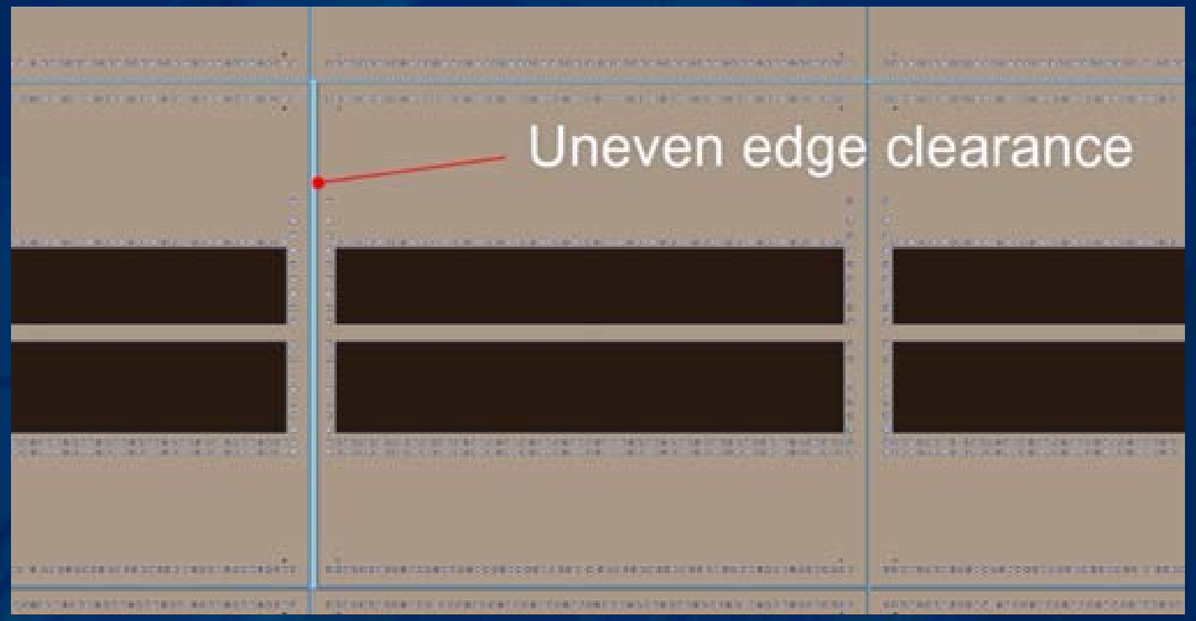


HBM chips are tested at the wafer level and shipped out without the final testing, increasing the risk of the final product being “scrapped”

Current Testing Methods for HBM

Wafer Level Probing

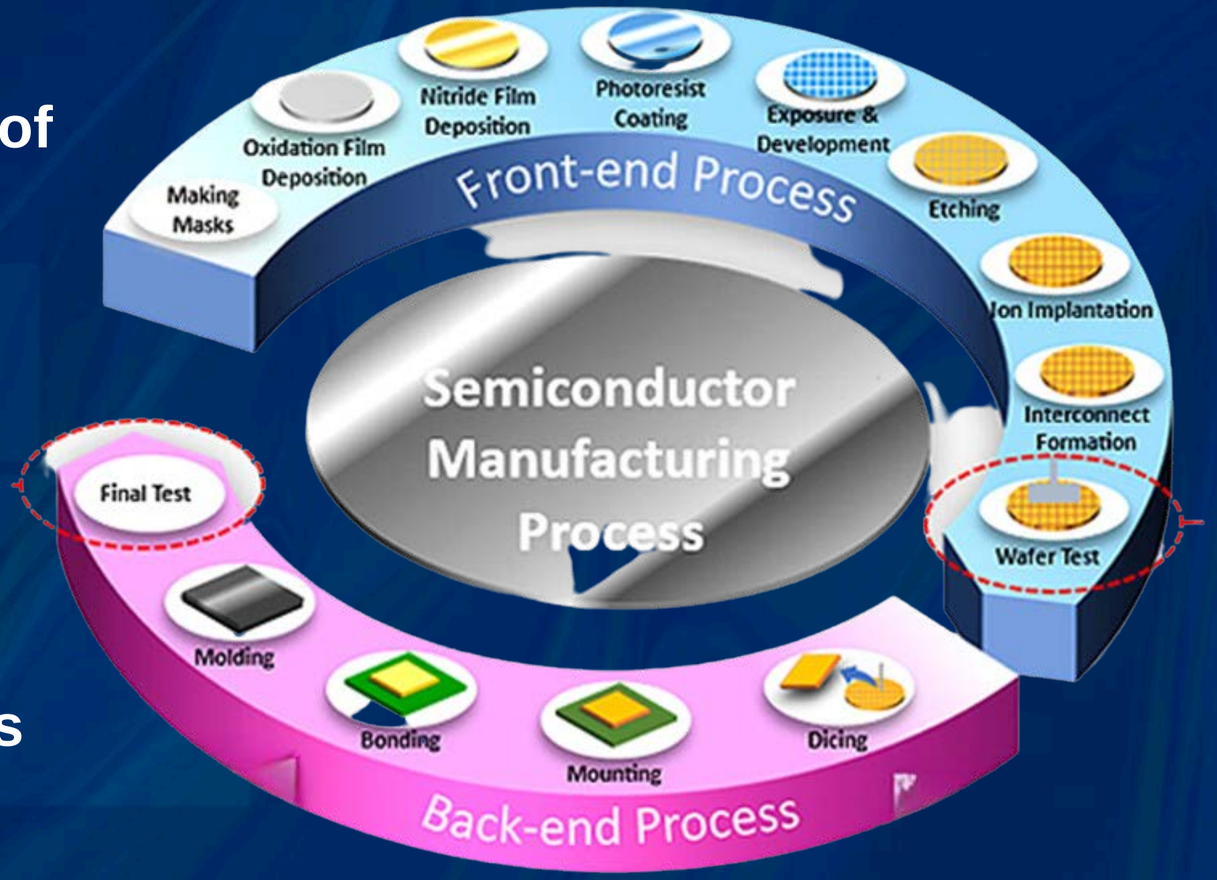




- **Sawing generated dust**
- **Cutting position errors**

Importance of Die Level Testing

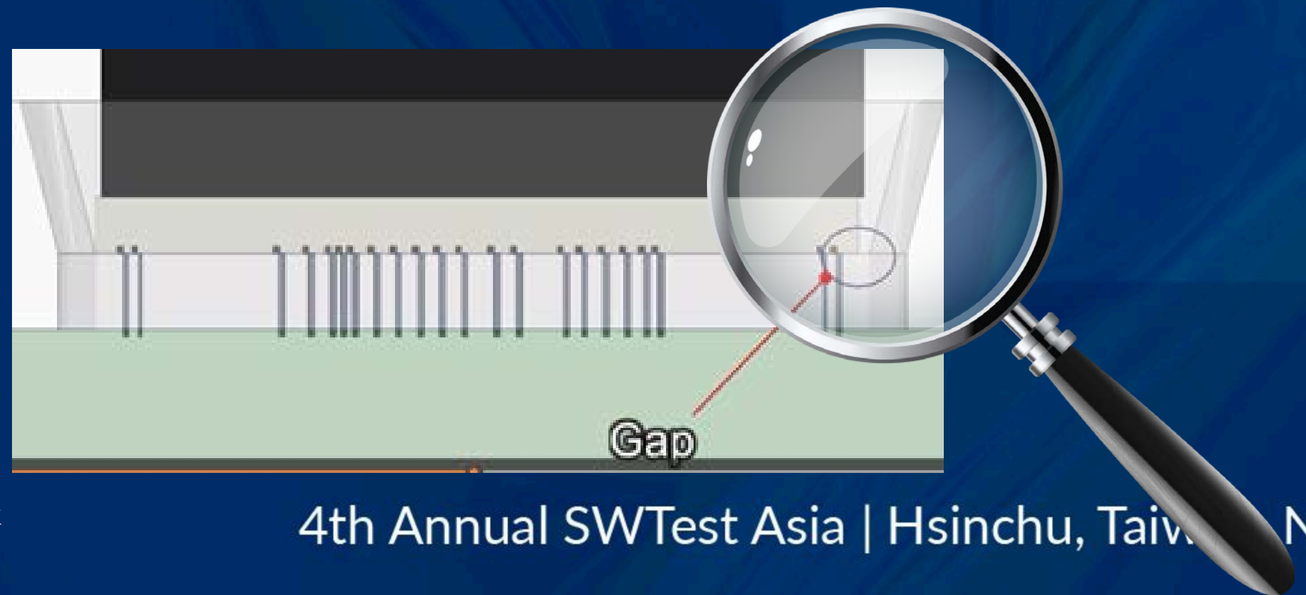
Robust KGSD testing safeguards the quality of semiconductor devices prior to packaging



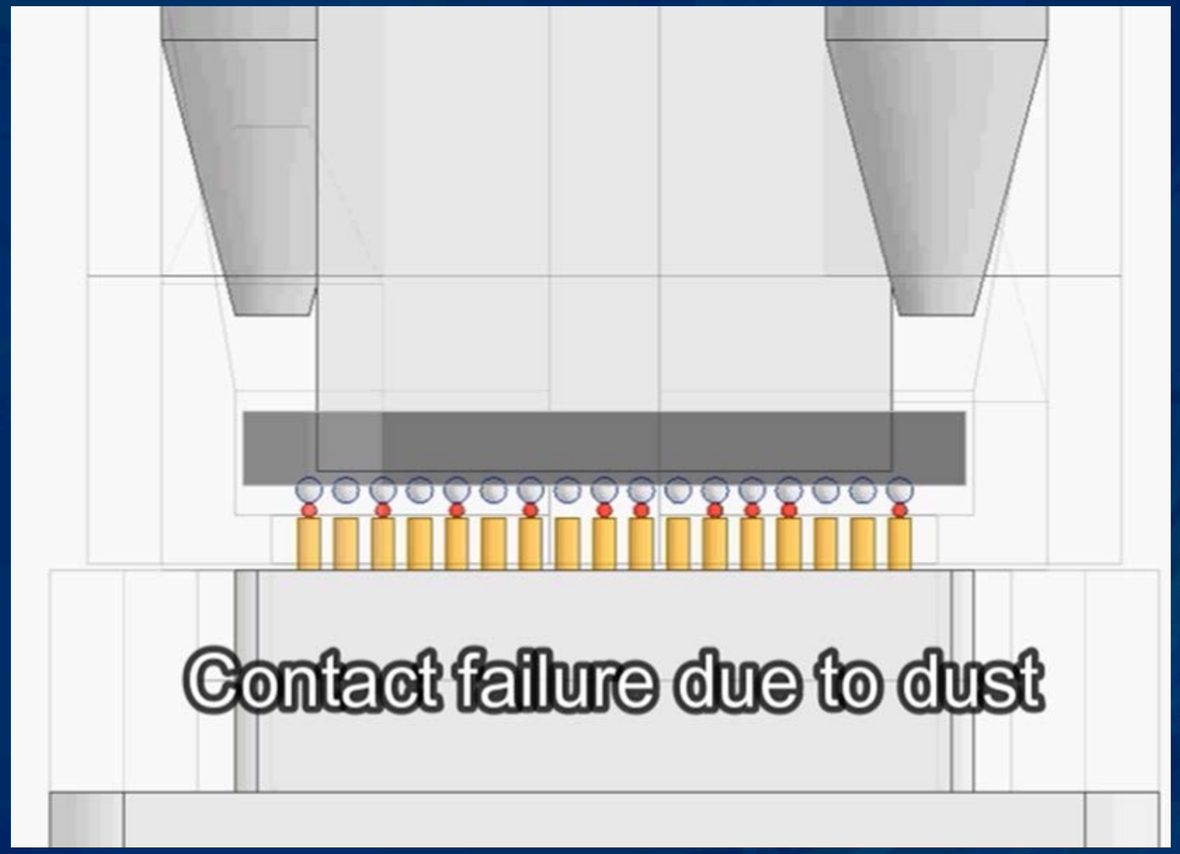
Post wafer sawing testing at die level ensures chip integrity, reduces rework, & minizes scraps

Challenges in Testing HBMs @ Die Level
Alignment Problem

- Testing requires test probes contacting I/O pins of the chips
- The small pitch between the bumps in HBM chips present a challenge for testing:
  - difficult access to individual bumps for testing
  - increases the risk of crosstalk or interference between signals.



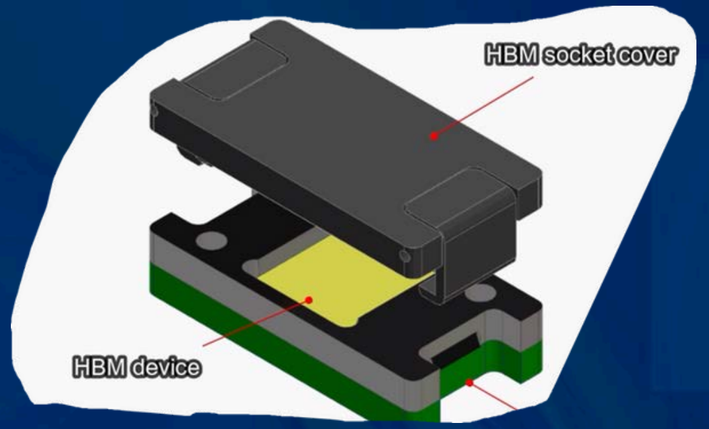
Challenges in Testing HBMs @ Die Level
Die Carrier Assisted Testing

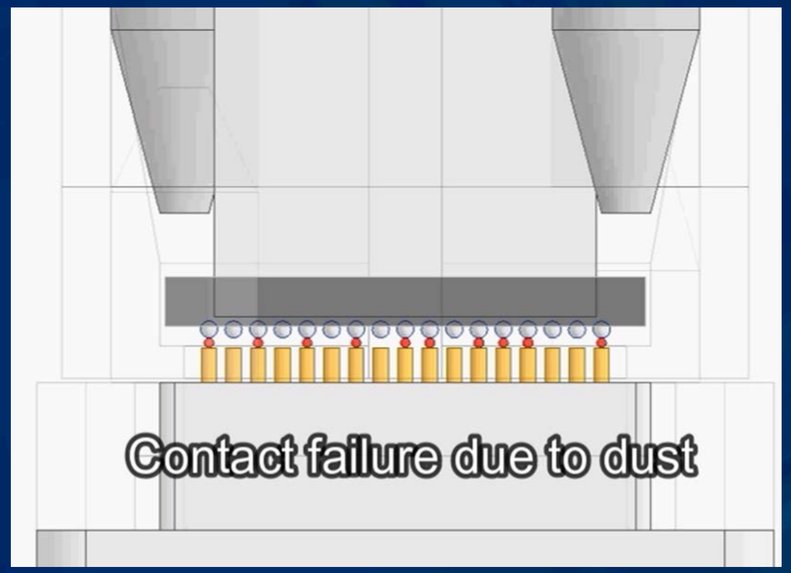


- Tri-temperature and electrical testing should be done after chip is “singulated” (i.e., cut from the wafer)
- The only alternative method of testing 3D chips at the die level is using a die-carrier, plastic housing for the chips
- Hot or Cold testing is difficult b/c die-carriers are heated or cooled in a temperature chamber- invariably introduces dust

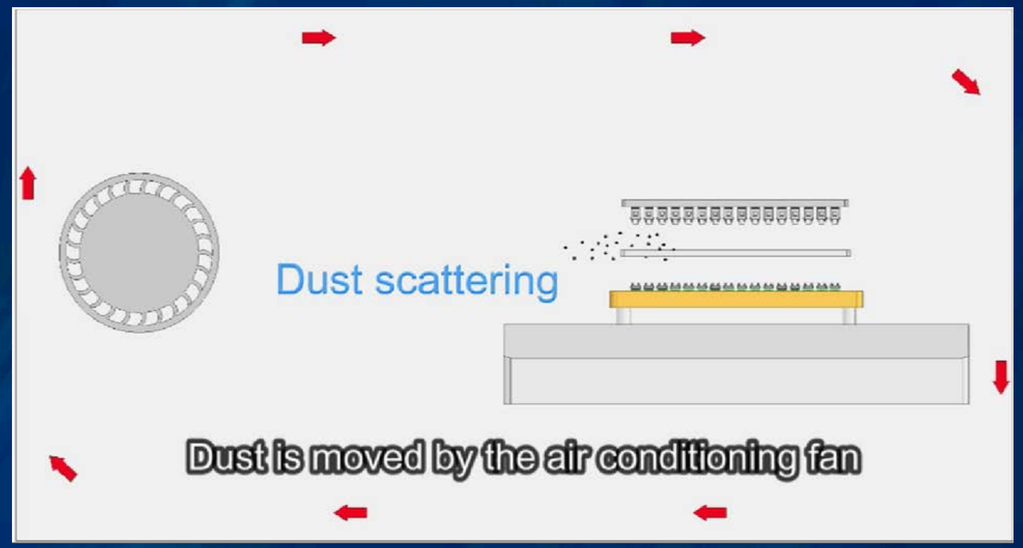
Challenges in Testing HBMs @ Die Level

Die Carrier Assisted Testing





Heating or Cooling Chamber



Hot or Cold testing is difficult b/c die-carriers are heated or cooled in a temperature chamber

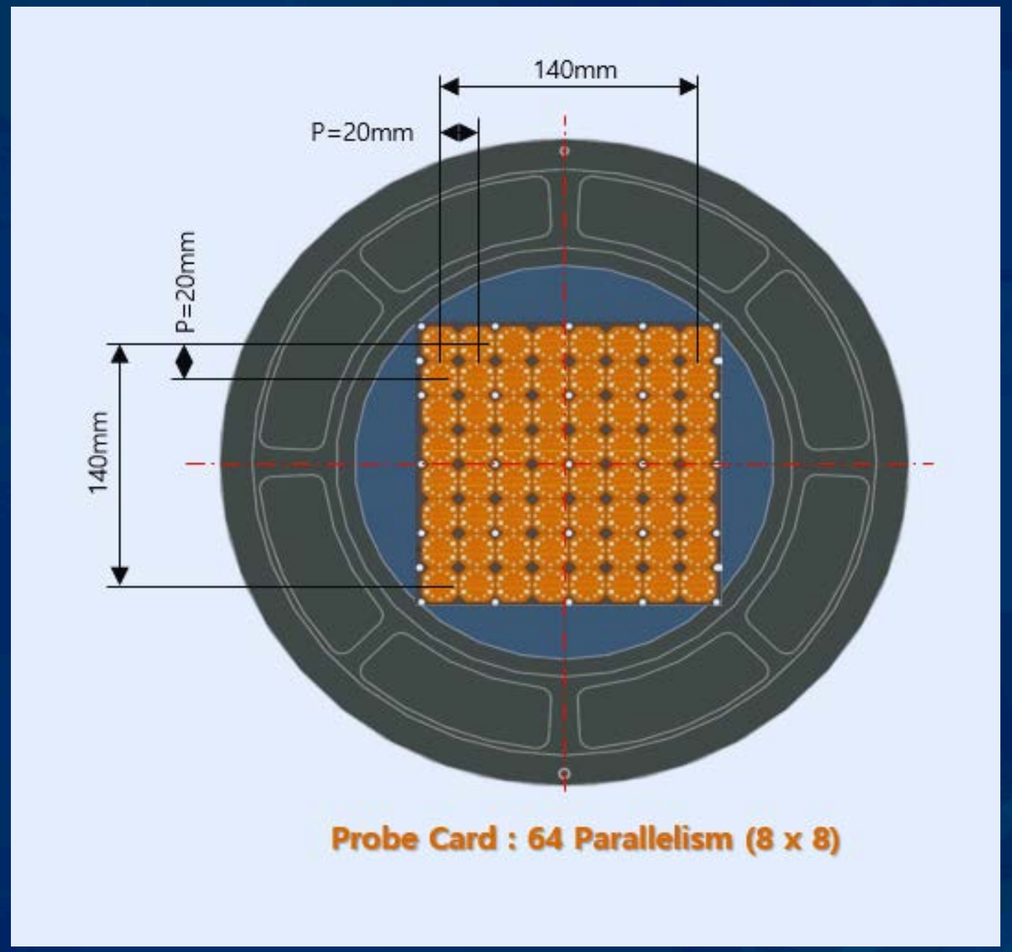
HOW TO PERFORM DIE LEVEL TEST FOR HBMs

Precision Engineering!

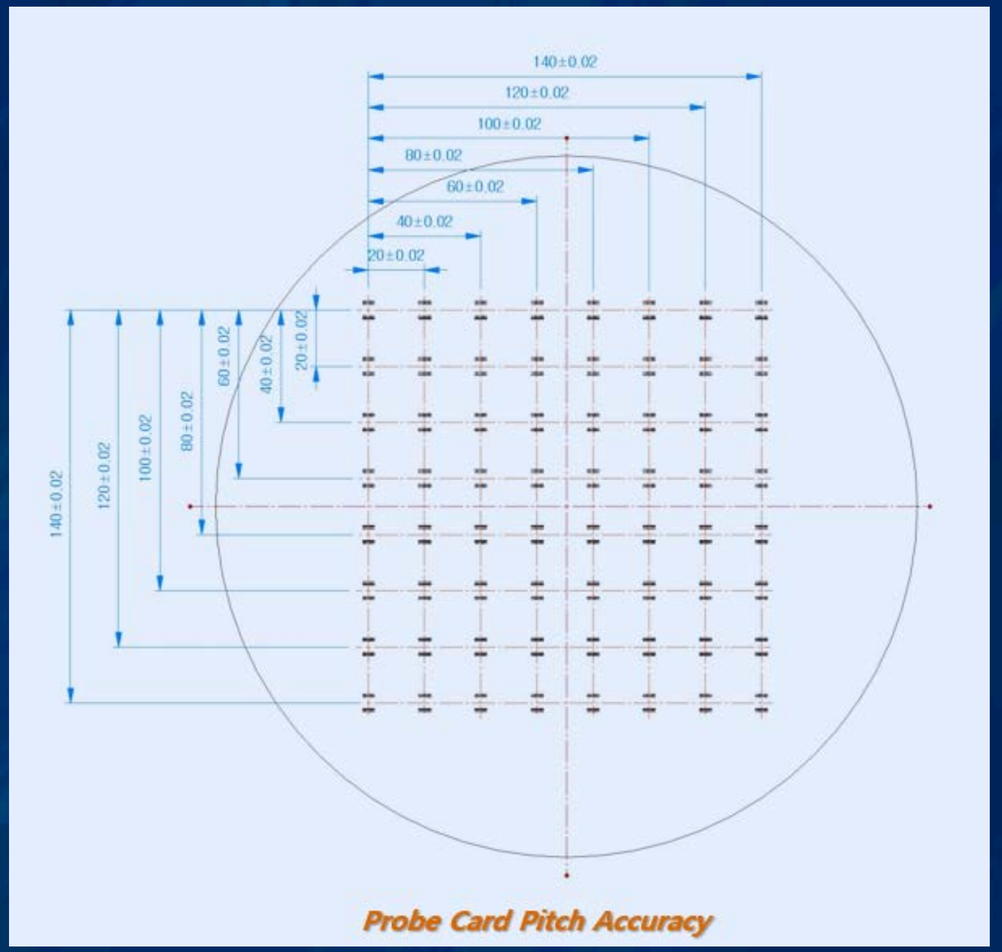
Ultra-Fine Alignment Accuracy

- **Fine Alignment: Precision probe positioning for the finest pitch size: +/- 5 micron alignment accuracy**
- **Thermal Control: Test temperature range of -45˚ C to 145˚ C**
- **High Parallelism: 64 parallel testing**
- **Versatile Device Type: HBM, BGA, WLCSP, MCP**
- **Compatibility with Existing Test Systems**

AMT5000 DESIGN CONSIDERATION & PARAMETERS

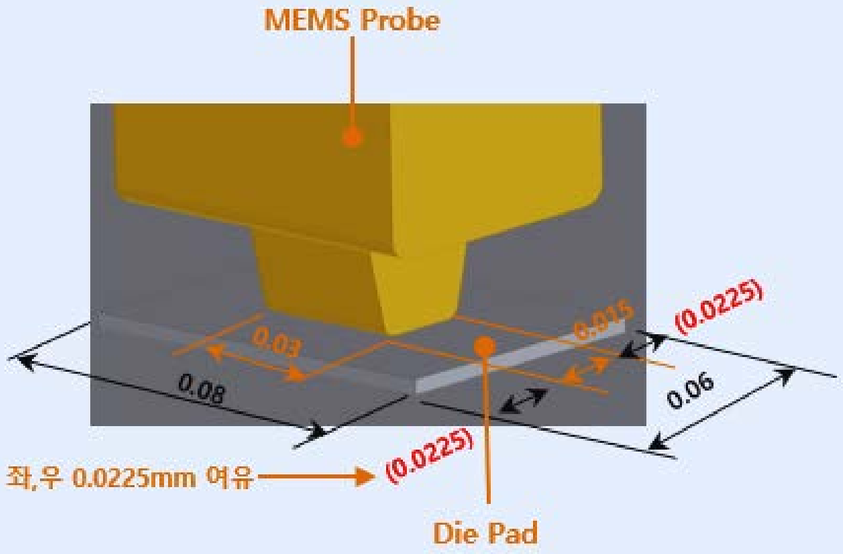


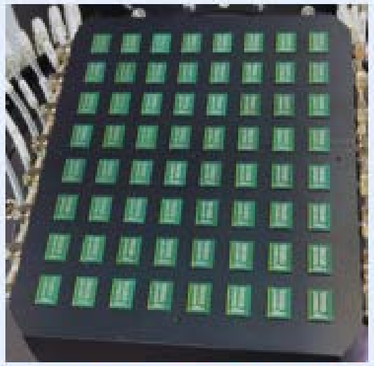
Probe Card : 64 Parallelism (8 x 8)



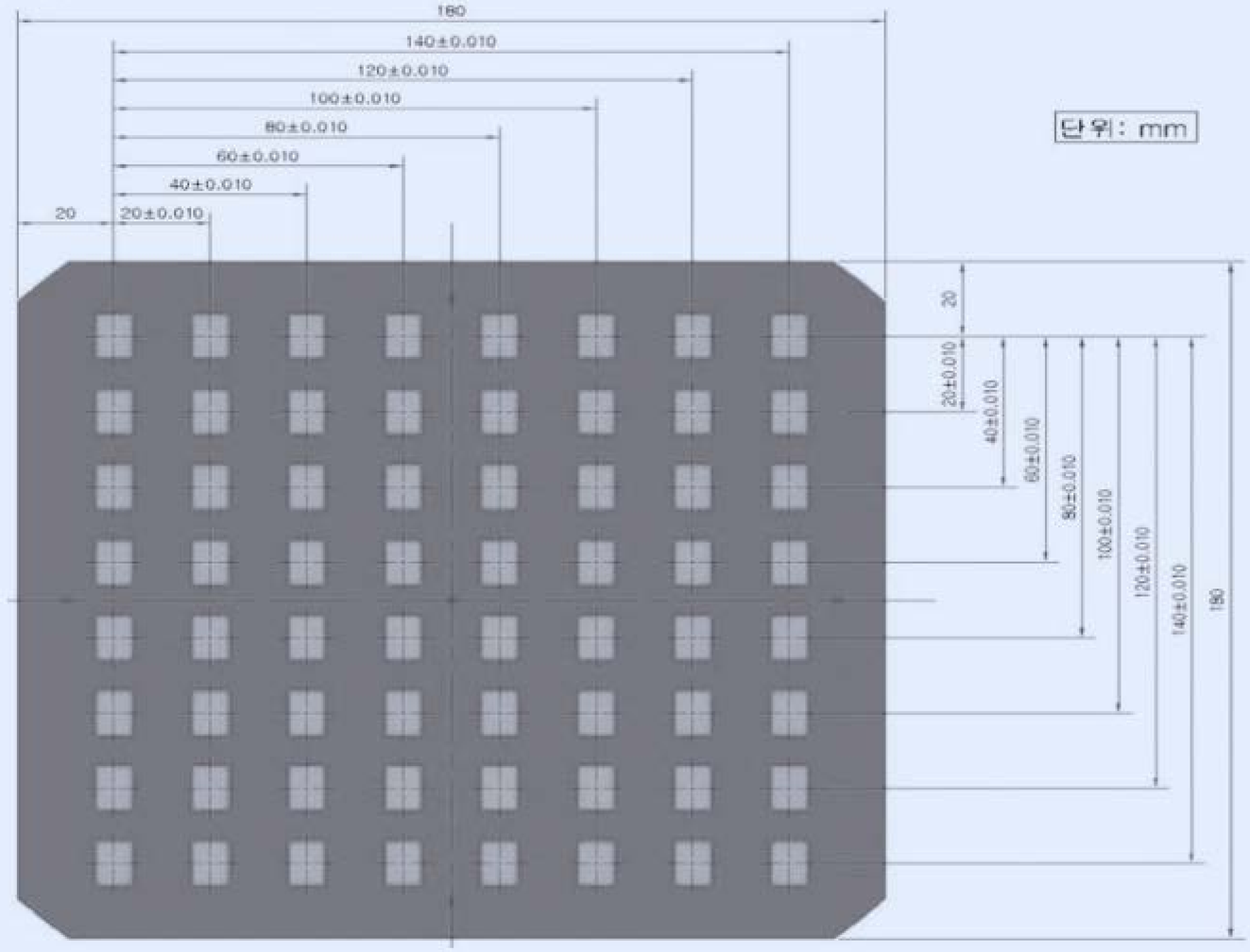
Probe Card Pitch Accuracy

AMT5000 DESIGN CONSIDERATION & PARAMETERS





Chuck Para : 64Para (8 x 8)

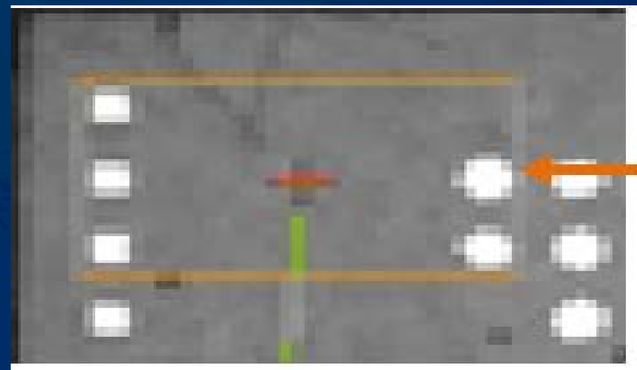


Die Alignment Accuracy

AMT 5000 DIE ALIGNMENT PRECISION MEASUREMENT METHOD

Reference Registatration	*Align the ball array of the initial material parallel to the centerline of the camera and register the upper-left and lower-left corners of the material as references for the pattern.*
Device Alignment	*Move the stage to each die position, conduct vision inspection, and compare the result data with the reference data to adjust the die position.* *Repeat this process to align all 64 dies.*
Measurement of Die Alignment	*Sequentially inspect all 64 dies using vision starting from the first material to calculate the positional error values compared to the reference data.*

AMT 5000 DIE ALIGNMENT PRECISION MEASUREMENT METHOD



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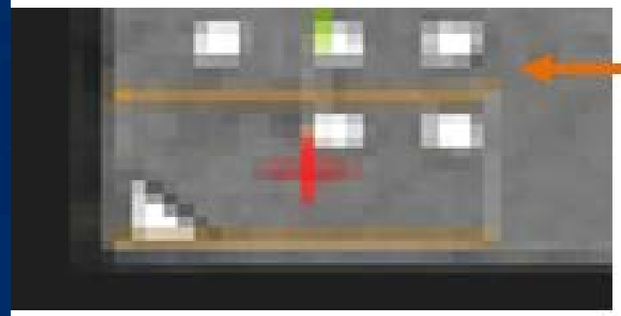

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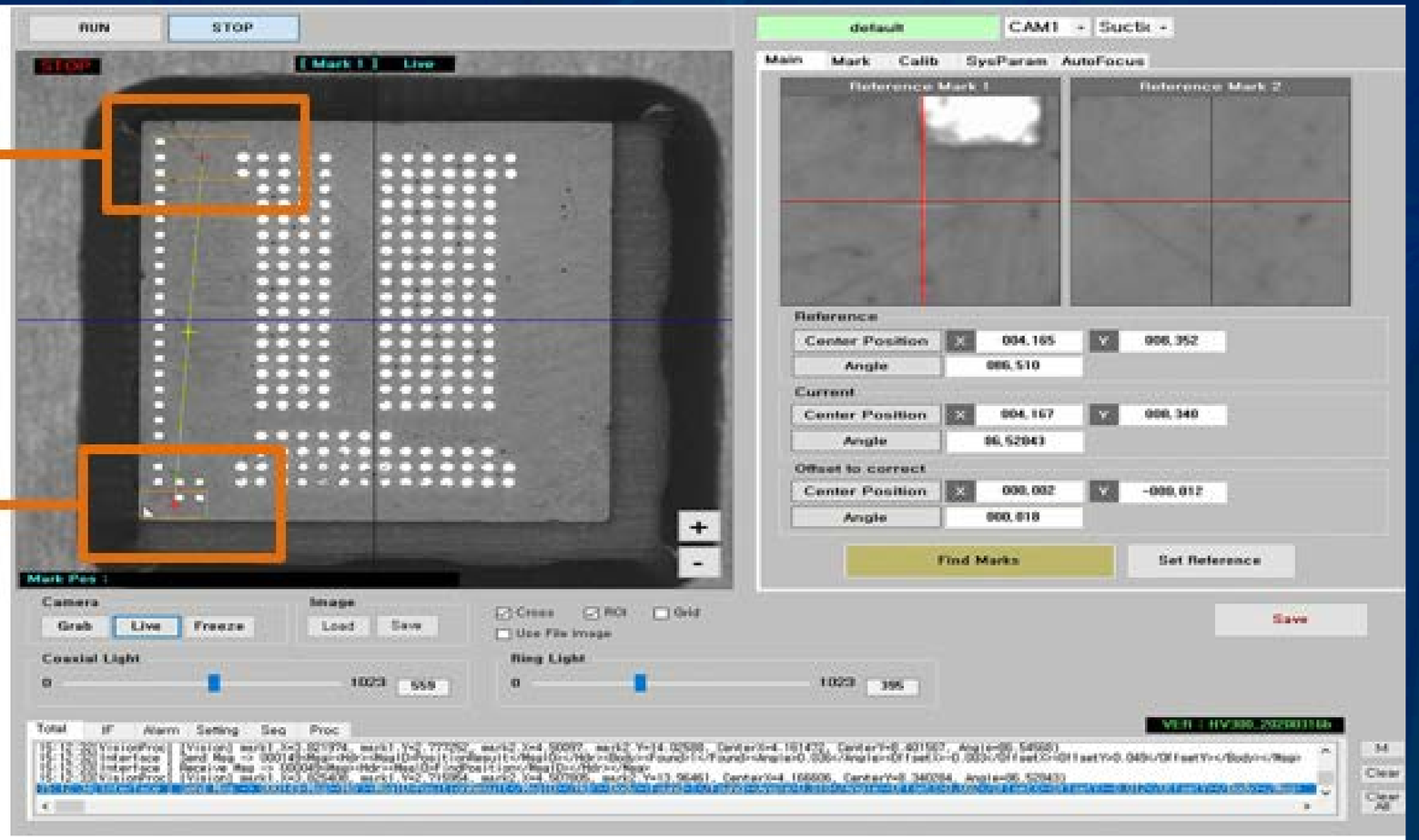


AMT 5000 DIE ALIGNMENT PRECISION TEST RESULTS

▶ [illegible] Alignment for Each Dual Stage Chip Alignment 64 Chips Completed, Position Value Measured with Vision (May 25, 2022)

▶ Chip Alignment Accuracy : ± 5㎛ (Head Base)

(Unit : mm)

Left Chuck	1		2		3		4		5		6		7		8	
	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
1	0.003	0.000	0.003	-0.002	0.003	0.003	0.002	0.000	0.002	0.003	0.002	0.002	0.002	0.002	-0.003	0.003
2	0.005	0.002	0.005	0.002	0.002	0.003	0.003	0.000	0.002	0.002	0.002	0.002	0.000	0.002	0.000	0.000
3	0.005	0.002	0.003	0.005	0.002	0.000	0.005	-0.002	0.003	0.002	-0.002	0.003	0.005	0.002	0.002	0.002
4	0.000	0.002	0.002	0.003	0.003	0.002	0.005	0.003	0.003	0.002	0.002	0.003	0.002	0.003	-0.002	0.002
5	0.005	0.002	0.003	0.003	0.003	0.002	0.002	0.002	0.003	0.002	0.005	0.003	0.002	0.003	0.000	0.005
6	0.003	0.002	0.005	0.002	0.005	0.005	0.003	0.000	0.007	-0.002	0.002	0.005	0.005	0.002	0.002	0.003
7	0.005	0.005	0.002	0.003	0.000	0.002	0.002	0.000	0.005	0.003	0.002	0.002	0.003	0.000	0.000	0.000
8	0.002	0.003	0.002	0.003	-0.002	0.002	0.005	0.003	0.000	0.003	0.003	0.000	-0.002	0.002	0.003	0.000

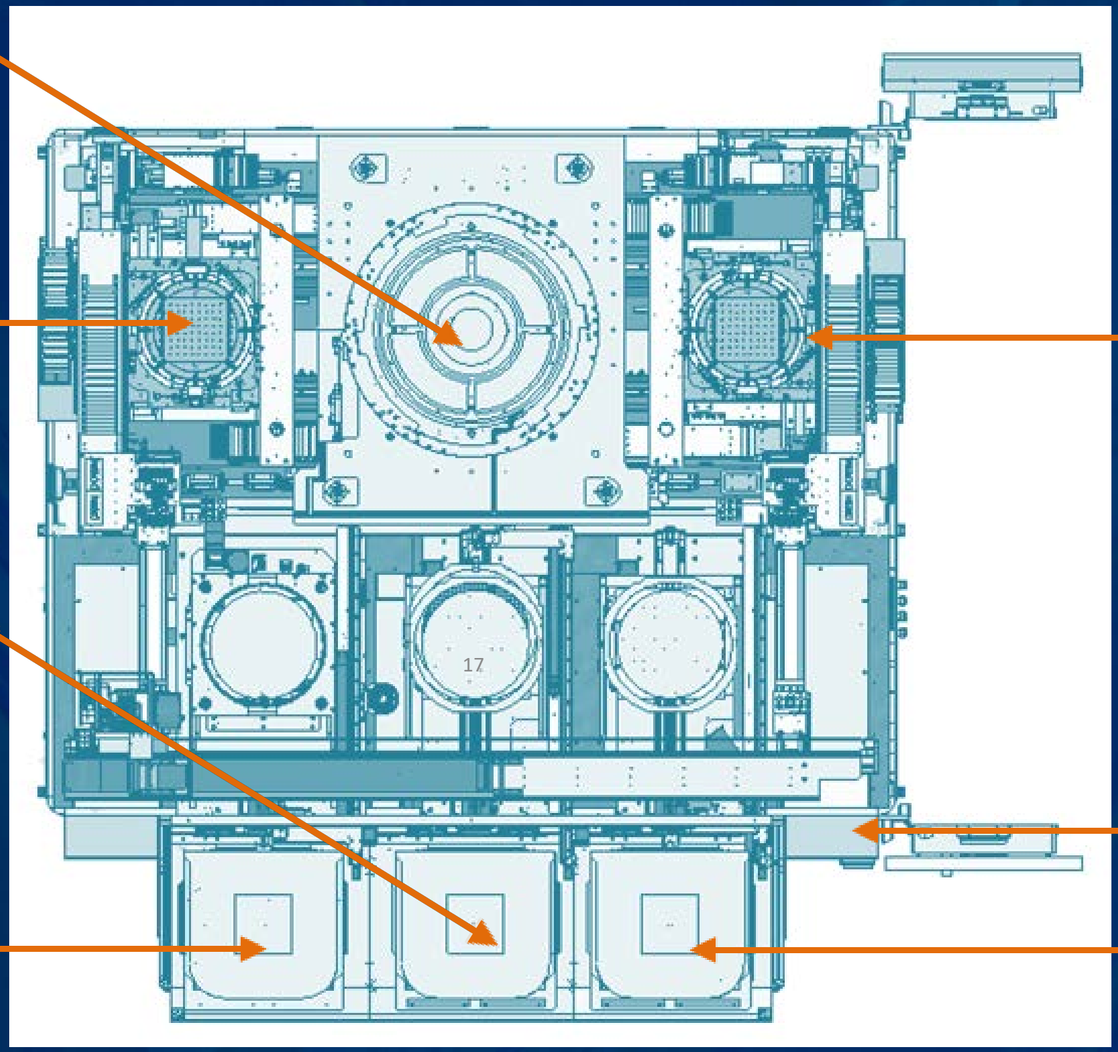
※ Measurement : X= -0.002 ~ +0.005 Y= -0.002 ~ +0.005

(Unit : mm)

Right Chuck	1		2		3		4		5		6		7		8	
	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
1	0.003	0.000	0.002	0.000	0.003	0.005	0.005	0.003	0.003	0.000	0.002	0.002	0.000	0.005	0.000	0.003
2	0.003	0.002	-0.002	0.005	-0.002	-0.002	0.003	-0.002	0.005	0.005	0.002	0.003	0.007	-0.002	0.005	-0.005
3	0.002	0.000	-0.002	0.000	0.007	-0.005	-0.003	-0.002	0.000	0.003	-0.002	-0.003	0.003	0.002	0.002	0.002
4	0.007	0.005	0.003	-0.002	0.005	0.000	0.007	0.003	0.003	0.000	-0.002	0.005	0.005	0.000	0.000	-0.002
5	0.007	0.005	0.005	0.000	0.002	-0.003	0.005	0.000	0.002	0.003	0.003	0.000	0.007	0.000	0.007	-0.002
6	0.003	0.003	0.000	-0.002	0.002	0.000	0.005	0.000	0.005	-0.003	0.007	0.000	0.003	0.002	0.003	0.003
7	0.003	0.002	0.002	0.002	0.003	-0.002	0.005	0.002	0.005	-0.002	0.003	-0.002	0.002	0.000	0.003	0.002
8	0.003	0.000	0.002	0.002	0.005	-0.003	0.007	-0.003	0.000	0.000	-0.002	-0.002	0.005	-0.002	0.003	0.002

※ Measurement : X= -0.003 ~ +0.005 Y= -0.005 ~ +0.005

AMT 5000 TECHNICAL CAPABILITIES



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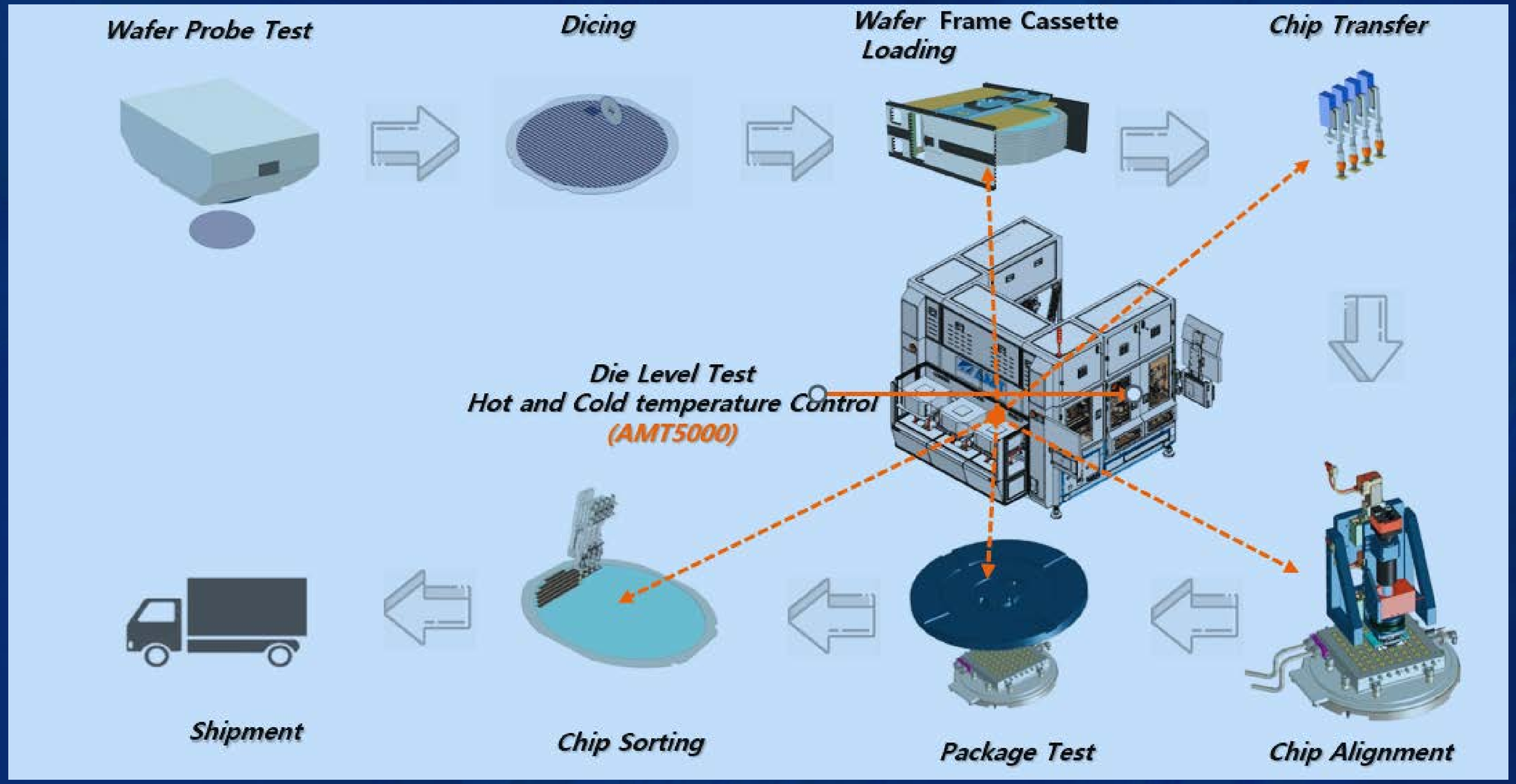

AMT 5000 TECHNICAL CAPABILITIES

	Description	
Test Device	**Device Type**	**HBM**, BGA, CSP, MCP, POP, etc. Device Ball (Pad) Pitch: 120μm or above
UPH(64Para)	**Output**	711ea/Hr. (Index Time: 4Sec) ; Test Time = 320Sec
Loader & Un loader	**Wafer Ring Frame (Cassette or FOUP)**	**AMT5000** Loader One Place, Unloading Two Place (Good, Reject)
	JEDEC Tray (Stacker Type)	**AMT5400**
Test Site	**Probe Station**	Probe Card or Fine Pitch Hi-Fix Board
	Parallelism	64Para, Parallelization Scalable
	Dual Stage (X,Y,Z,θ)	Accuracy =±10μm Repeatability = ±2μm Resolution = 0.1μm Max Speed = 500mm/sec
	Loader /Un loader Picker (X,Y,Z)	Accuracy = ± 20μm Cycle Time = 1.2 sec Pick & Place Load = 1N ~ 2N 1 Head 4 Picker
	Chip Align & Vision (X,Y,Z,θ)	Accuracy = ± 0.5μm Alignment Tact Time = 320 sec/64para Chip Alignment Accuracy = ±5μm (Pad) Vision : Chip Align
	Hot & Cold Chuck (Dual)	-45℃~+145℃ (±1℃)

More about AMT solutions can be seen here:

AMT HBM Test Handler™

- https://www.youtube.com/watch?v=hrxTY8dsUSE&t=20s
- https://www.youtube.com/watch?v=-CG8Am9uSJI
- https://www.donga.com/en/List/article/all/20230705/4268749/1

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