



# Waveform Considerations on Shared Driver Signals



Micron Memory Japan

# Overview

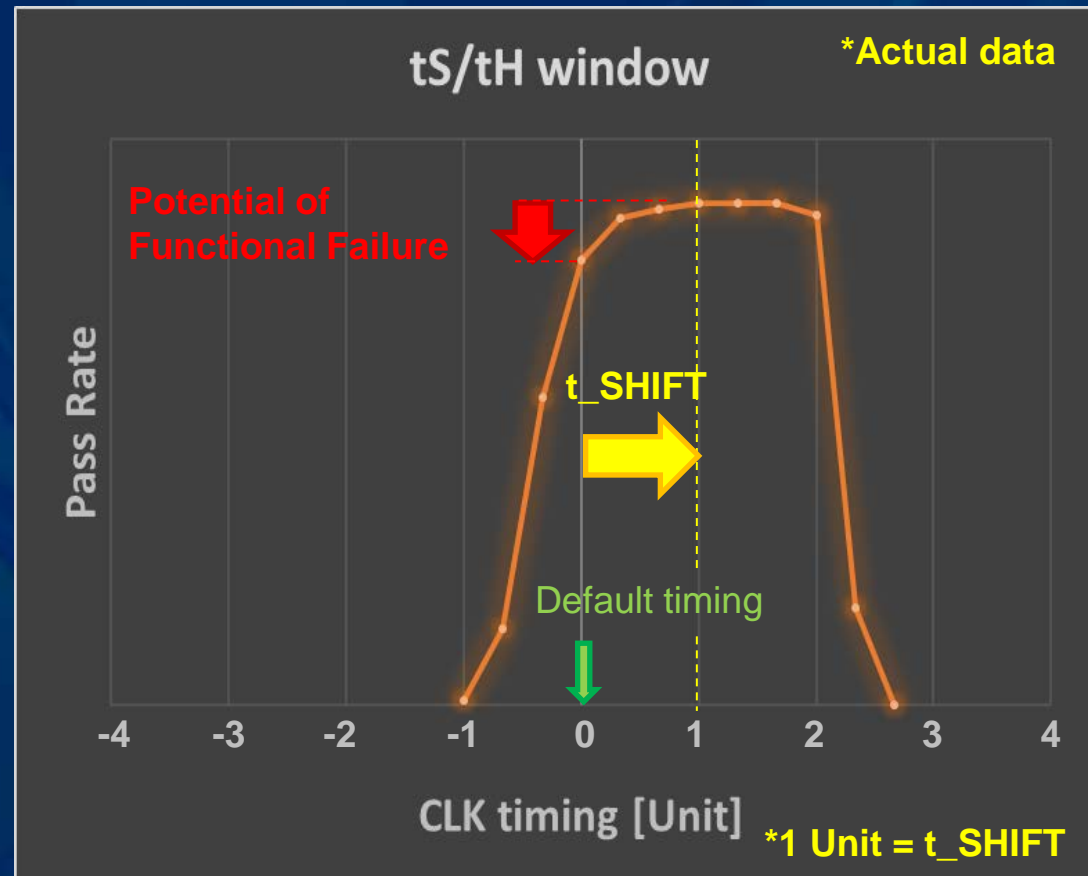
- **Background**
- **Problem statement with real case examples**
- **Waveform simulation**
- **High frequency and KGD**
- **Ask of the industry**
- **Summary**

# Introductory Background

- **Increasing parallelism by driver sharing can reduce test costs.**
- **Limited tester resources require high sharing of driver signals.**
- **Understanding & managing high sharing impacts is challenging.**
- **These challenges will be highlighted in this presentation.**

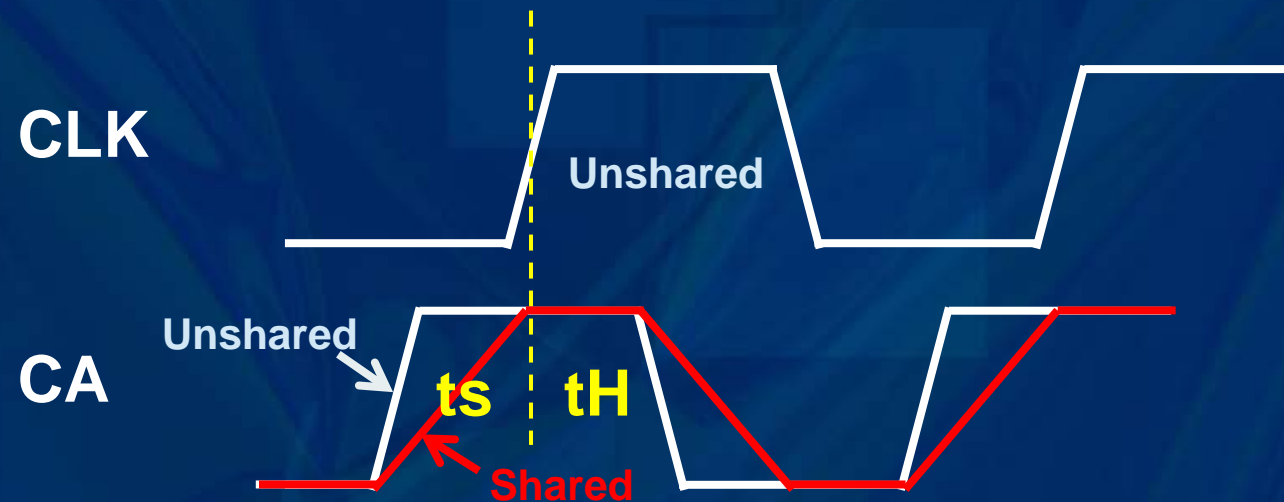
# Problem Statement

- During test program debugging functional failures observed.
  - What caused tS/tH window between CLK vs. CA to shift?



# Combination, Unshared & Shared Driver

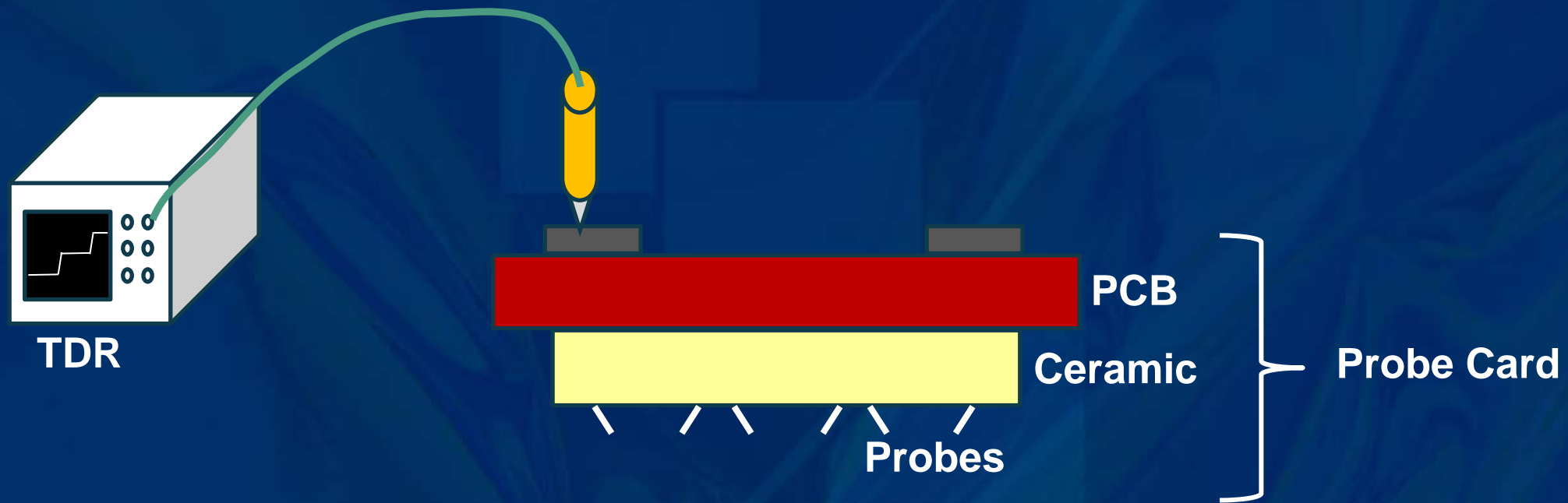
- In this case, both unshared and shared drivers were used. It was known that there was a timing delay between CLK & CA due to slower rise time on the shared CA driver.
  - CLK pin – Unshared
  - CA (Command / Address) pins – Shared



# Compensating for Timing Delays

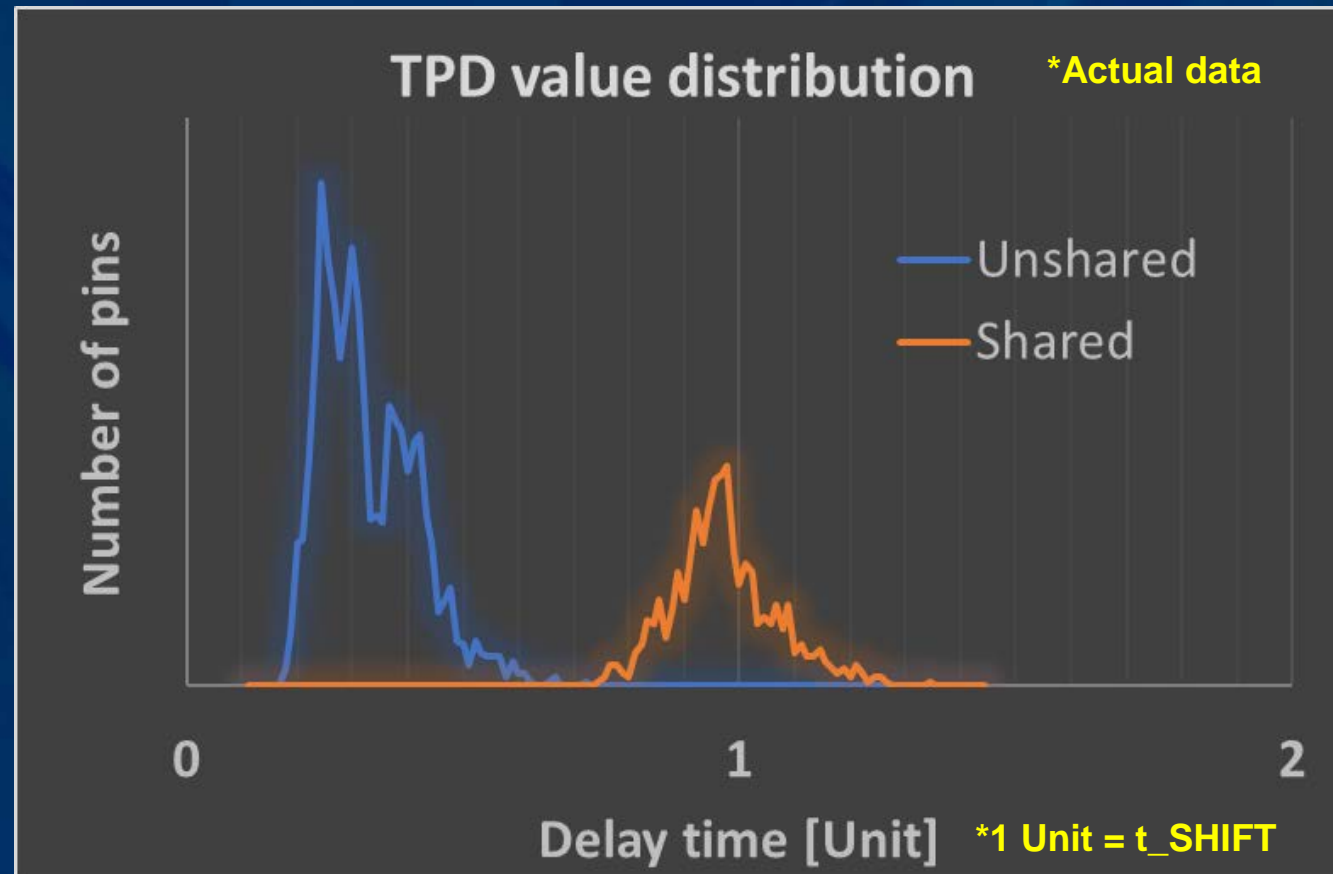
- TPD value by TDR measurement can compensate timing delays.

\*TPD : Time Propagation Delay



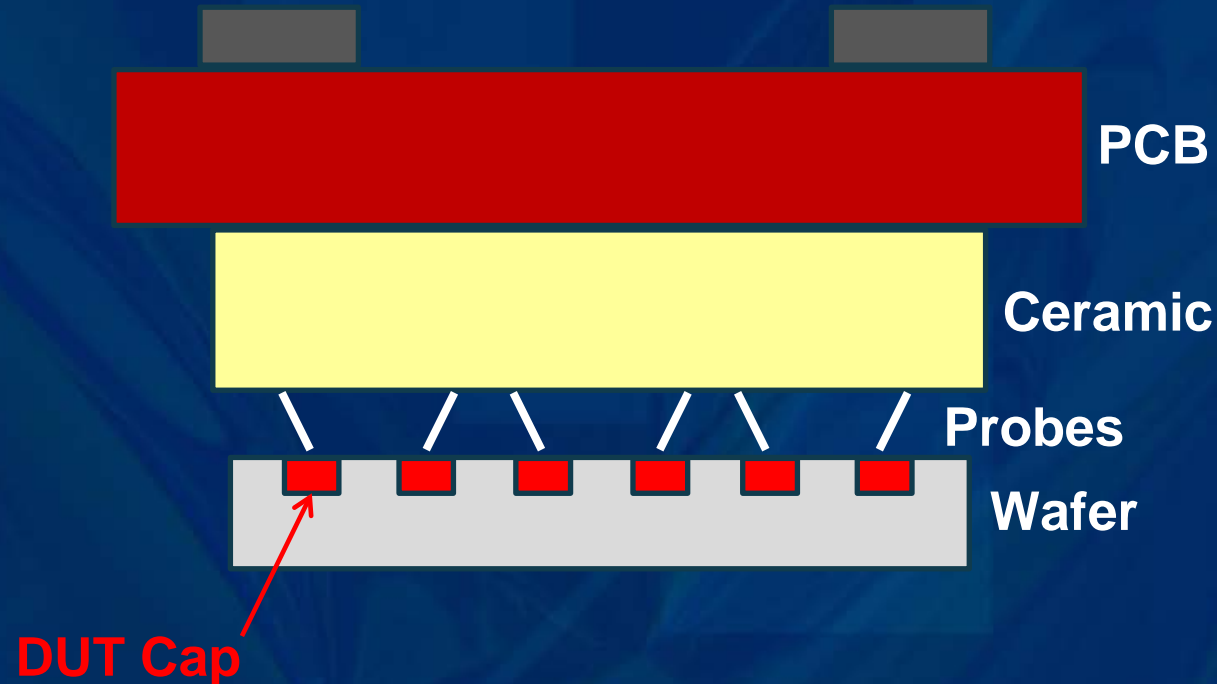
# Distribution of Measured TPD Value

- TPD values were implemented, functional fail still occurred.
  - Any other parameters missed in design?



# Missing Parameters

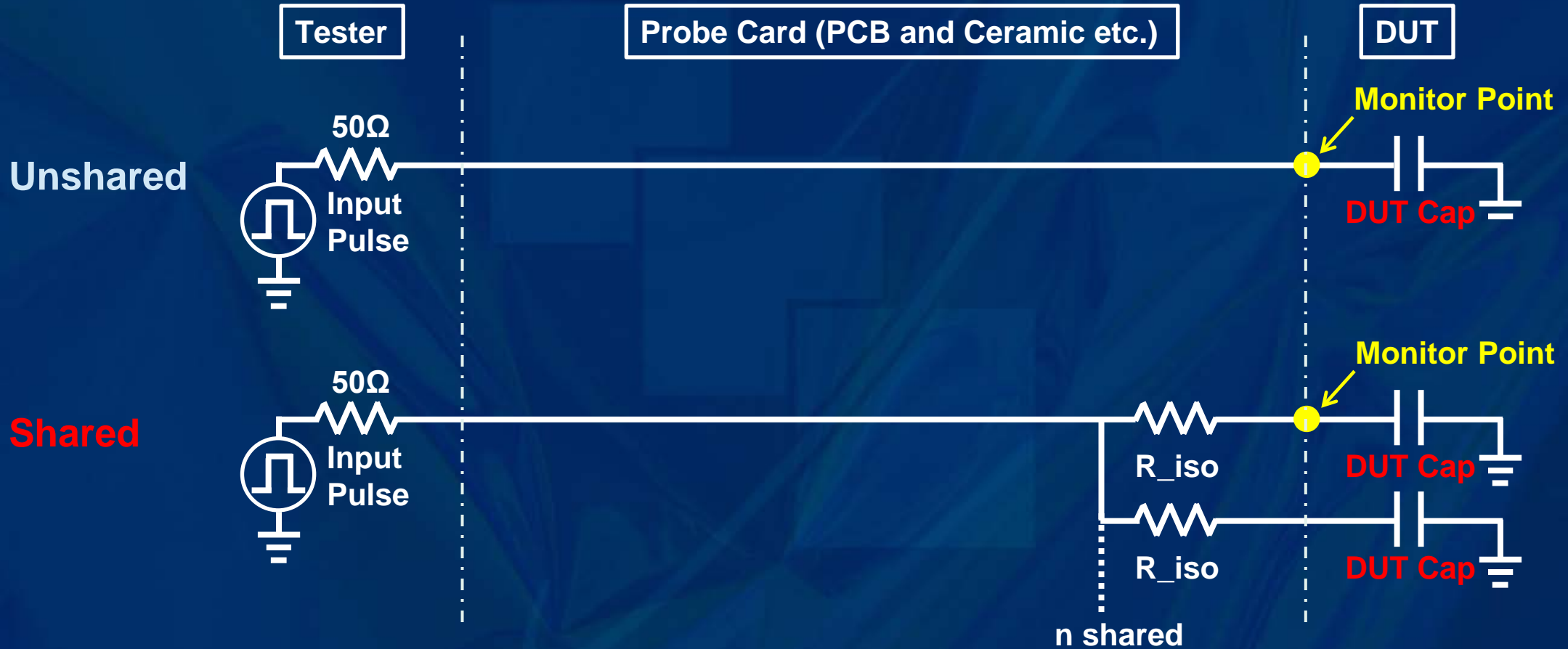
- What if the input capacitor on the device pads were missed?





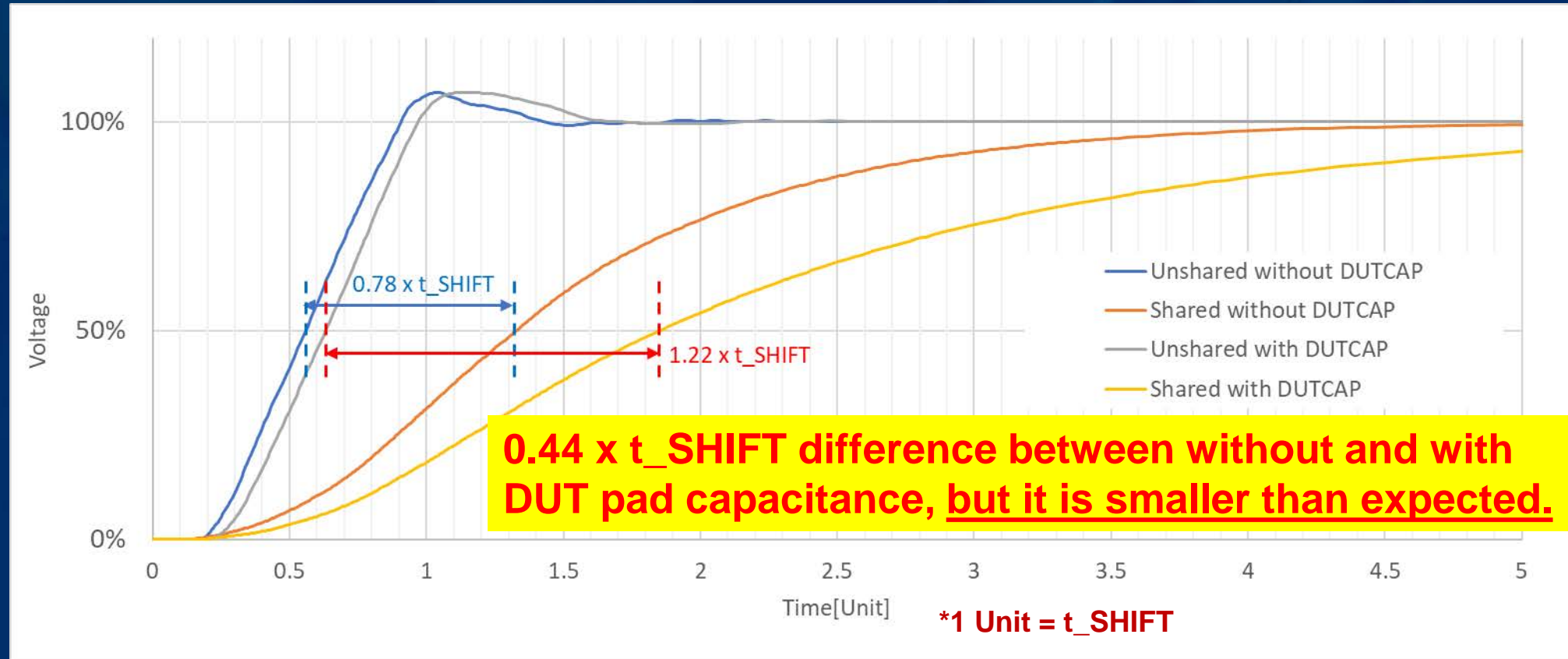
# Waveform simulation (1)

- Simulation model



# Waveform simulation (2)

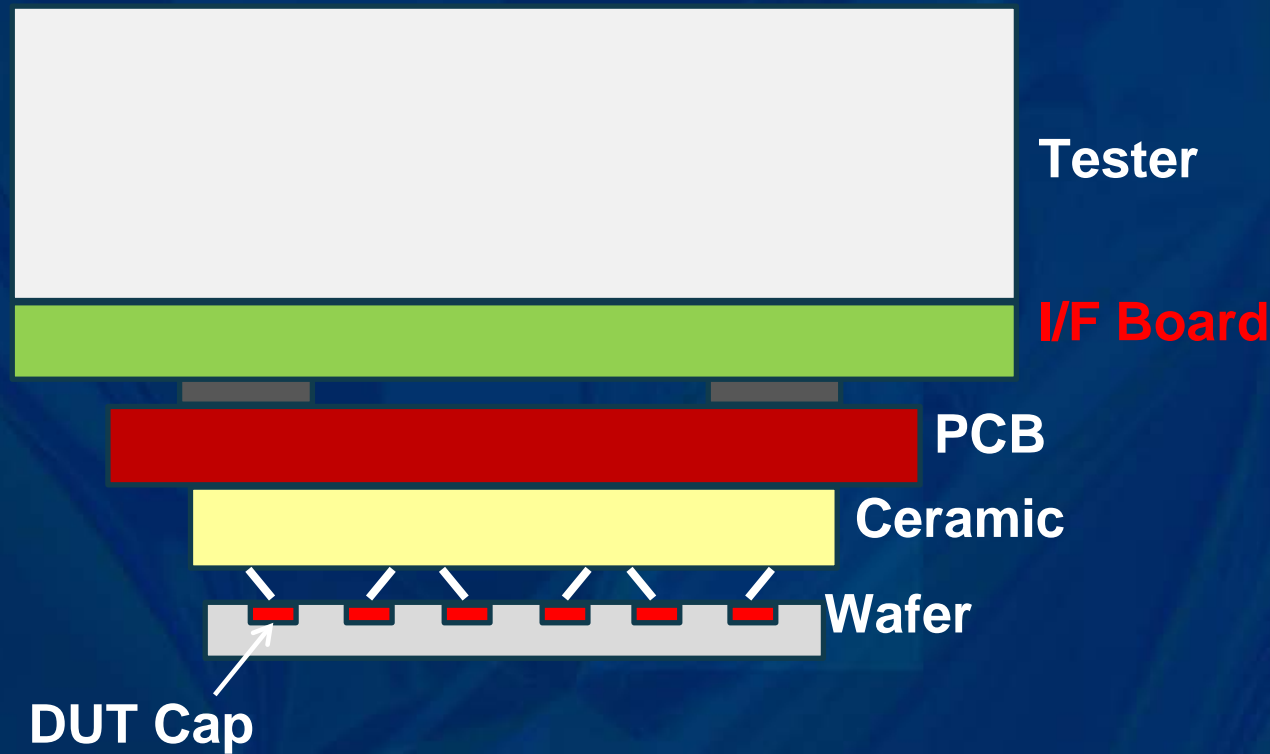
- Difference between without & with DUT pad capacitance



- Other missing parameters?

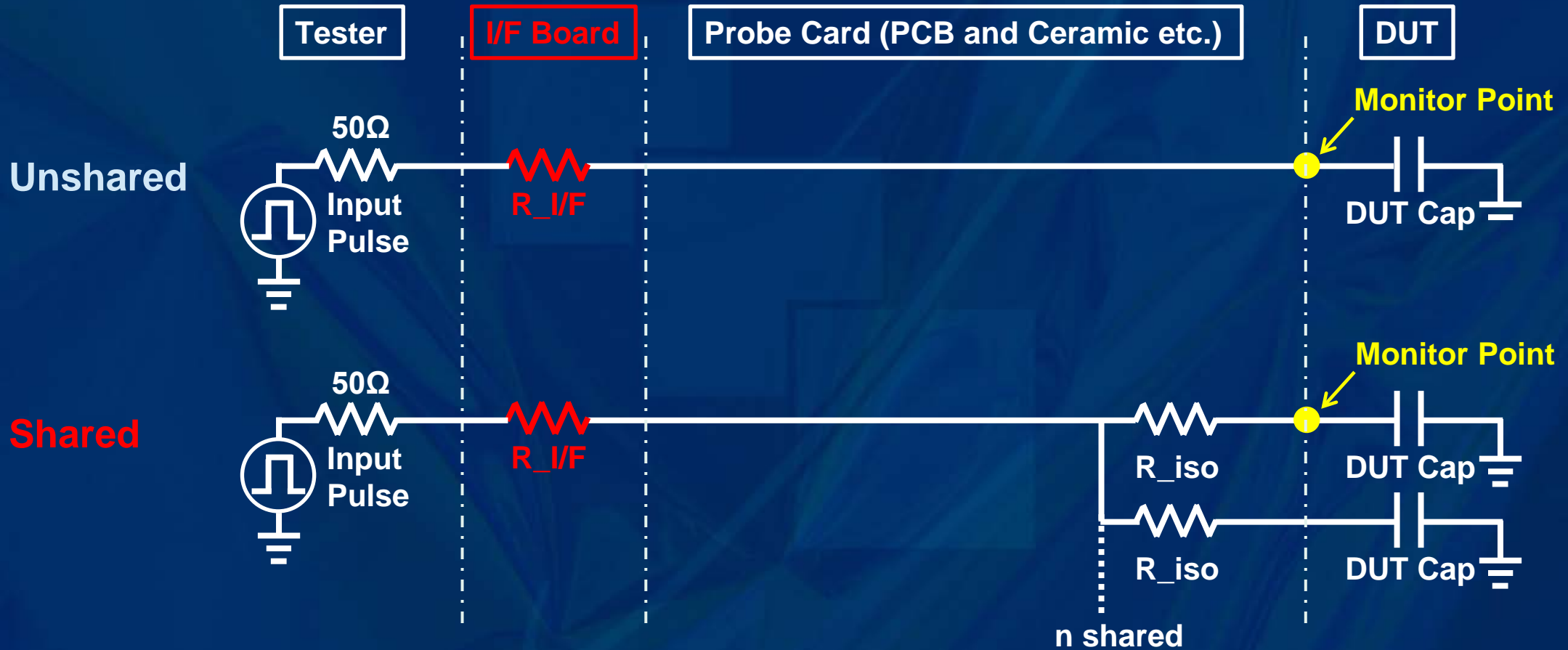
# Another Missed parameter

- What if resistance of the I/F Board was missed in simulations?



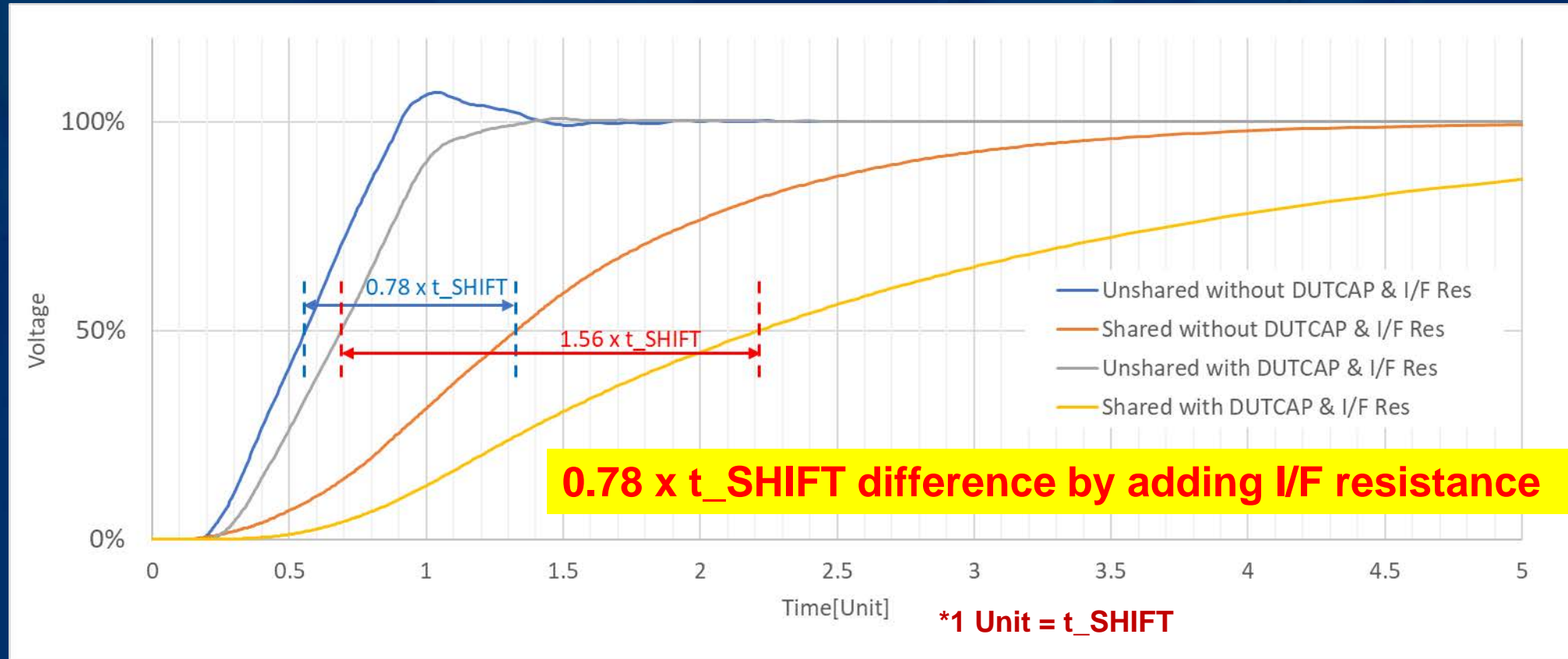
# Waveform simulation (3)

- Simulation model (2)



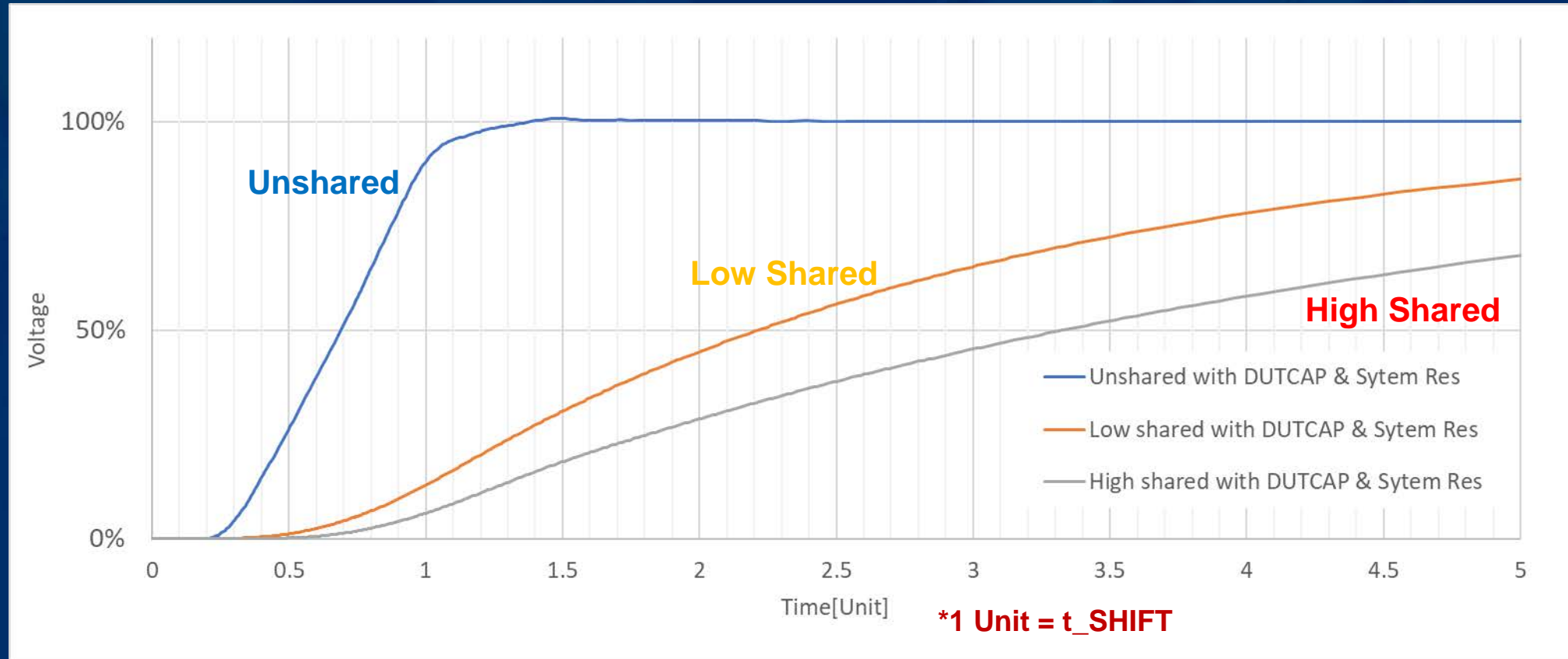
# Waveform simulation (4)

- Adding an additional resistance from the I/F board



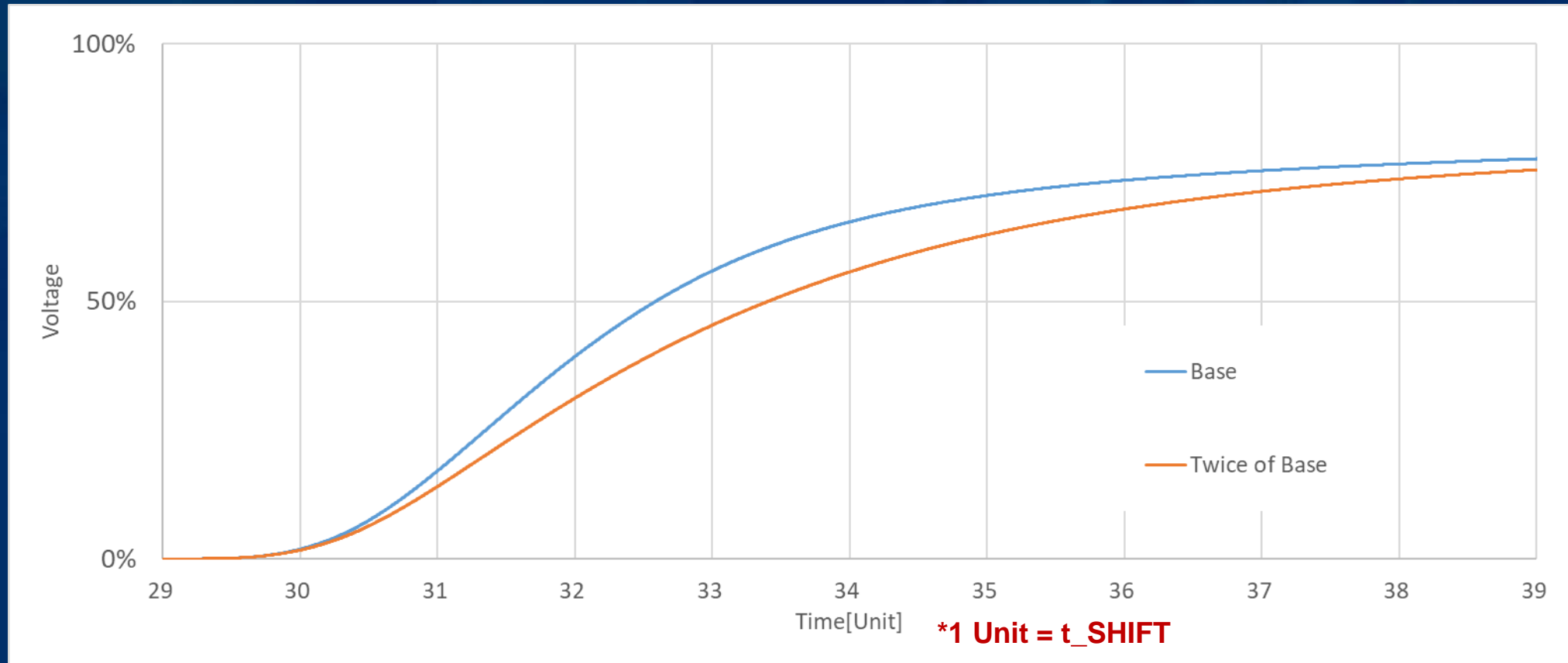
# Waveform simulation (5)

- Dependency on number of shared drivers



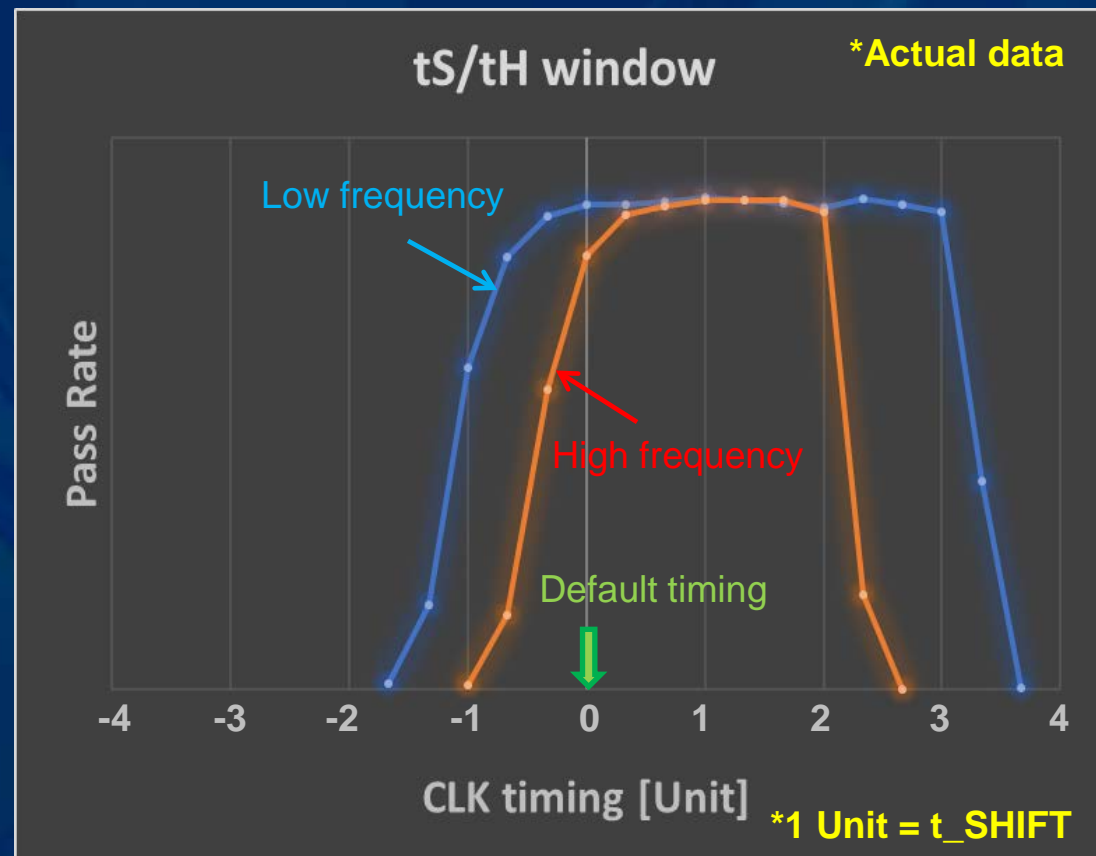
# Waveform simulation (6)

- Changing wiring capacitance on the probe card



# High Frequency Functional Testing

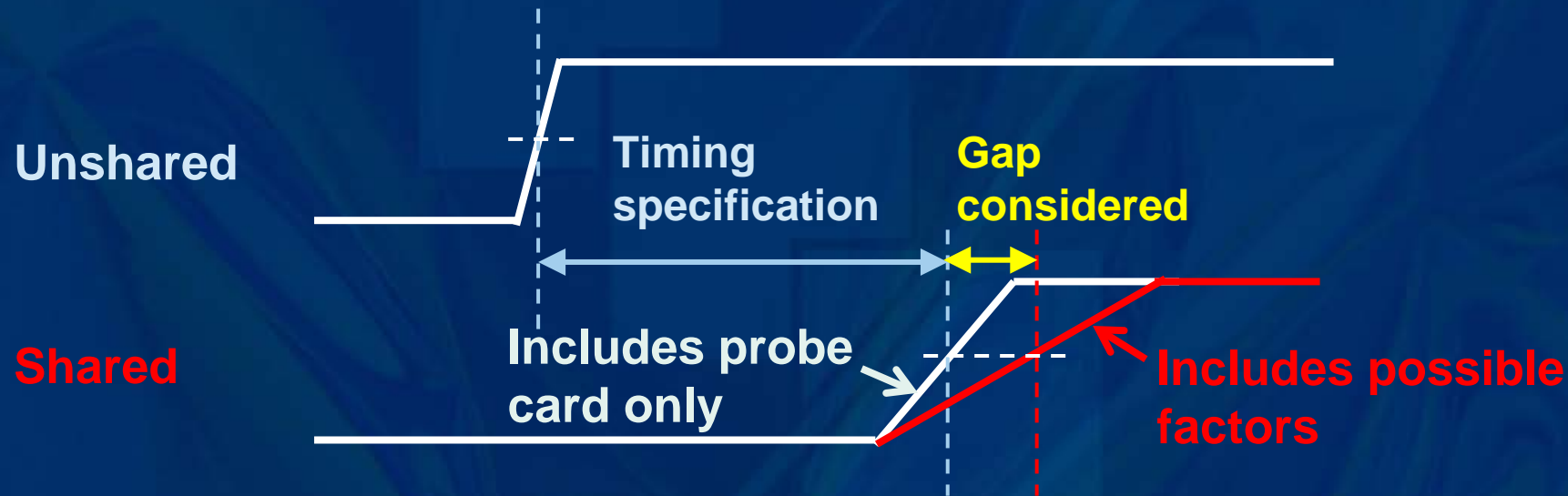
- **High test frequency reduces test time but narrows tS/tH window.**
  - Overcoming shifted tS/tH window (shared & unshared signal).





# Used Case Known Good Die (KGD)

- As KGD timing specification is guaranteed by wafer test, the shared/unshared phenomena must be accounted for during test.



# Ask of Probe Card Industry

- Lowering the value & variation of capacitance & resistance of trace lines helps to keep test conditions equally between Duts.
- Micron is asking Probe Card supplies to help in this area

$$\tau = (R_{\text{CARD}} + R_{\text{ISO}} + R_{\text{SYSTEM}}) \times (C_{\text{CARD}} + C_{\text{DUTCAP}} + C_{\text{SYSTEM}})$$

# Summary

- **Factors other than probe card can change a tester's waveform.**
- **Micron considers the whole ATE test cell system during design.**
- **Probe Card trace to trace difference in capacitance, resistance, shared & unshared is an area for Probe Card Suppliers to help.**

# Acknowledgements

- **Special thanks to:**

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