

### Silicon Photonic On-Wafer Test





S.L Tan, W.L Sio CompoundTek Pte Ltd C.L Lou, B.B Lim STAr Technologies, Inc.

### Overview

- About CompoundTek and STAr Technologies
- Need for Silicon Photonics (SiPh) Wafer Test
- Silicon Photonics Wafer Test Solution
  - Prober Layout and DUT Layout
  - Types of Optical Coupling
  - GRnR Results
  - Typical SiPh Test Items
  - Video Demostration
- Summary



### **Our Commitment**



Deliver leading edge Open-Source silicon photonics platform



Accelerate time-to-market



Founded by Industry Experts. "Virtual fab business model" with proprietary technology





**2017** Operations began with patented manufacturing technology running in our fab partner

> 20 Commercial Customers in 9 different countries are served by our cutting-edge SiPh foundry capabilities



>25 International leading Research Institutes/ Universities are a part of our global SiPh ecosystem



**70 provisional filing/know-how in FY20** forms our large IP bank, capabilities are heavily promoted via media/press (22 releases, FY20) for differentiated branding



1st globally embarking on a 8" & 12" agnostic SiPh commercial testing hub

### CompoundTek



### Asia's 1st SiPh Foundry Agnostic Wafer Test Hub. Testing Centre of Excellence Operation

- ▶ Backed by CompoundTek's strategic partnerships with leading industry test equipment players (prober and instruments)
- ≥ 8" and 12" & O and C band ready
- ▶ Ideal for EO components, 400Gbit/s and higher
- State-Of-The-Art equipment (up to 67GHz LCA for e.g)
- Powered by in-House proprietary proven test executives
- Patented software coding with AI, big data analytic, up to 40% throughput improvement vs market benchmark
- ▶ Managed by team with proven track record

### **STAr Technologies Overview**





# SiPh Market Size



### Increase predominantly driven by

- Data Communication such as transceivers,
- Photonics Processing Applications
- Smart Sensors such as LiDar
- Consumer health applications, such as silicon photonics based biosensors in wearables

Source: (1) McKinsey: Imperatives for photonics companies in the next wave of growth (Jan 23)

(2) Yole: Silicon Photonics: To SOI and beyond (Aug 22); Yole: Silicon Photonics 2021 Market Technology report

Author

# SiPh Wafer Test Challenges



High technical complexity required

- Optics Testing unknown to existing OSATs
- Complex hardware/prober design for both Optical & Electrical test.
- High precision alignment of <1um a must, for optical light coupling in/out of Device-under-Test (DUT).
- No cost effective wafer test with edge coupling solution in market
  - Test done at vertical light coupling but actual application is edge coupling, mismatch between test & actual application can limit test coverage

 Recommend for new products to ensure Design for Testability

Special layout

rules and

guidelines

 Enforced during design phase. Designer to layout optical grating and electrical pads according to guidelines to ensure testability

Long test time, high test costs

 Long alignment time needed for optical coupling. Fast and repeatable optical coupling needed to ensure cost effective production testing

7

### **SiPh Wafer Test Solution**





- 8"/12" wafer compatible.
- Vertical Coupling and Edge Coupling fiber array.
  - CompoundTek Edge Coupling fiber array design coupled with STAr's Patented Edge Coupling Alignment SiPh Solution
- Full O-band, C-Band and L-Band.
- Optical/electrical testing/RF Testing
- Suitable for mass volume production & cost-effective testing.

# **STAr SPT System Overview**



#### Objectives

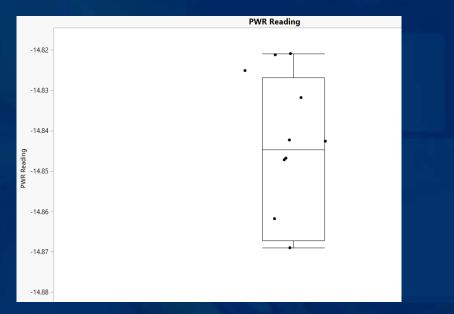
 To provide a cost effective semi-automated or full automation wafer-level test system for characterization and acceptance tests of silicon-photonics devices

### **System Capabilities**

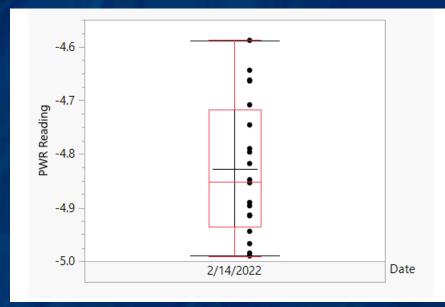
- Characterization & Technology Development
- WAT/E-tests/Inline PCM
  - All E-tests parameters including process monitor control, device parameter test, statistical process control, etc.
  - Optical components for process control and monitor

# **Optical Coupling GRnR Results**

#### Vertical Coupling GR&R



#### Edge Coupling GR&R

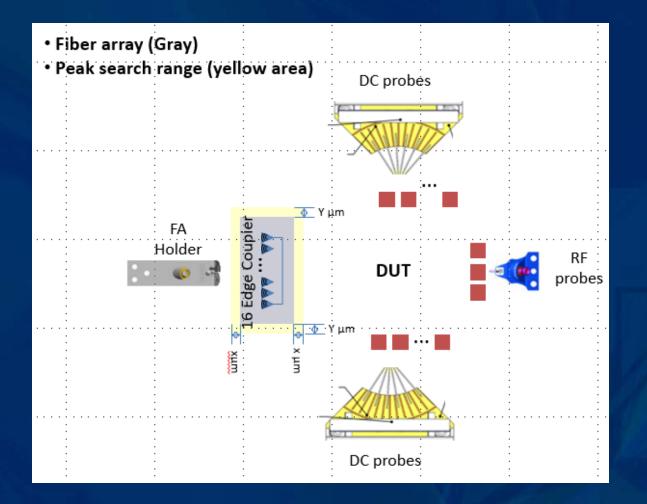


### Vertical Coupling GRnR: 0.06 dBm

### Edge Coupling GRnR: 0.17 dBm

Worse GRnR at edge coupling due to more stringent precision needed for edge coupling compared to vertical coupling

# **Test Configuration**

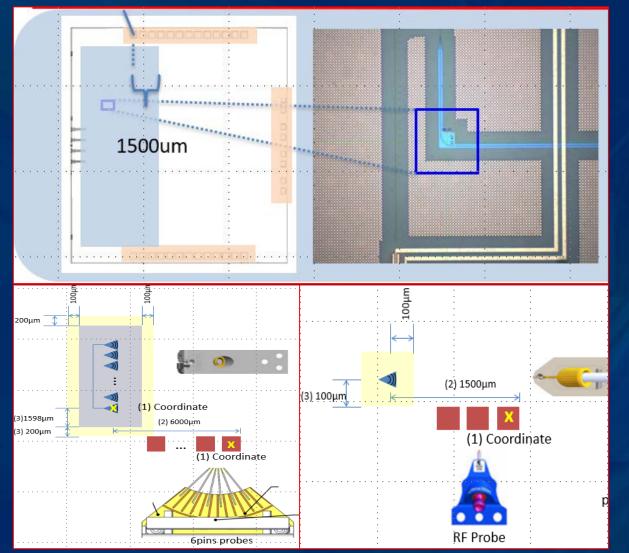


Types of IO	Orientation		
Optical Edge Couplers	West		
Electrical Pads (DC/RF)	North/South/ East		

*Flexible orientation possible by rotating the wafer* 

- O-band and C-band.
- Trench Width:  $\geq$  80 µm (zero change of existing layout).
- Trench Depth: :  $\geq$  40  $\mu$ m
- Number of Edge Couplers: 16.
  - Customization of edge fiber array possible for edge couplers ≥ 16.
- Edge Coupler Pitch: 127/250 μm.
  - Edge Couplers on same side of die.
- Electrical Pad (DC and RF) size: 80 x 80 μm (recommended)
  - Pitch 100 μm.
  - **RF Pads configuration GSG, GSGSG.**

## **Design Rule Layout**



CompoundTek wafer test design rule layout for both vertical and edge coupling available to customers during chip design to ensure wafer can be tested after Fab out

- Consists of keep out area for pads, edge couplers/vertical gratings
- Dimensions and design of deep trench

# **Typical SiPh Wafer Test Items**

#### **Electrical Test**

- Photodiode Dark Current
- Optical Modulator terminator, VOA, heater etc active structure IV (resistance) measurement.

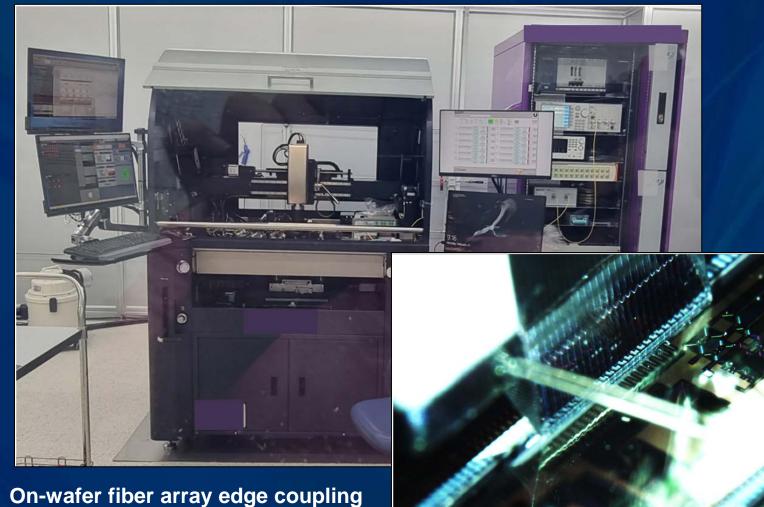
#### **Optical Test**

- Passive device parameter including IL, PDL, WDL etc
- Waveguide
  Propagation Loss
- Tap Coupler Coupling Strength

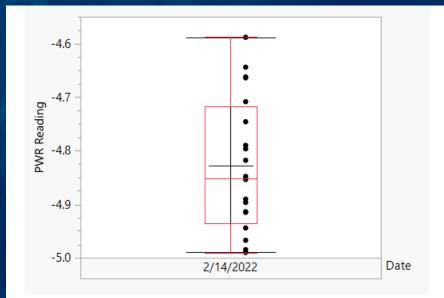
### **Opto-Electrical Test**

- Photodiode Responsivity
- Photodiode Bandwidth
- Modulator
  Extinction Ratio
- Modulator Bandwidth

# SiPh Wafer Optical Edge Coupling







#### **Edge Coupling Performance**

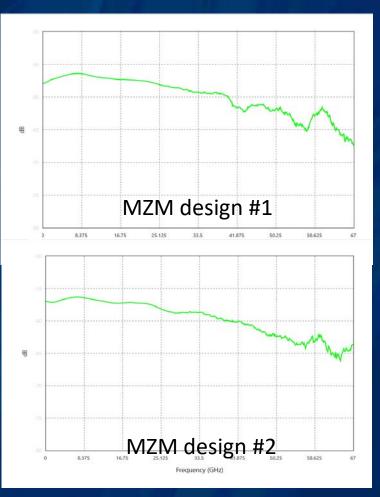
Trench Top Width	> 80µm (No change in layout )
Coupling Loss	~4.8 dB/facet (Depending on MFD mismatch)
Std Deviation	0.17dB

### Integration with LCA for Bandwidth Measurement

#### **Capable to perform Edge Coupling + Optical Bandwidth Measurements**



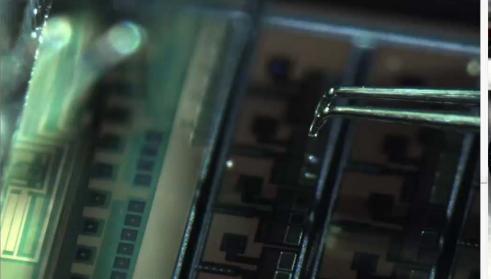
No significant bandwidth difference as compared to customer diced chip measurement

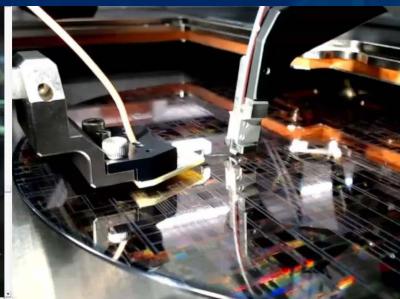


### **Photo Diode Test Video**

**Macro View** 

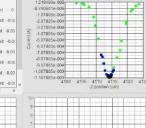
DUT

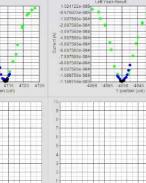


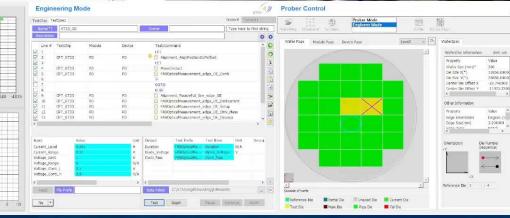


Coupsing algo limith, total time. 13.82(sec) : 0 2022,0401 14 15.30 BearPos(cm): 3388 40, -4850 00, 4114 10, -0.00(dtm) : 0 2022,0401 14 15.30 2022,0401 14 15.30 2022,0401 14 15.30 Left fine feasin, more left fasis b. -4869 00, macCurrent - 0.01 2022,0401 14 15.30 Left fine feasin, more left fasis b. -4869 00, macCurrent - 0.01 2022,0401 14 15.30 2022,04

9-					-
1					
7:					
8					
5	1				_
2	-				
2					
1					
0 1	2 3	4 5	6 7	8 9	10







Micro View

Video Demo on Edge coupling OE Testing on PD. 2 dies tested in video

1) Optical Input at West

FA Holder

**2)** Electrical probes at East

4th Annual SWTest Asia | Hsinchu, Taiwan, November 2-3, 2023

DC probes

# **Edge Coupling Performance**

	Key Features				
1.	Coupling Loss	CT average between 4 to 5 dB per facet			
2.	GRnR	Excellent GRnR, 0.17dB @ 1 sigma			
3.	Trench Width	> 85 um			
4.	Trench Depth	> 40 um			
5.	Coupler Pitch	127 um/250 um			

Enable fast yield and performance feedback on wafers by up to 3 months compared to chip level test. Saving up to a year for full product development cycle (assuming 4 iterations)

## Summary

- Need for SiPh wafer test solution to address market needs as SiPh volume ramps up in the next 5 years
- SiPh Wafer Test solution with both vertical and edge coupling designed for high volume wafer test.
  - CompoundTek Wafer edge coupling fiber array coupled with STAr Technologies wafer prober solution
- Solution proven with customer production SiPh wafers.
  - Optical Passive Test
  - Opto-electrical Test
  - High Speed Bandwidth test