Testing Challenges for Latest SiC and GaN Devices

Mr. Elia Petrogalli
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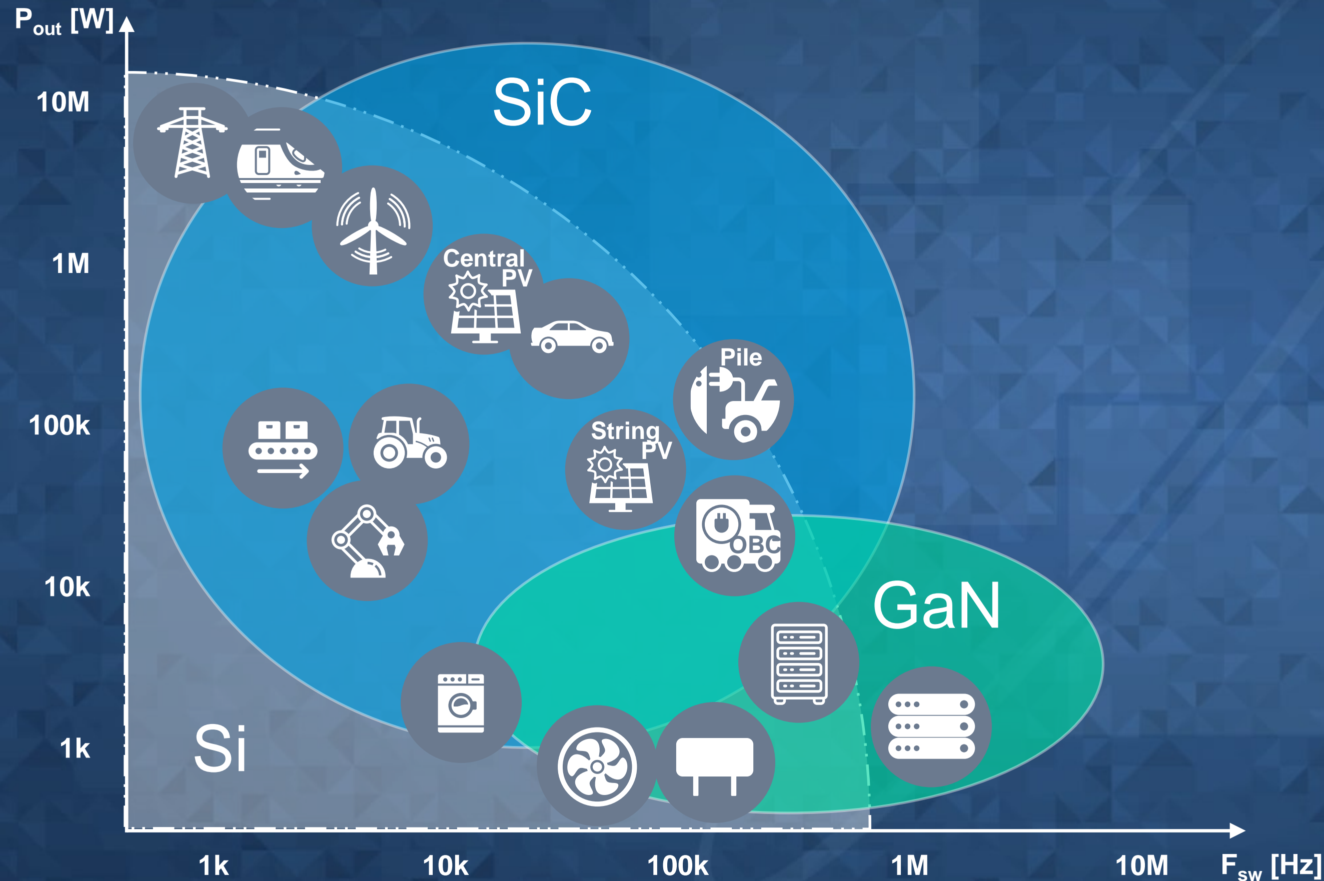
Overview



Silicon (Si)

- Main stream technology

Silicon Carbide (SiC)

- High Power – High Frequency
- Single phase + Three Phase

Gallium Nitride (GaN)

- Medium Power – Highest Frequency
- Single phase

Source: Infineon Technologies

Advantages of Wide Bandgap Devices

High Frequency Power Converter Circuits are becoming more and more desirable.

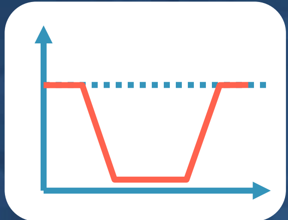
Wide Bandgap technologies like SiC and GaN offer promising opportunities to become a solid and viable solution for this type of applications.

Wide Bandgap devices vs **Silicon** advantages:

- Smaller Physical Size
- Lighter Weight
- Fast Switching
- Higher Voltage capability
- Lower Switching losses

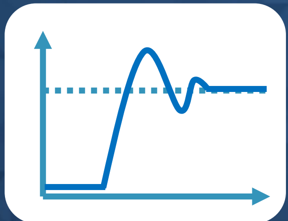
Testing Challenges

Wide Bandgap technologies also present a few drawbacks, that pose new challenges for the testing process.



Unpredictable conduction losses > Importance of **Dynamic RDS(on)**

The unpredictable conduction losses that characterize wide bandgap devices make the dRDS(on) test a crucial measurement to ensure the device reliability



Risk of voltage overshoots > Need to minimize **stray inductance** along signal path

Minimize voltage overshoots during commutation is a must, but the design of a correct signal path can be a time-consuming and costly process

High Voltage Testing on SiC KGD devices > Need to eliminate **electrical arcing**

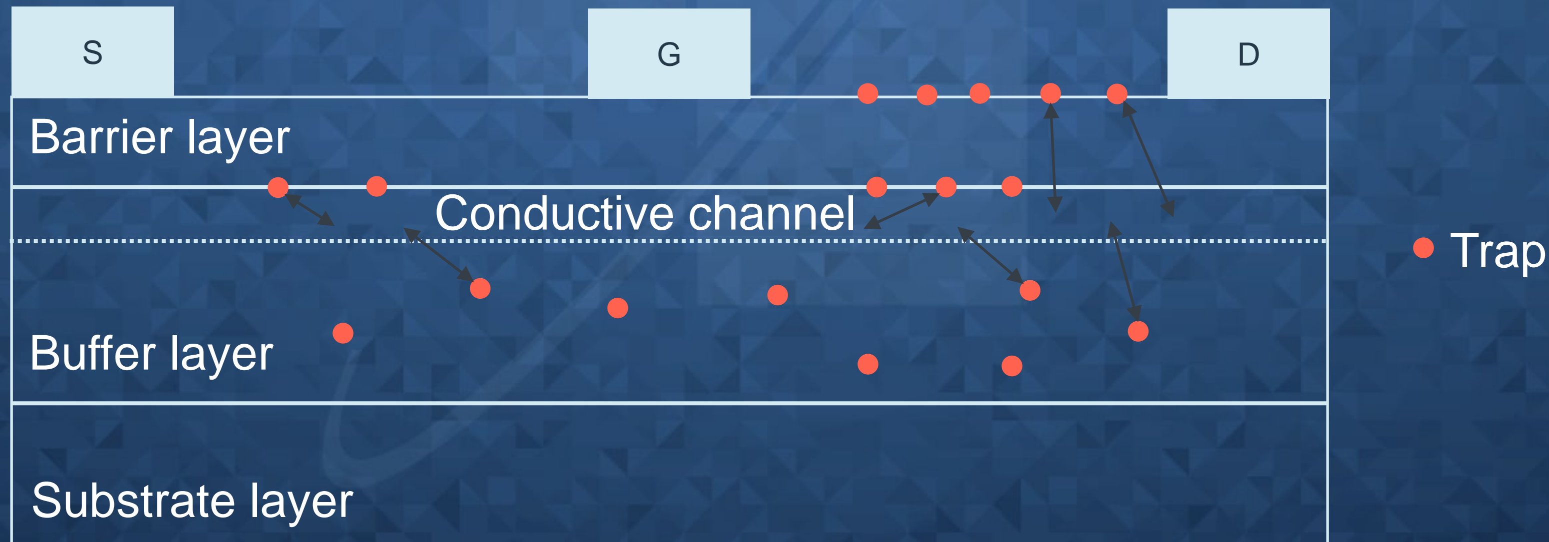
The absence of a molded package around the silicon, combined with the increasingly high breakdown voltage, increases the risk of electrical arcing during the device contacting

1

DYNAMIC RDS(on) TEST.

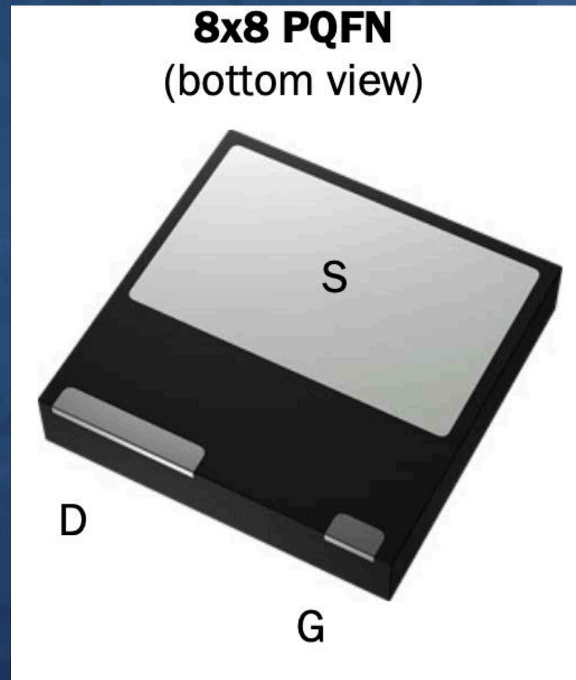
$dR_{DS(on)}$ Case Study Introduction

- $dR_{DS(on)}$ phenomenon in GaN structures is mainly due to the **drain bias voltage when the device is in cutoff** condition
- Electrons fill the trap levels on the surface and in the buffer layer under high electric field
- When the conduction channel is created by applying a proper V_{GS}, electrons must leave the traps before the drain current can reach the maximum value; otherwise, a current collapse will result when a high drain off-voltage is applied.



Selected **Device**

- We evaluated the ATE capability of measuring the dRDS(on), with a commercially available 650V GaN FET device.

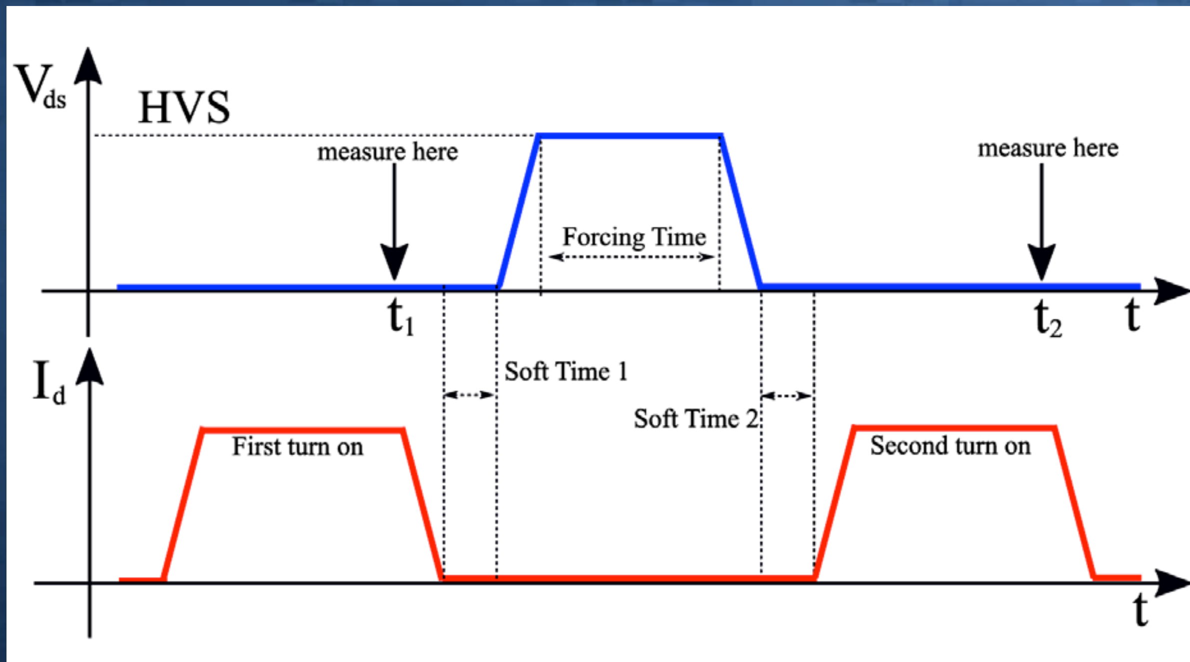


Key Specifications	
V_{DSS} (V)	650
$V_{(TR)DSS}$ (V)	800
$R_{DS(on)eff}$ (mΩ) max*	180

$dR_{DS(on)}$ Measurement Methods

Two measurements of the $R_{DS(on)}$ are needed, before and after applying a stress voltage to the component, to verify if current collapse occurs.

A critical aspect is the need to combine a wide measurement range (to cover both $V_{DS(off)}$ and $V_{DS(OFF)}$) with the high resolution required to get a consistent measure. With $V_{DS(off)}$ of hundreds of Volts, the minimum resolution of the oscilloscope would be close to 1V, which is completely unacceptable for $dR_{DS(on)}$ measurement.



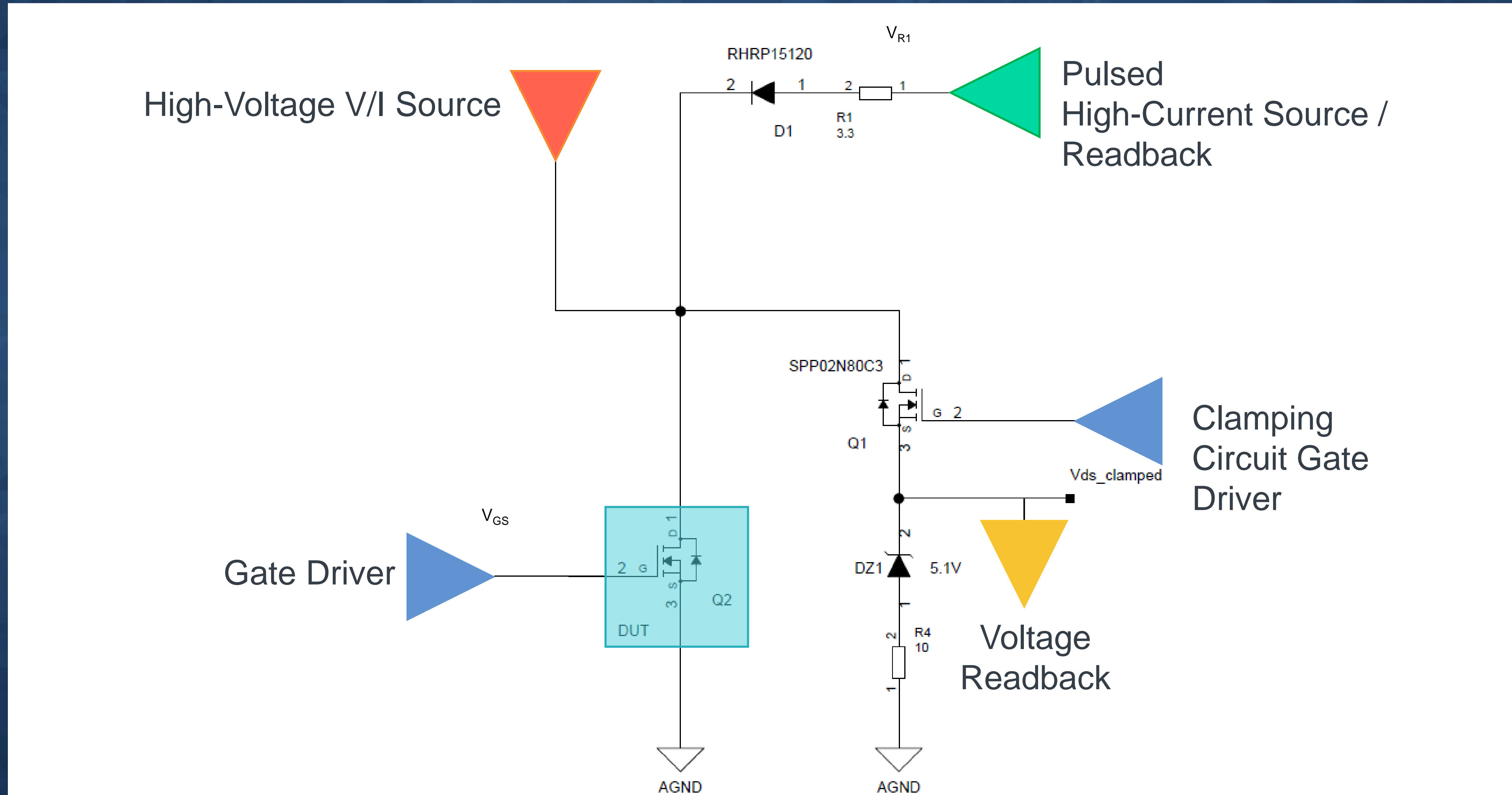
Test Flow:

1. Compute $R_{DS(on)1}$ by calculating the ratio between the measured V_{DS} and the forced current
2. Apply a V_{DS} stress voltage with the DUT in cutoff
3. Provide a constant current when the DUT is turned on
4. Measure the voltage drop between drain and source
5. Compute $R_{DS(on)2}$ by calculating the ratio between the measured V_{DS} and the forced current

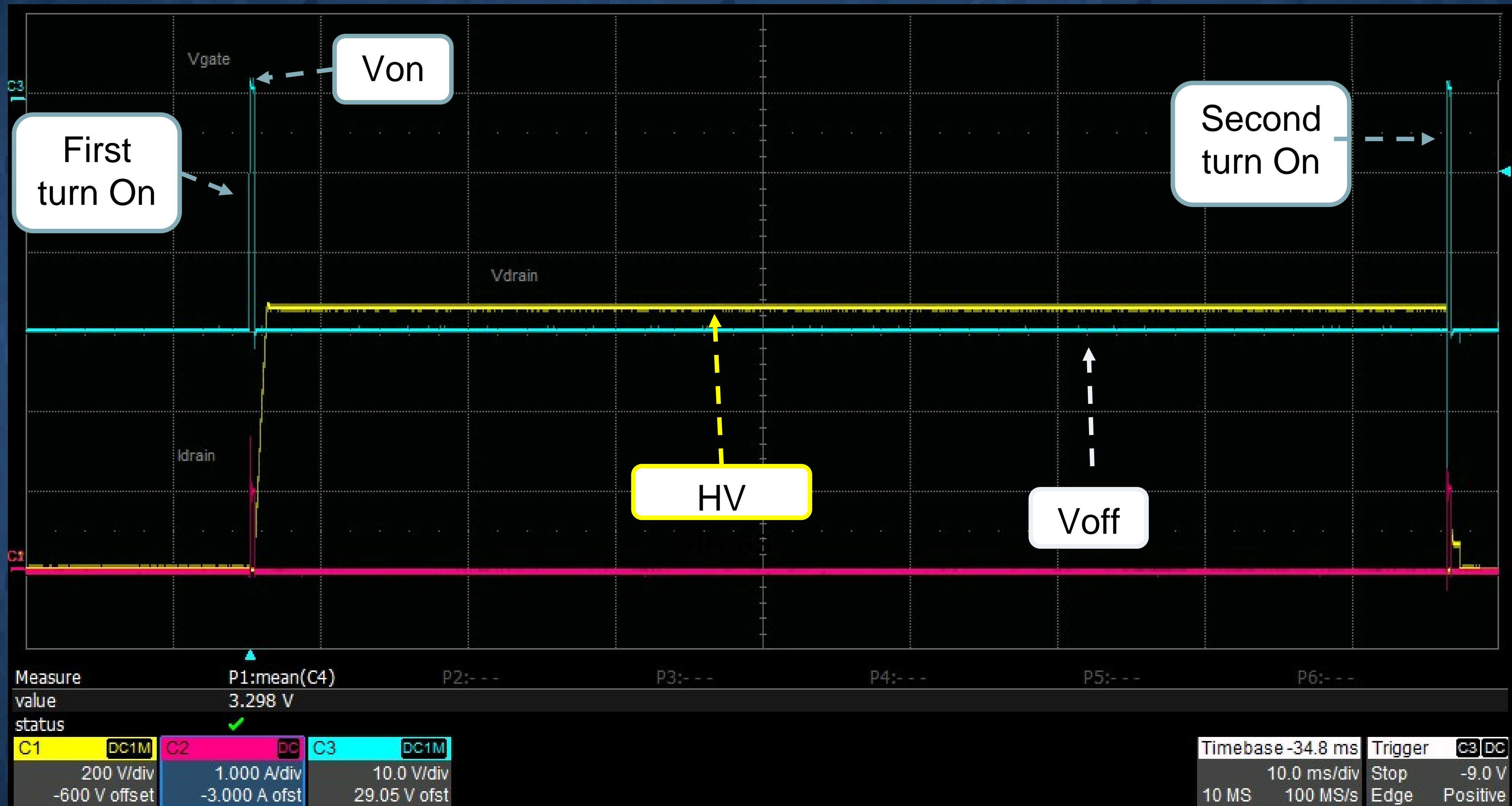
The current I_{DS} is provided through a pulsed current generator.

$dR_{DS(on)}$ Schematics

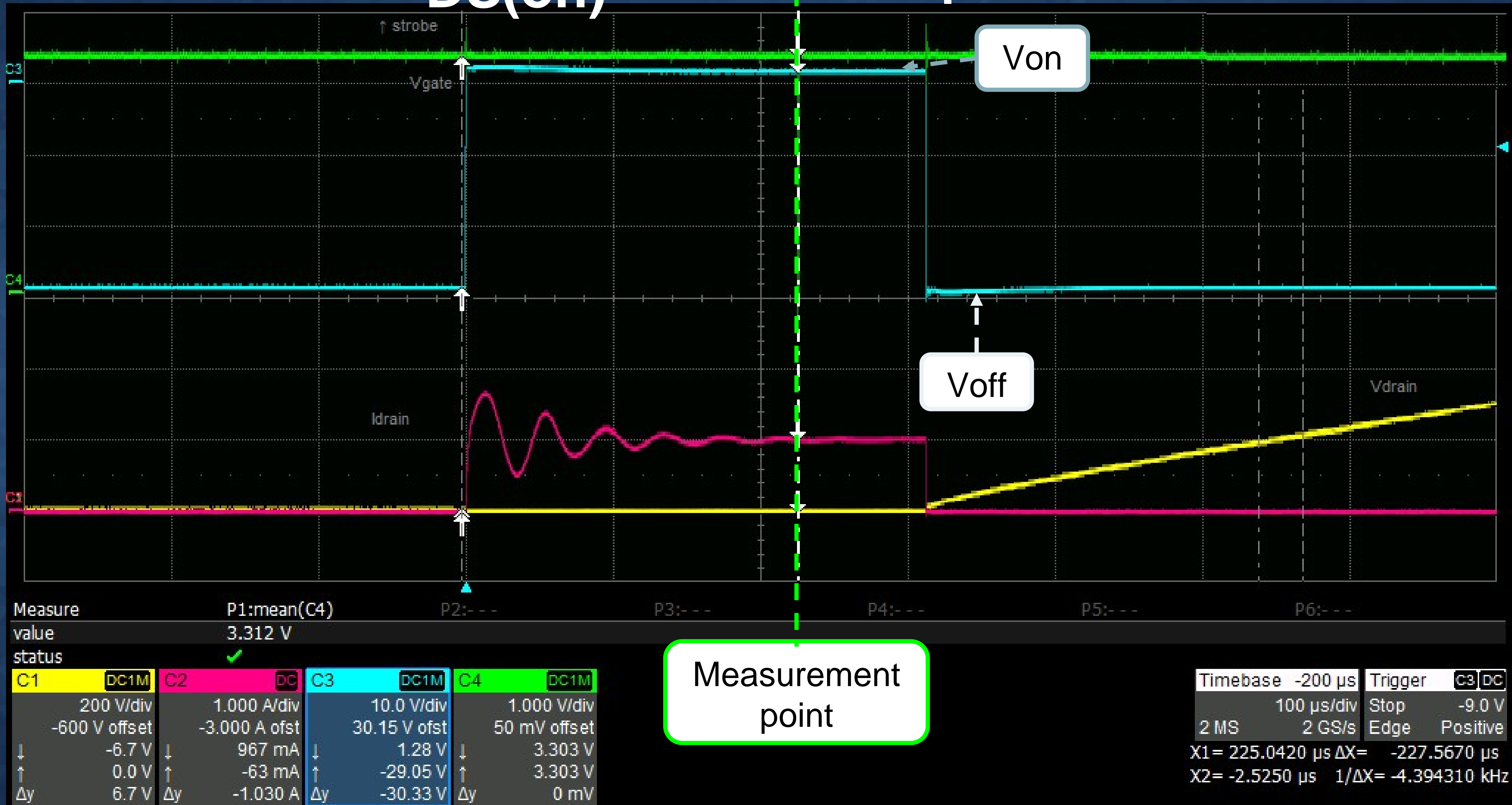
The electrical representation of the test circuit is the following:



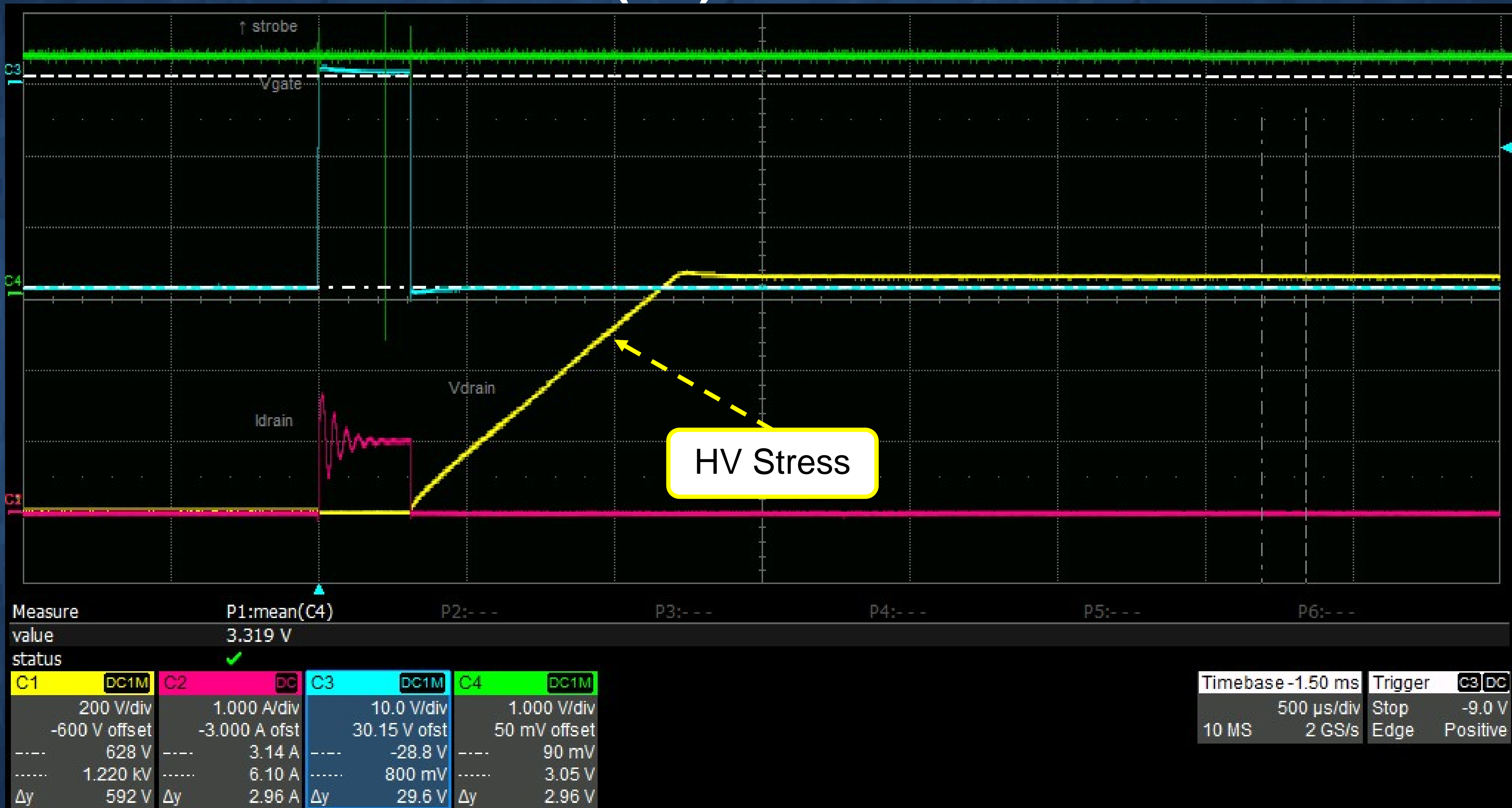
$dR_{DS(on)}$ Measurement Acquisition



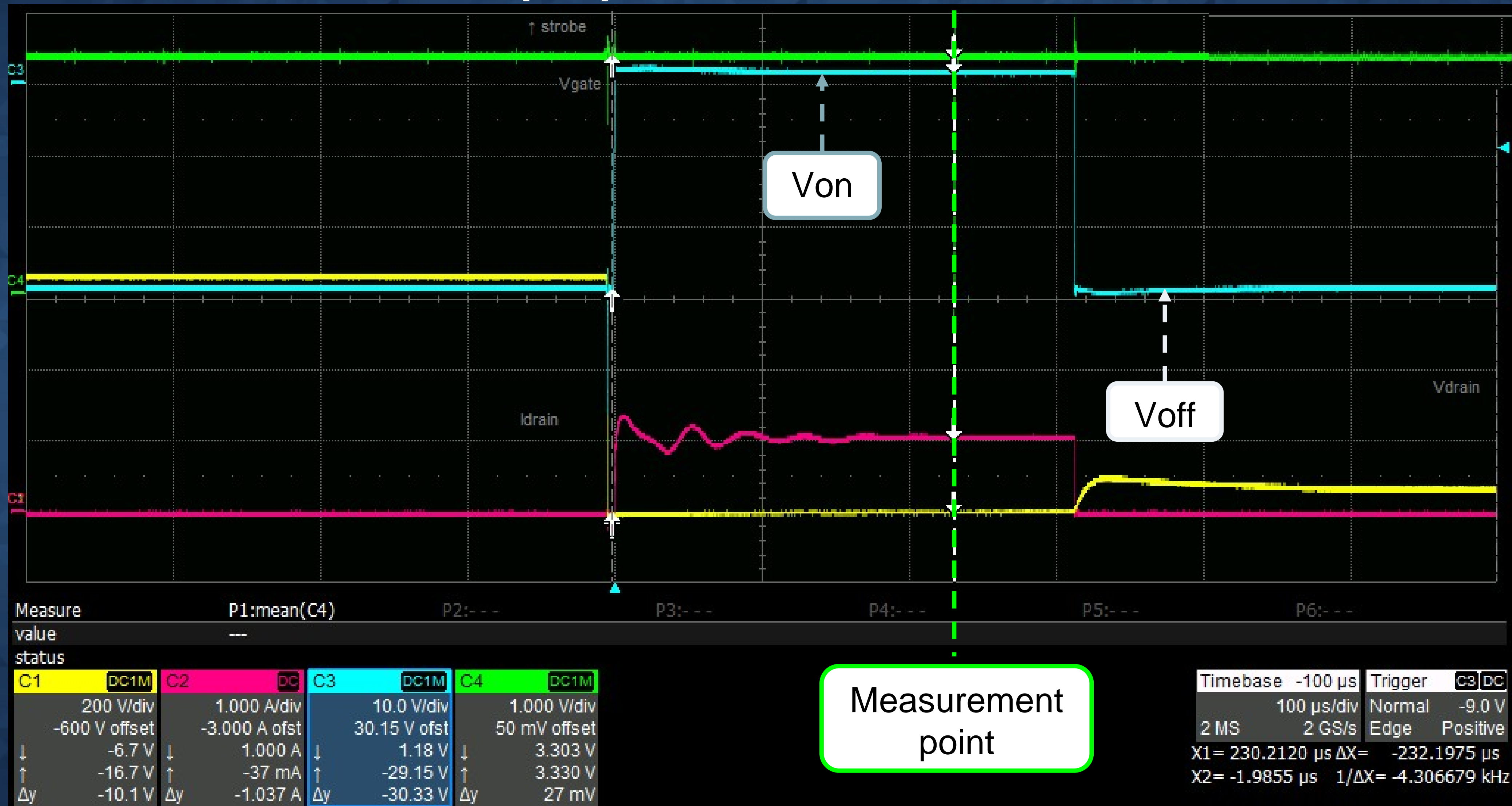
$dR_{DS(on)}$ First Acquisition



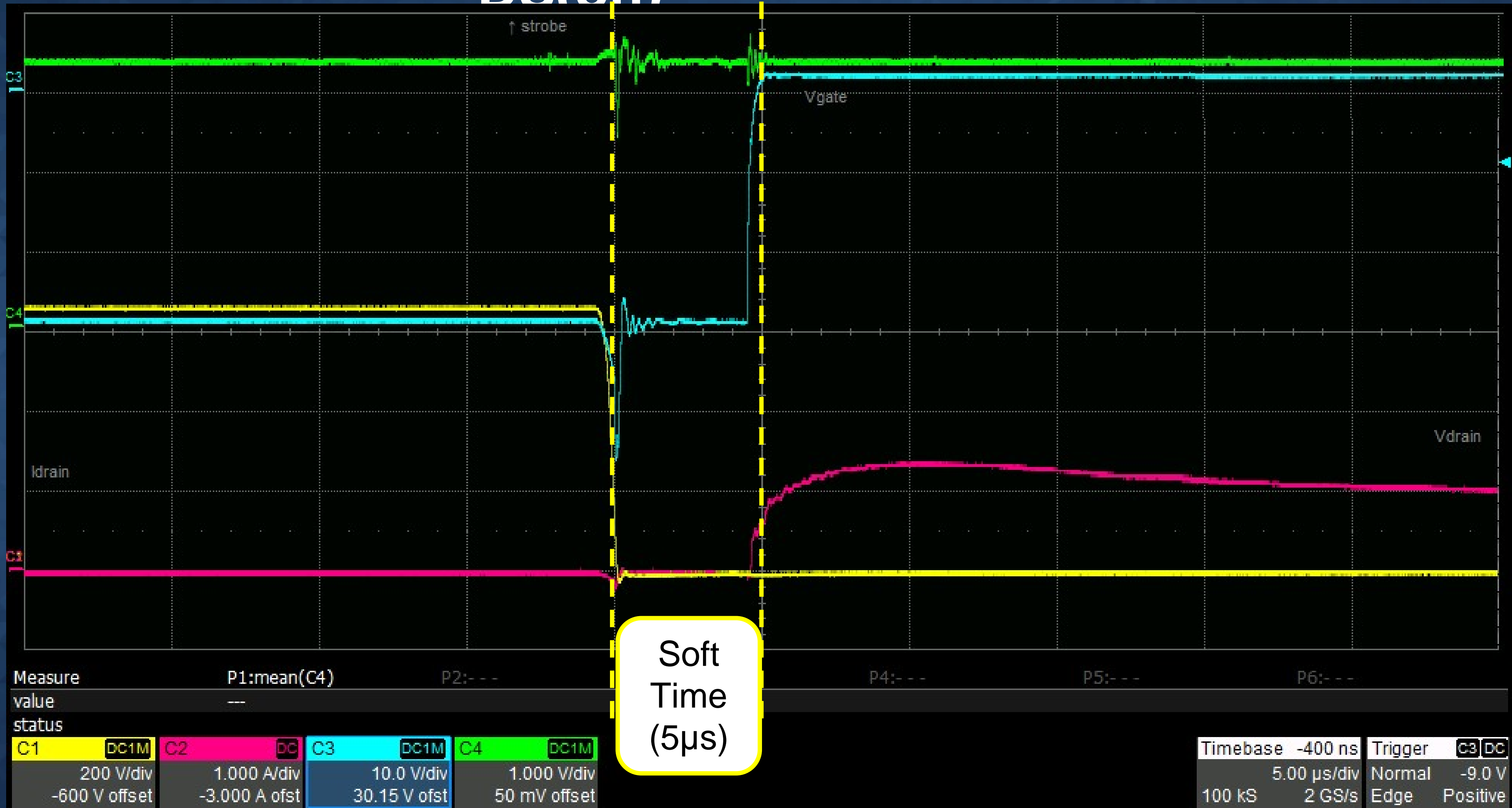
$dR_{DS(on)}$ HV Stress



$dR_{DS(on)}$ Second Acquisition



$dR_{DS(on)}$ Soft Time Detail



$dR_{DS(on)}$ Conclusions

- The test lead to the following results:

  $R_{DS(on)1}$ = 141.93 mOhm $R_{DS(on)2}$ = 153.03 mOhm

- The **two $R_{DS(on)}$ acquisitions have a difference of 7.8%**

- The proposed test methodology confirms the **possibility to perform challenging tests, such as the $dR_{DS(on)}$, with standard ATE instrumentation working in mass production**

2 MINIMIZE THE STRAY INDUCTANCE.

Introduction

- A **good design of layout and interconnection** of tester electronics, sockets and contactors is critical to minimize the overall stray inductance, in order to avoid the occurrance of voltage overshoots during commutation
- Ensuring the lowest value of parasitic inductance along the whole connection chain, from the tester to the device under test (including probe card, and sockets) can be **a time consuming and costly process**
- An **accurate software modeling of all the elements** can help the design process

DUT-Tester **Connection Chain Simulation**

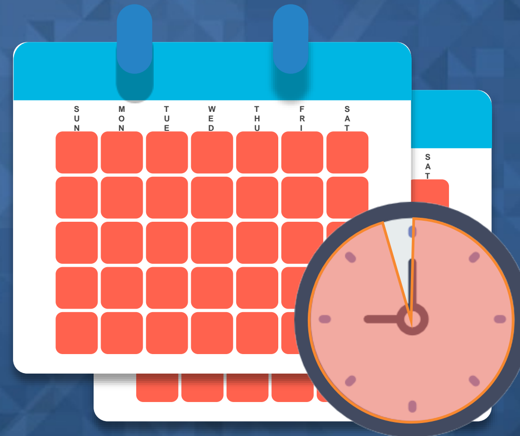
- The detailed software modeling of every element allows the test engineer to simulate the connection chain between tester, probe card, and device under test
- The test engineer can predict the behavior of all the elements, verifying:
    - **Power Delivery Network**
    - **Signal Integrity**
    - **Hybrid parts** (mechanical + electrical), in order to precisely calculate any parasitic inductance along the chain

Advantages

- **Early risk detection**
- **Quick design review**, based on simulation
- **First-time-right** hardware manufacturing
- Possibility to accurately **predict the behavior** of the hardware elements, by simulating all the possible critical conditions
- **Minimized debug and characterization**

APPLICATION DESIGN REVIEW

WITH REAL HARDWARE:

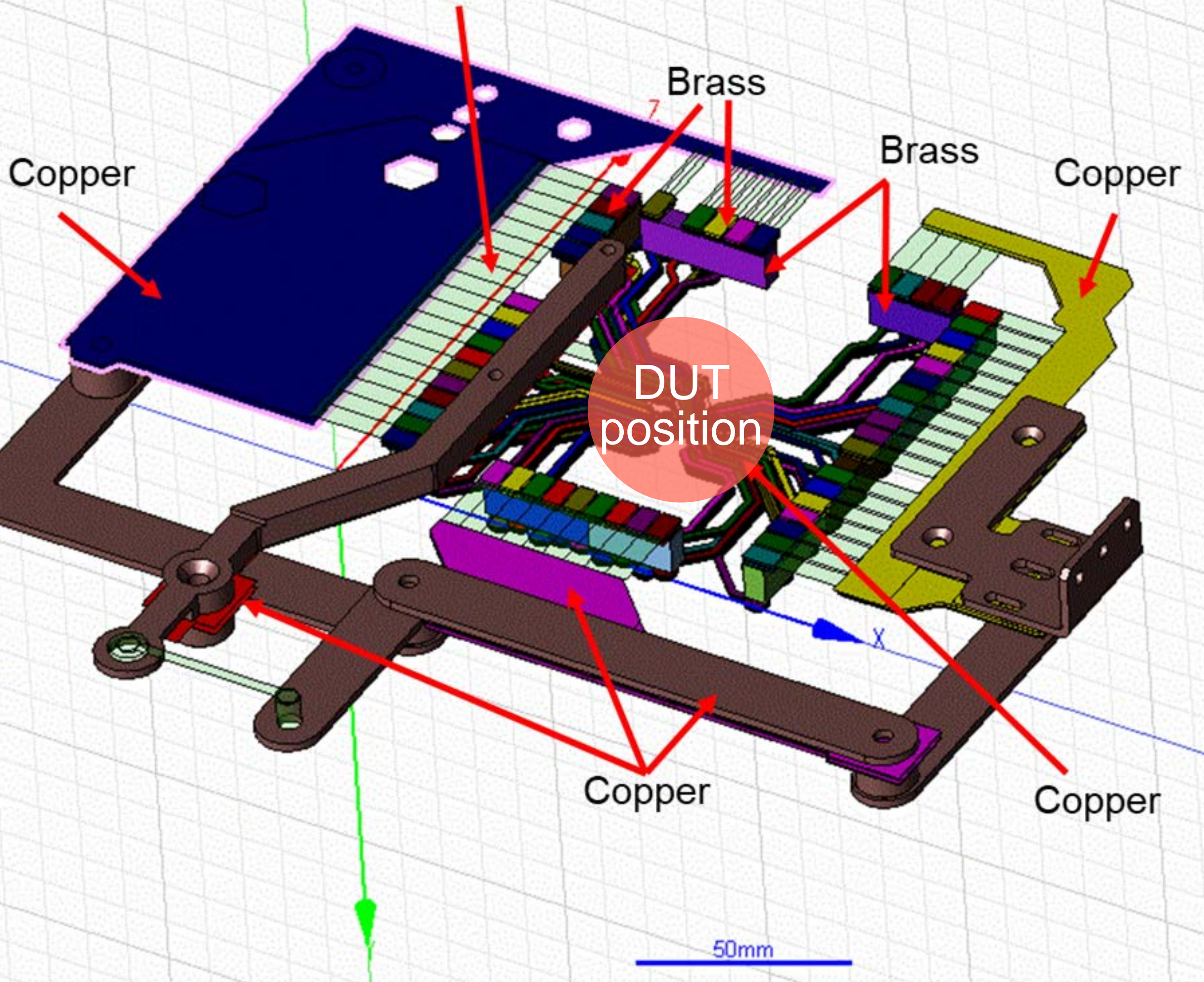


Several weeks

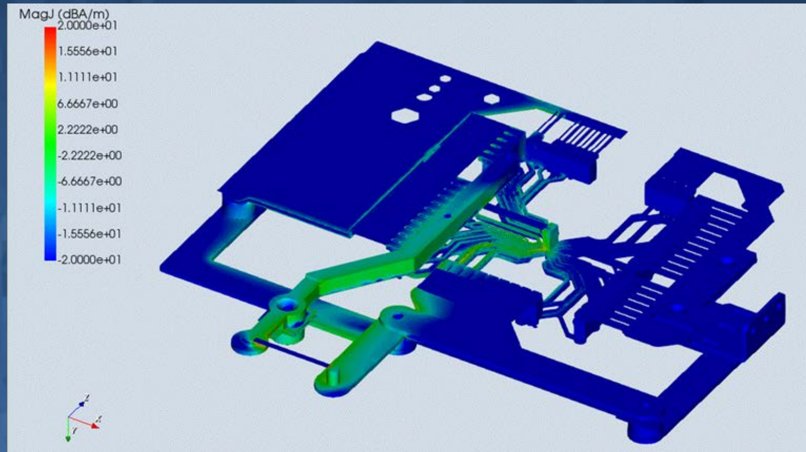
BASED ON SIMULATION:

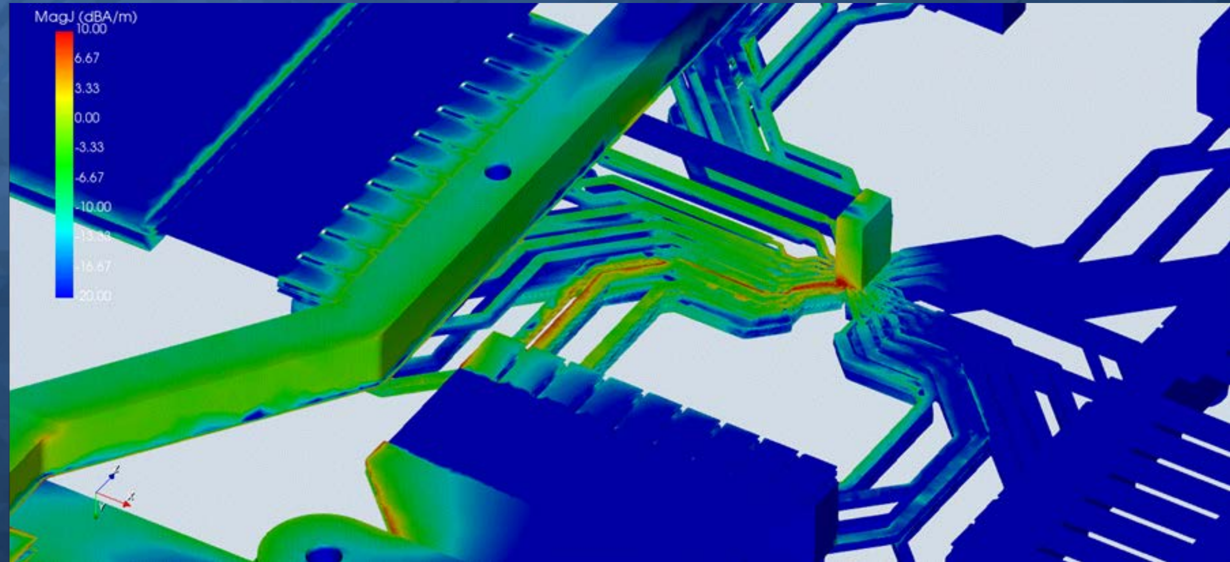
2-3 days

Example: **KGD Contactor Structure**



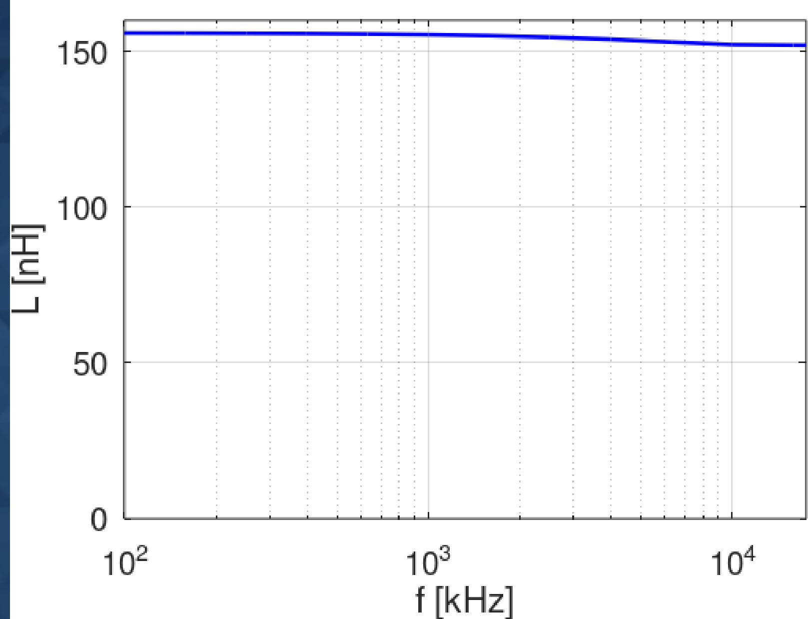
CURRENT DENSITY ANALYSIS @10MHz





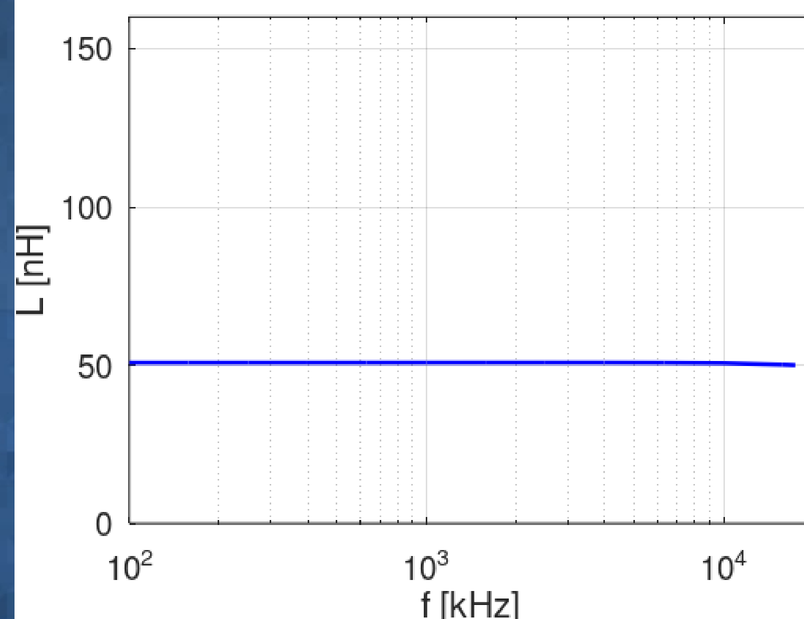
Stray Inductance Analysis

STEP 1



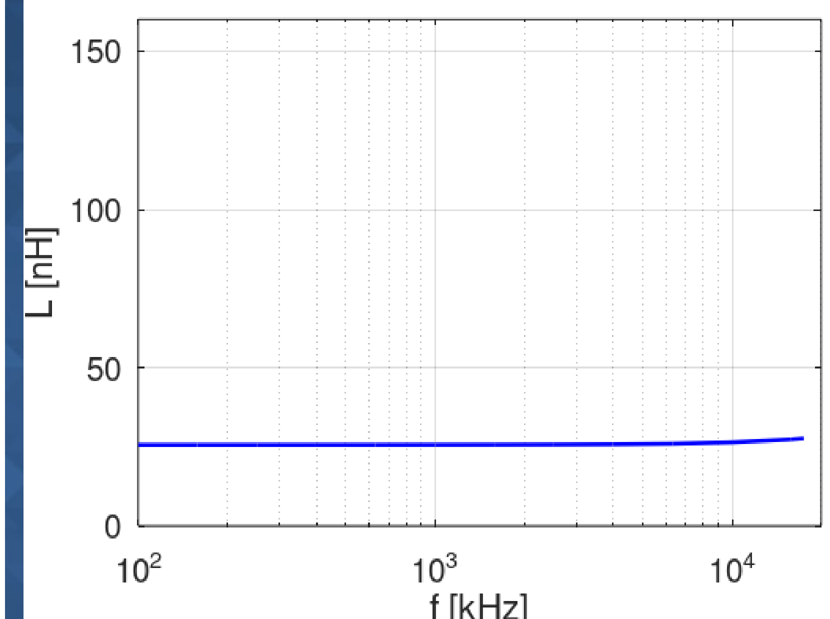
It can be seen that the inductance is fairly constant along the frequency range, and it is about 155.5nH at 1MHz.

STEP 2



A first design review of the contactor has been carried out: several functions that were carried our by hybrid structures (mechanical + PCB) are now incorporated in the PCB. Stray inductance is significantly lower.

STEP 3



After a second design review (consisting in a layout optimization that reduced the overall size), the stray inductance is lower than 25nH in the whole frequency range of use.

Conclusions

- The simulation of the behaviour of all the connection elements allows the test engineer to:
    - Get a first-time-right hardware, with no need of further re-design and adjustments after manufacturing
    - Validate the design by simulating a high number of possible variants and conditions that could impact on the stray inductance
- As a result, the **stray inductance will be minimized, controlled, and replicable** in the production environment; this will eliminate the negative effect of voltage overshootings

3

POWER KGD TESTING.

Wafer Testing can be not enough

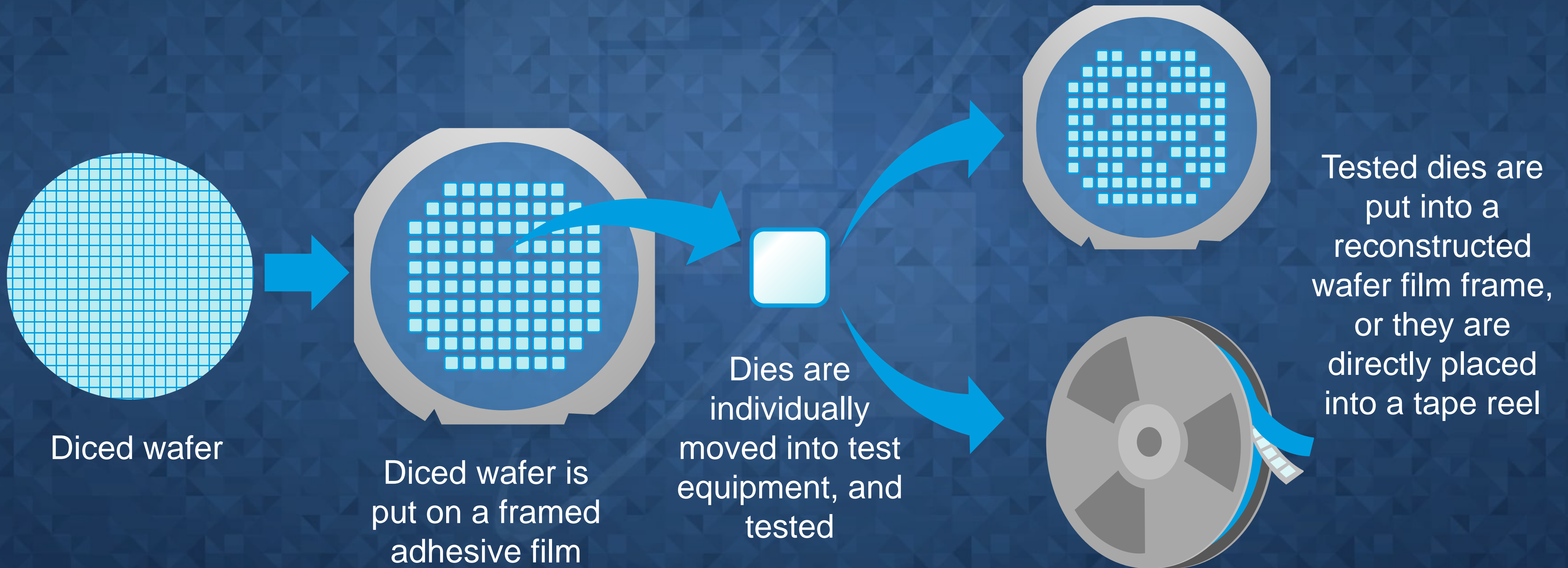
The parametric testing executed at wafer level is not sufficient to eliminate the failure rate on WBG power components:

- It is not possible to reach the voltage and current ratings required
- It is not possible to perform all the dynamic measurements to ensure that the device performances meet the datasheet specifications
- Die-to-die interference can affect the test performance

This will inevitably turn into yield loss, defective assemblies, parametric drift.

KGD Testing Process

To guarantee the goodness of KGD, it is necessary to bring at die level the same performance and methods that are used to screen out defects in the final test phase.



KGD Testing Challenges

TEST COVERAGE

- **DC parametric testing**
- **AC testing**, conditioning the DUT with high current and high voltage simultaneously to verify the device switching parameters
- **UIS/UIL Avalanche**
- **RG/CG**
- **Short Circuit Testing**
- **Thermal conditioning**

THROUGHPUT

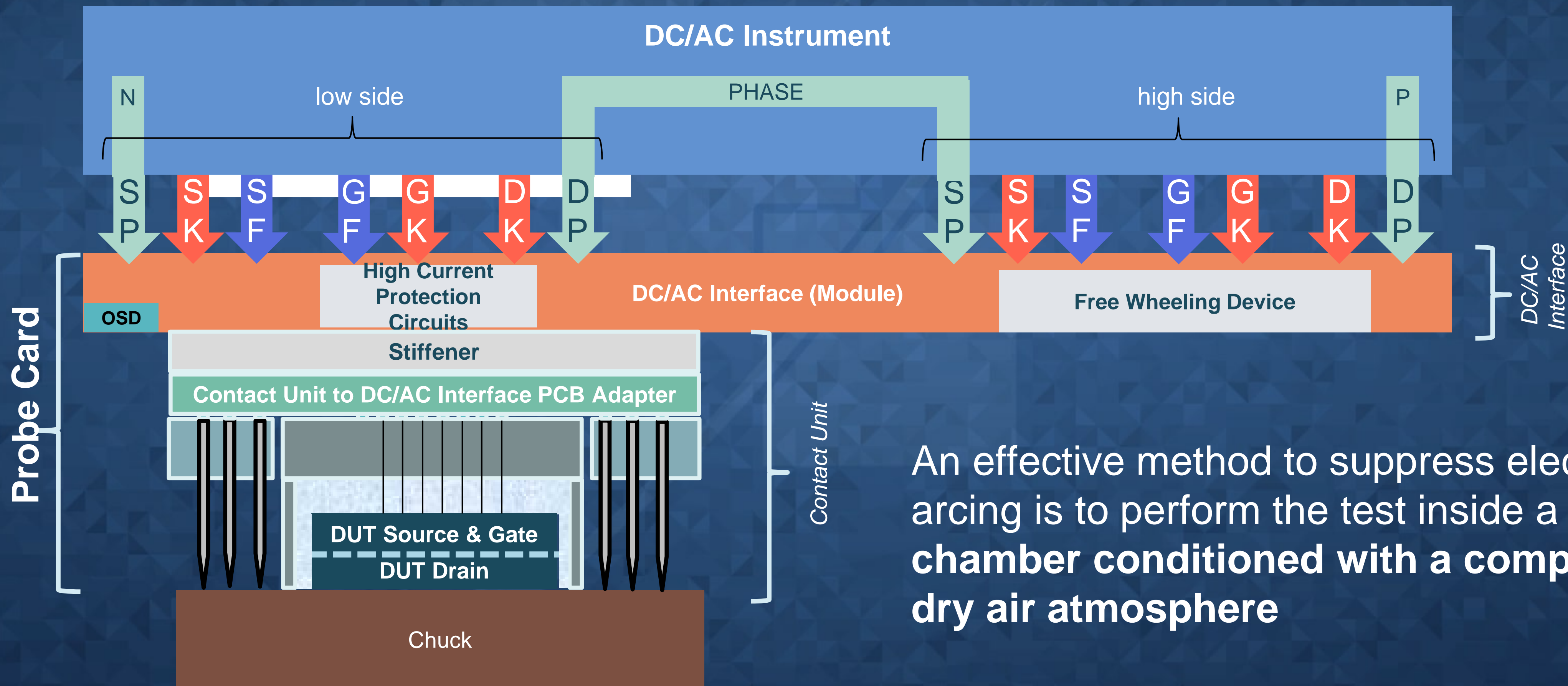
- **Automatic handling from / to diced wafer**
- **Process integration (handling, chuck, probe, thermal conditioning)**

PROTECTIONS

- **Anti-arcing for high voltages**
- **Overcurrent and overvoltage protection circuits**
- **Voltage monitors on output relays commands**
- **Open/short check**
- **Contact needle protection**

Anti-arcing for high voltages

Typically, when measuring voltages above 1000V, there will be electrical discharge (arcing) between probe needles. This also occurs between the DUT and adjacent devices (vertical layouts) or other test pads (lateral layouts).



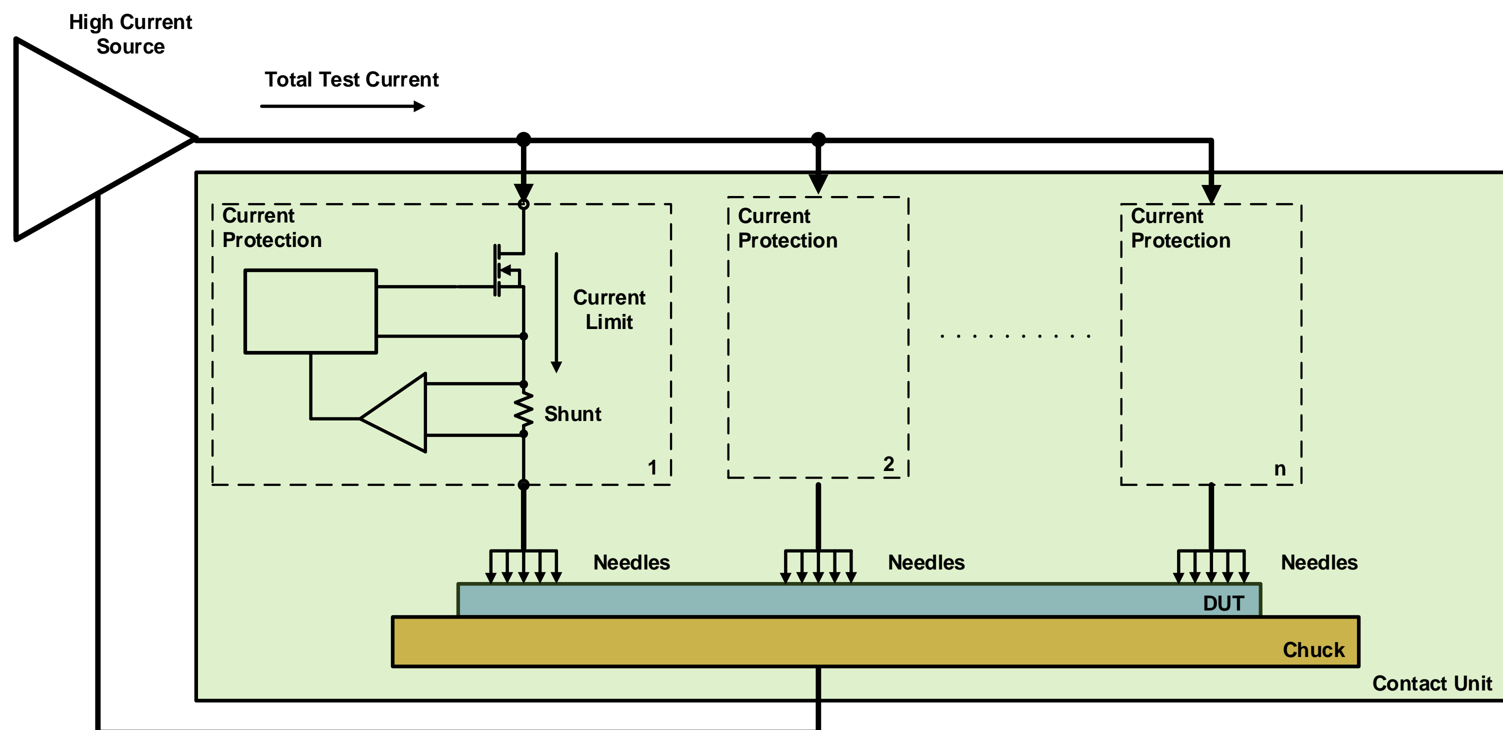
An effective method to suppress electrical arcing is to perform the test inside a **test chamber conditioned with a compressed dry air atmosphere**

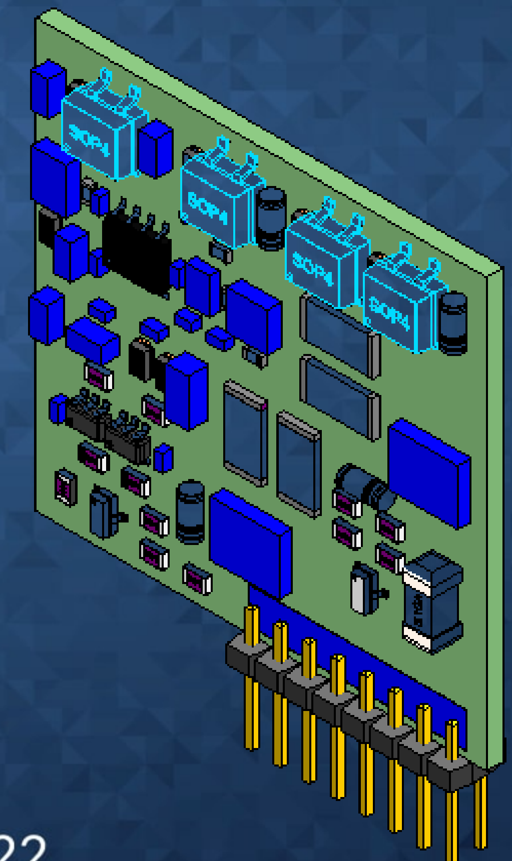
Contact Needle **Protection Circuit**

High current values involved in power testing can damage the contact needles used to probe the DUT.

A protection circuit can be used to limit the current in the contact needles. This current limiter should be sized based on the carry current of the needles themselves.

Typically, the needles are grouped: this circuit also enables to balance the currents between the different groups of needles.





Conclusions

Answering the test challenges that SiC and GaN devices pose, relying on industry-standard test equipment, is the way to performant, high-throughput production test.

In detail, we saw how test equipment can answer 3 major challenges:

1. Need to perform **Dynamic RDS(on) test**, to detect unpredictable conduction losses

Standard ATE instrumentation can be suitable to perform this and other challenging tests

2. Need to **minimize stray inductance** to avoid voltage overshooting during commutation

Software modeling can be proficiently used to simulate and analyze the stray inductance, designing all the hardware connections and layout so as to minimize the stray inductance

3. Need to perform **KGD test on diced dies**, to verify that the DUT performances meet the datasheet specifications

Dedicated **KGD test equipment** can perform automatic handling and test of diced dies, including AC test in **anti-arcing test chambers**