POSTER #SWTA24-45

Hybrid Bonding Technology for Next-Generation 3D-IC/Chiplets

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Supercomputer with AMD's 3D V-Cache Using Enhanced Chiplet & Hybrid Bond

AMD 1st Gen. EPYC 7001

3D V-Cache (8 Core + L3 cache) × 8 chips = 64 Core

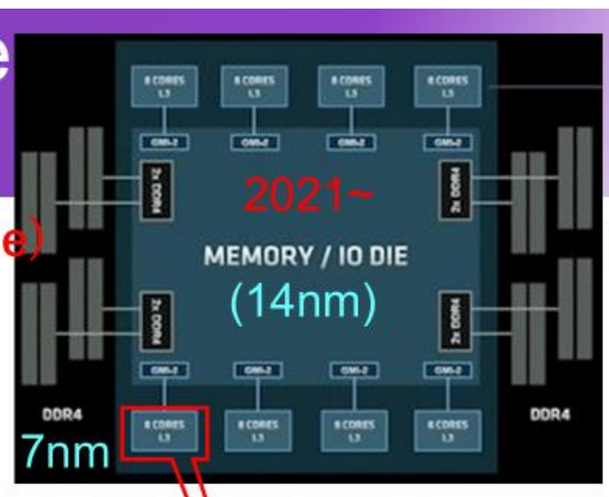
4 Core × 2 × 4 chips = 32 Core
(Die size: 4 × 213mm² = 852mm²)

2017~ 1st Gen EPYC™

32 core
852mm²

4 CPU dies inc.
memory & I/O (14nm)

32 core
777mm²



2021~

2022~
4th Gen. EPYC
9004 series
CCD die (5nm)
I/O die (6nm)

Structural Si (STEM:
Si Thermal Enhancement Module)

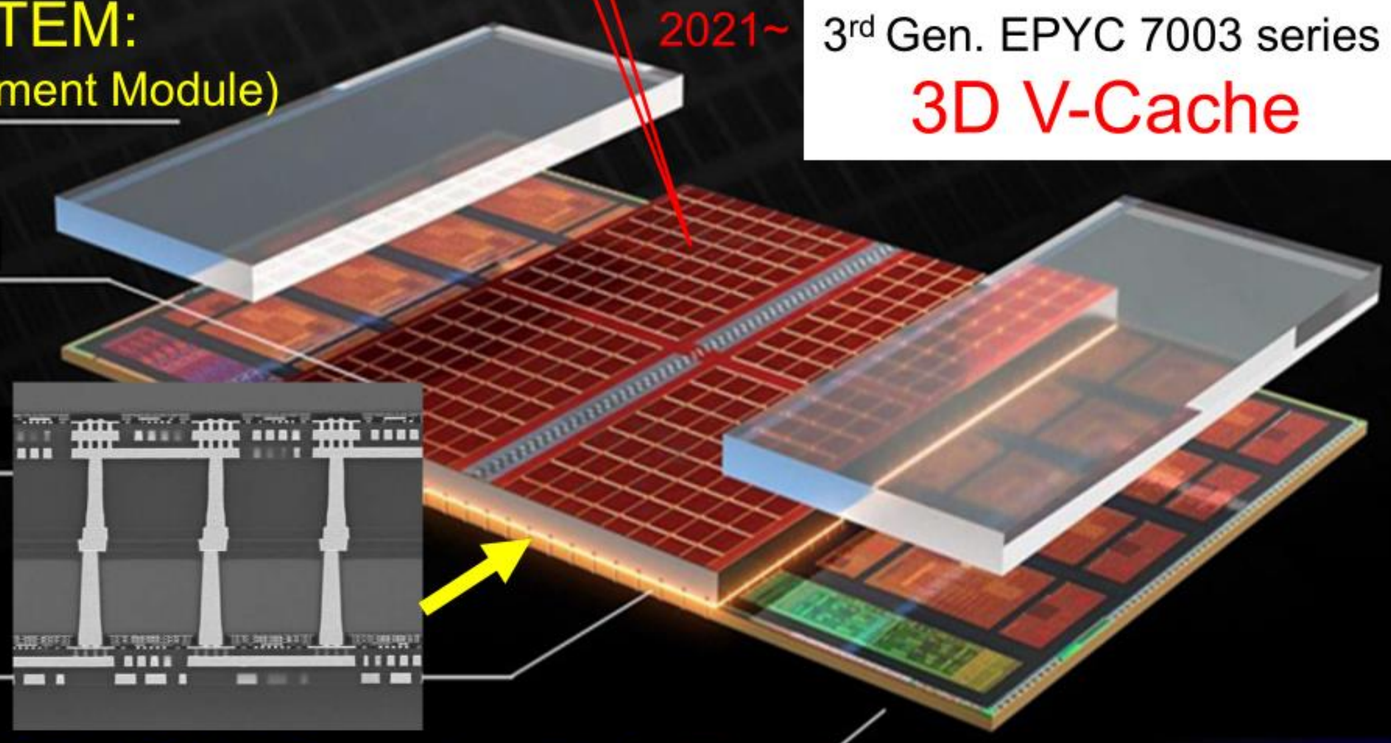
L3 Cache

Hybrid bonding

TSV

8 Core Zen 3 CCD (CPU Complex Die) (7nm)

2021~
3rd Gen. EPYC 7003 series
3D V-Cache

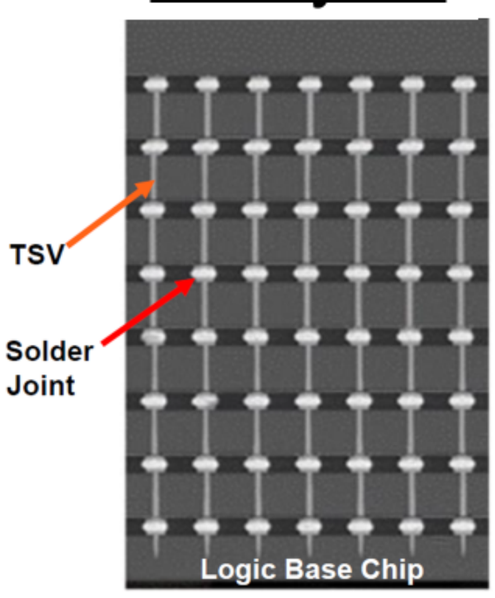


AMD

Requirement for Chip-to-Wafer Cu-Cu/SiO_2-SiO_2 Hybrid Bonding

3D-staked DRAM
(HBM:
High-Bandwidth Memory

12 layers



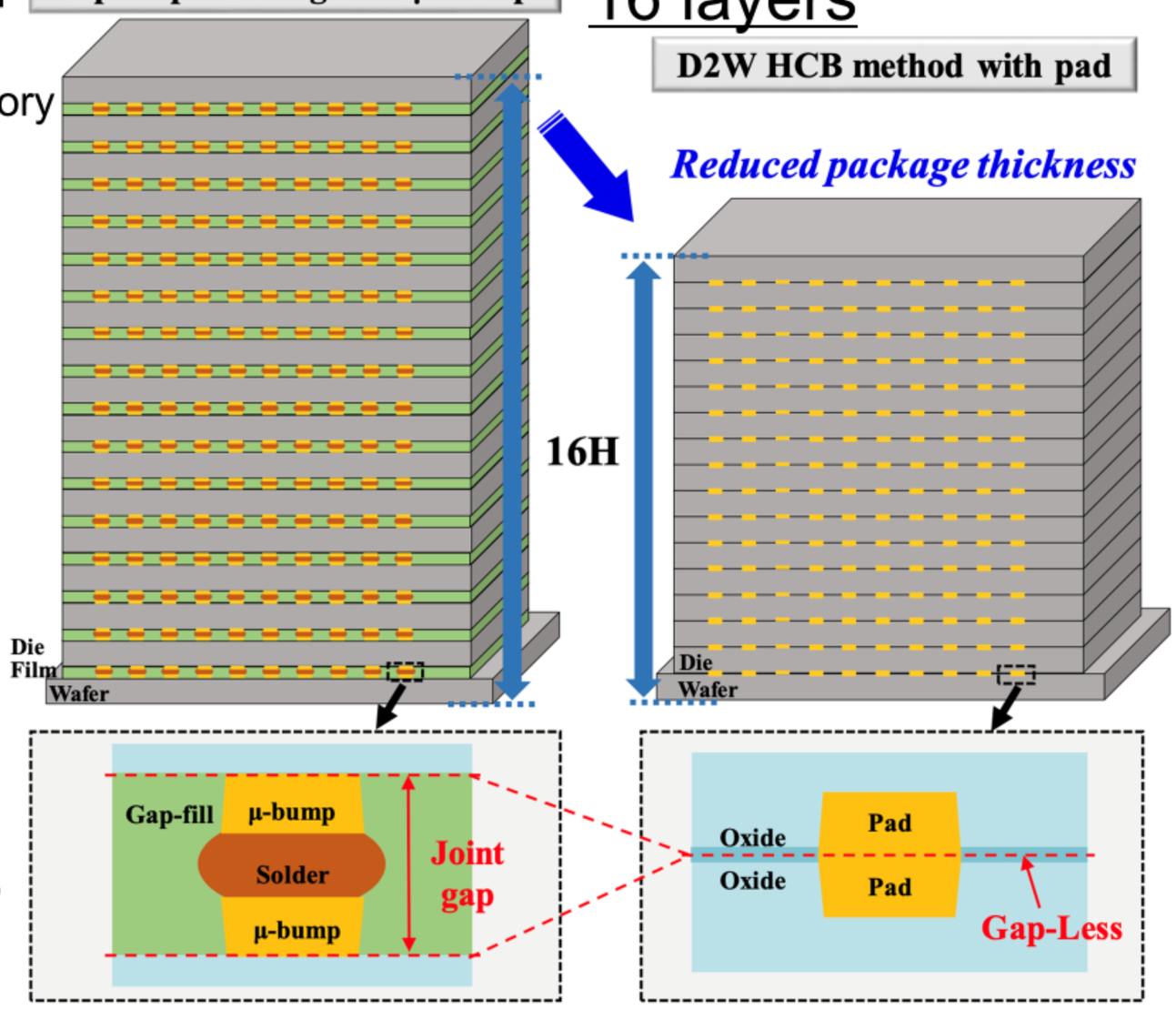
HBM2

Flip-chip bonding with μ-bump

16 layers

D2W HCB method with pad

Reduced package thickness



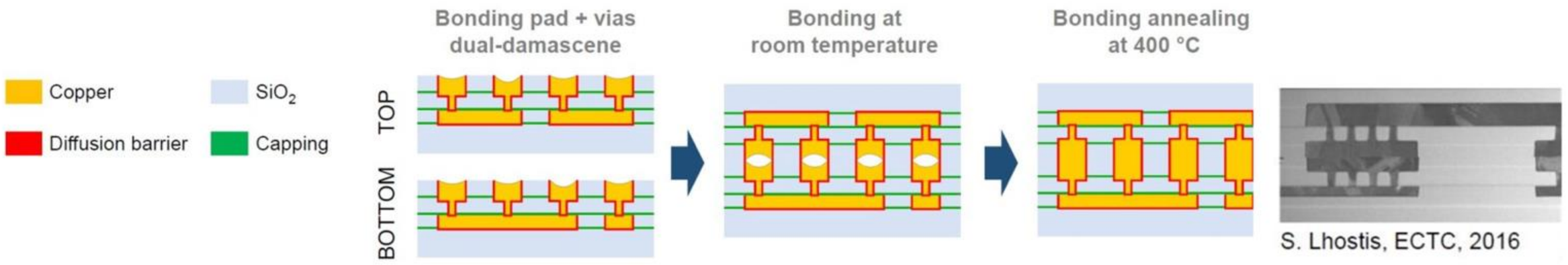
M.-K. Kim *et al.*,
1672–1676,
ECTC2023

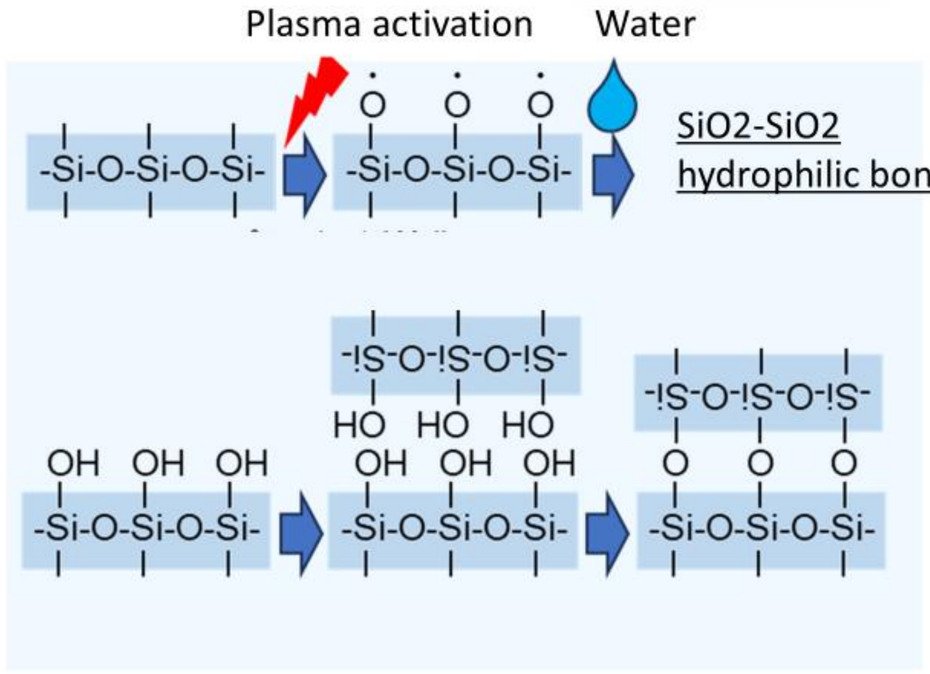
Requirement

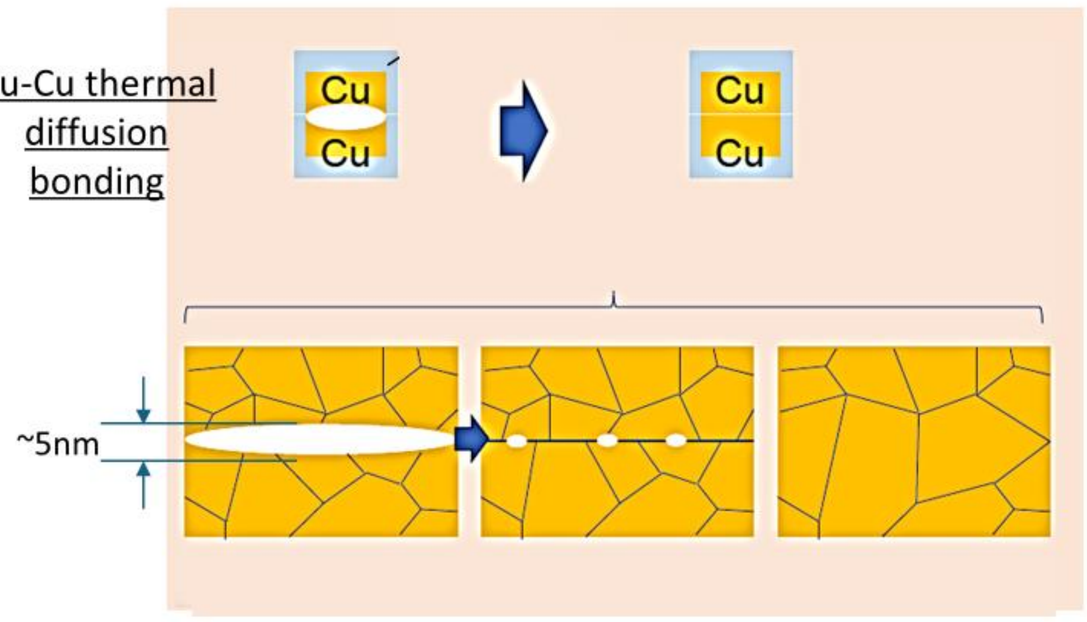
- More than 16 layers
- Alignment accuracy
  DRAM ±1μm
  CPU/GPU ±0.1μm
- Assembly throughput
  >36,000 UPH
- Bonding pressure
  < 1MPa
- Bonding temperature
  < 200℃
- High thermal conductivity
  No underfill/solders

SWTest Asia Conference 2024, Oct 24 to 25, 2024

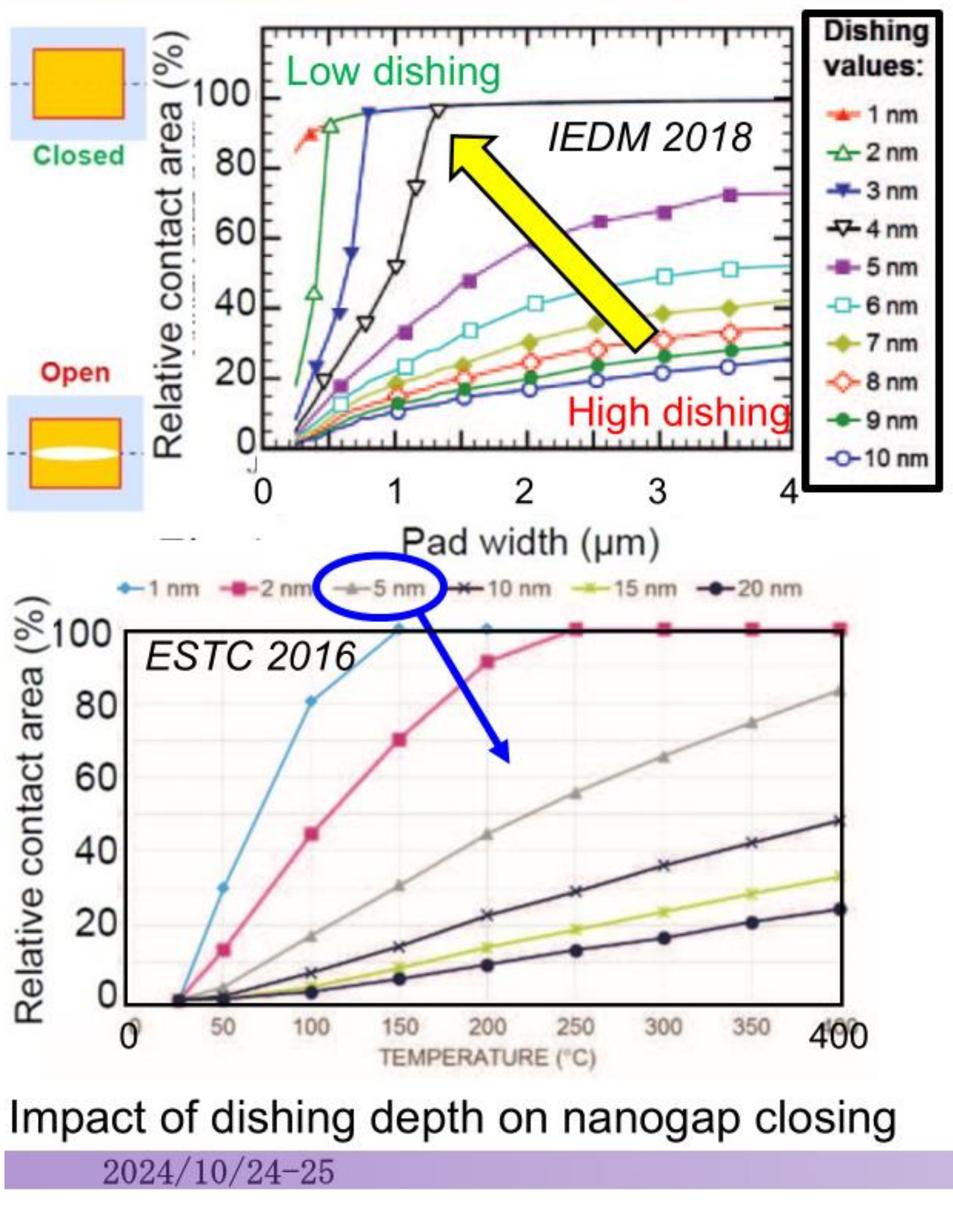
Typical Cu-Cu/SiO_2-SiO_2 Hybrid Bonding Flow







Cu-Cu/SiO_2-SiO_2 Hybrid Bonding Parameters



Impact of dishing depth on nanogap closing

Low-temp. bondability	Sort bond time	Bond energy Incl. between Cu & SiO_2	Adhesion & Cu barrier
CMP compatibility (Dishing, Erosion, Corrosion etc.)	Plasma compatibility & Q-time	High-throuput & high accuracy trade-off	Small warpage & low stress
Fine-pitch & Dielectric property	Low loss & Low water uptake	Electromigration tolerance	Thermal dissipation
Cu orientation control	Cu passivation against CuOx	Cu grain size & Cu diffusion length	Particle (tolerability))

Useful Links for Technical Posters

If you have any questions, please contact

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IEEE Spectrum / **Hybrid Bonding Plays Starring Role in 3D Chips**

The quality of the connection counts, too. The metals in chip interconnects are not a single crystal; instead they're made up of many grains, crystals oriented in different directions. Even after the copper expands, the metal's grain boundaries often don't cross from one side to another. Such a crossing should reduce a connection's electrical resistance and boost its reliability. Researchers at Tohoku University in Japan reported a new metallurgical scheme that could finally generate large, single grains of copper that cross the boundary. "This is a drastic change," says Takafumi Fukushima, an associate professor at Tohoku. "We are now analyzing what underlies it."

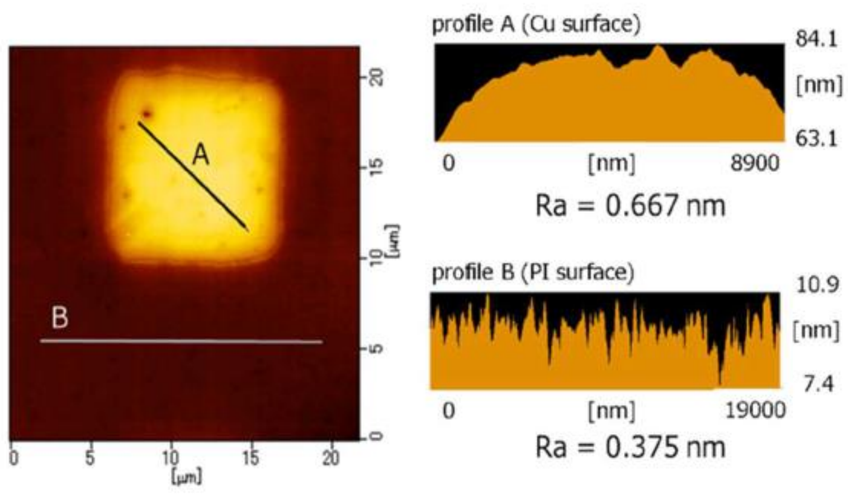
"I think it's possible to make a more-than-20-layer stack using this technology."

At ECTC, researchers from Tohoku University and Yamaha Robotics reported work on a similar scheme, using the surface tension of water to align 5-μm pads on experimental DRAM chips with better than 50-nm accuracy.

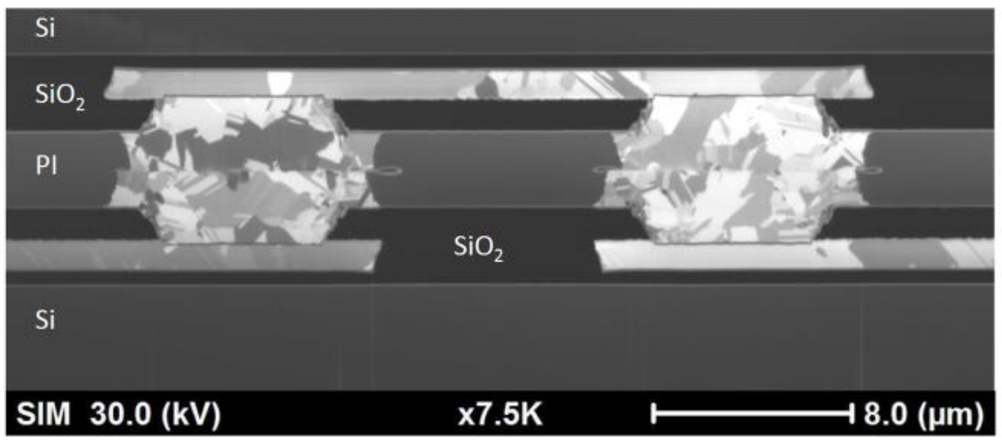
IEEE Spectrum 11 Aug 2024

Tohoku's Hybrid Bonding Activity in ECTC2022

AFM Image



Cross Sectional SEM Image



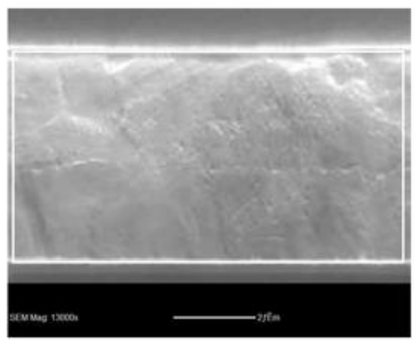
Excellent bonding interface was observed.

Soft organic dielectrics can ignore (embed) small particles.
CTE is higher than Cu, and dishing control is not so critical.

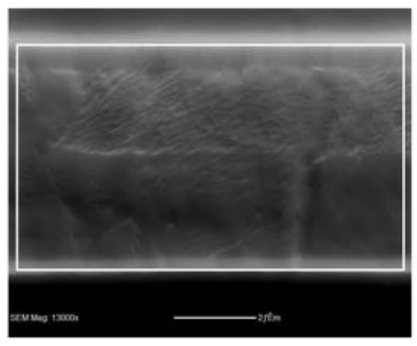
Tohoku's Hybrid Bonding Activity in ECTC2023

Annealing at 400℃

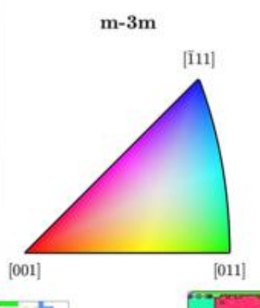
Plating chemistry A



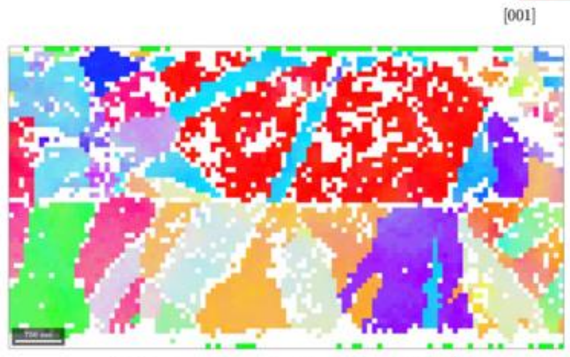
Plating chemistry B



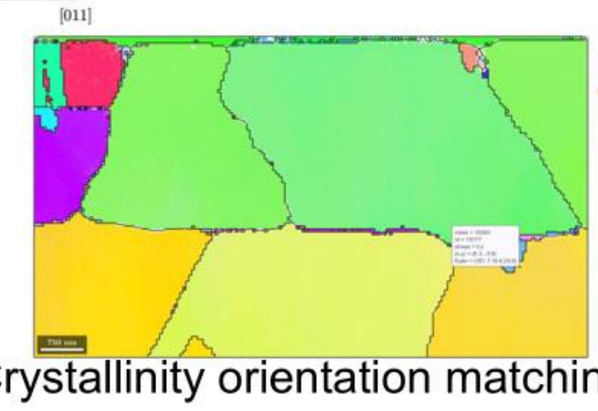
Annealing at 300℃



Random multigrain



Random orientation



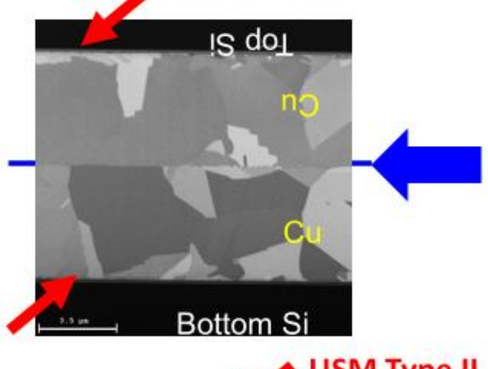
Crystallinity orientation matching

Oriented multigrain

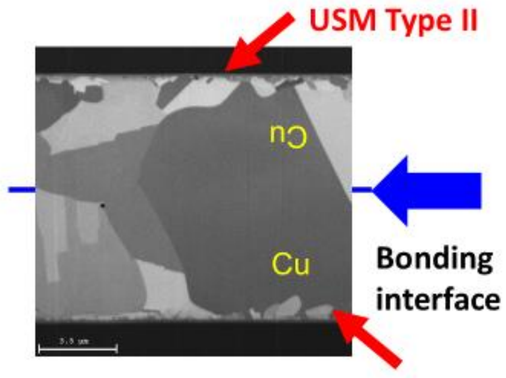
JCU

Under Seed Metal (USM)

USM Type I

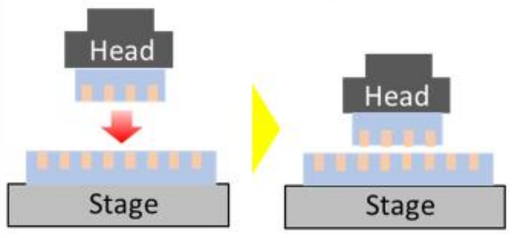


USM Type II



Tohoku's Hybrid Bonding Activity in ECTC2024

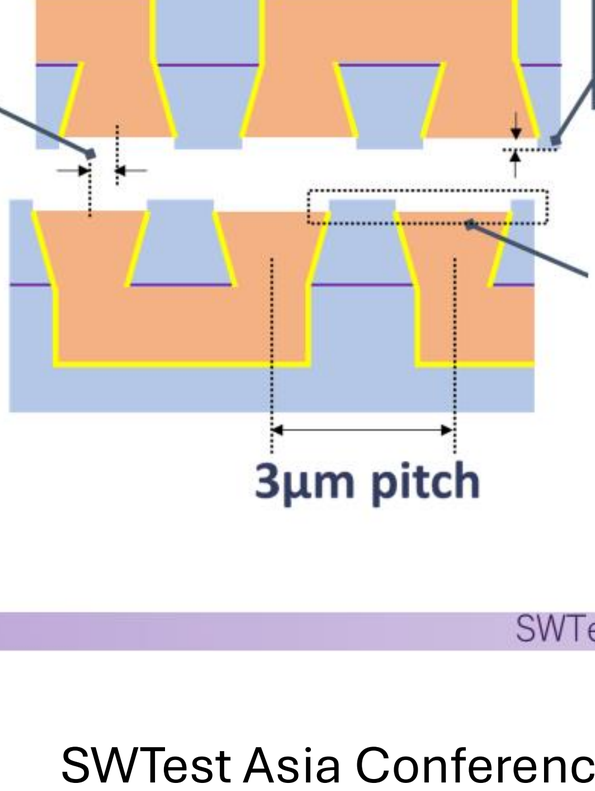
1.Bonding Equipment



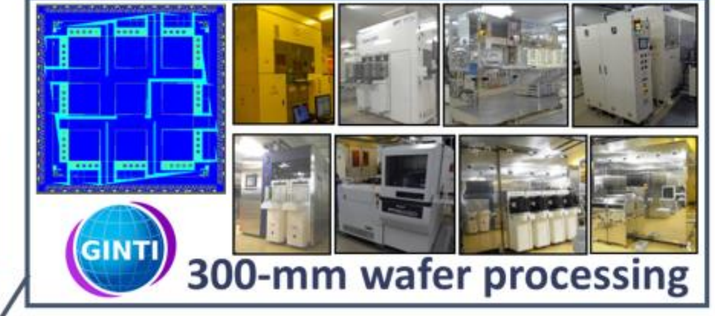
Submicron-level bonding accuracy

'TORAY' Toray Engineering

3-μm-pitch Chip-to-Wafer hybrid bonding is completed



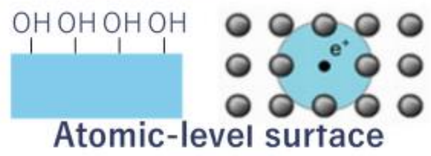
2.Design & Fabrication



GINTI

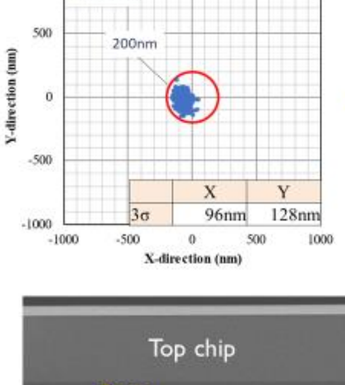
300-mm wafer processing

3.Surface Activation



Atomic-level surface control

YNU YOKOHAMA National Univ. Univ. of Tsukuba



FC bonder ±200nm @3σ