POSTER #

Testing AI chips and KGD at wafer-level: A new approach for full content test in wafer probing

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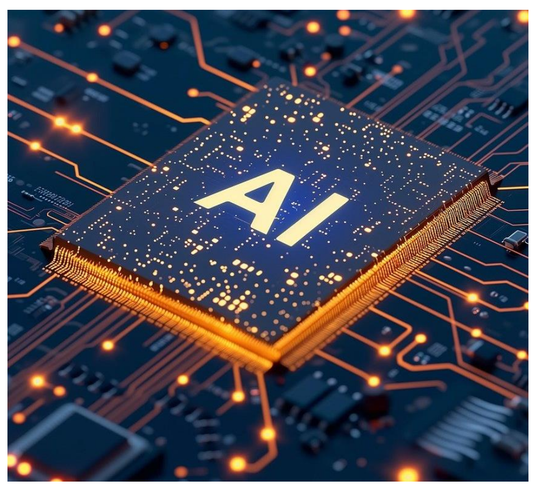
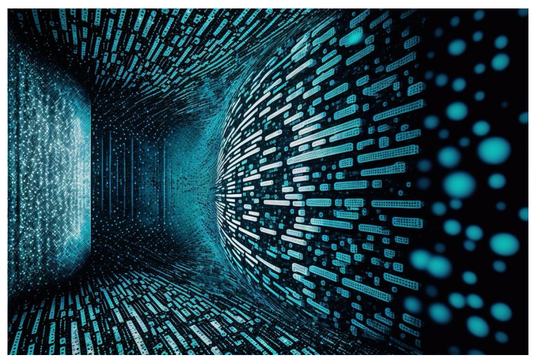
Introduction

- Social Networks, Big Data and Artificial Intelligence require a huge amount of the highest performing CPUs and GPUs
- In combination with Advanced Packaging, Known Good Die (KGD) is an essential demand
- Running a full content test on these chips is associated with enormous power loss and which will create a lot of heat in the DUT
- As the power will change very fast, the temperature of the chip will follow, even with a constant DUT backside temperature





The Fundamental Difference Between Single Die Test And Wafer Test

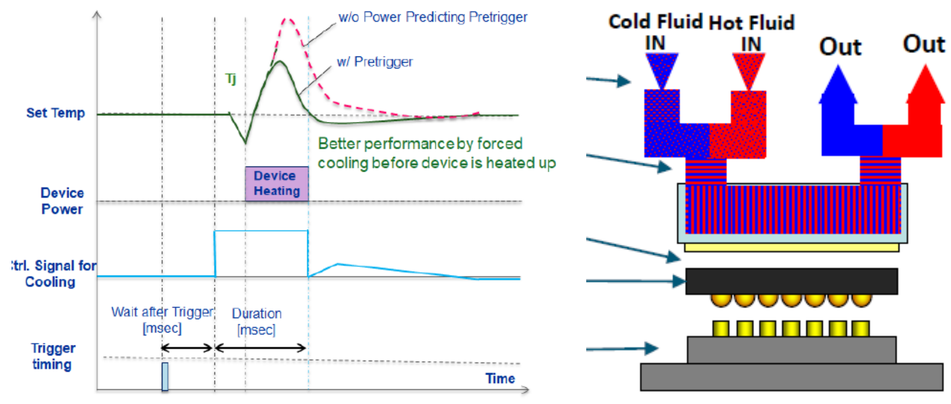
Single Die Test

In final test, low thermal mass of the temperature transmitter allows very fast thermal transitions:

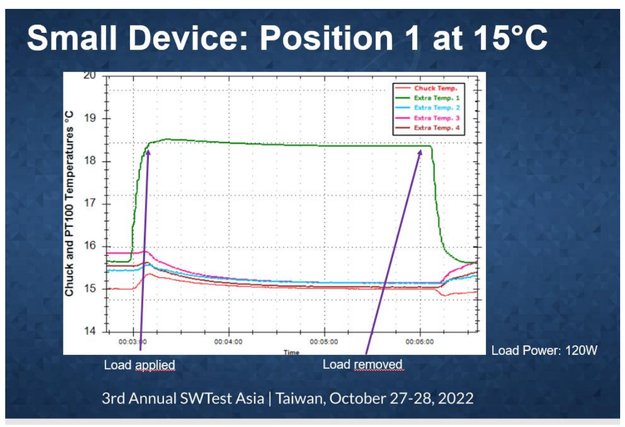
VS

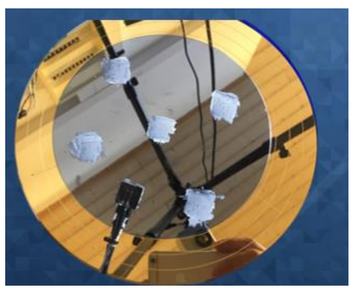
Wafer Test

In wafer test, large thermal mass prevents rapid temperature change of the chuck:



Armstrong, D. «Our Best-Known Methods for the Testing of High-Power Ics», Too Hot to Test Workshop, 2021

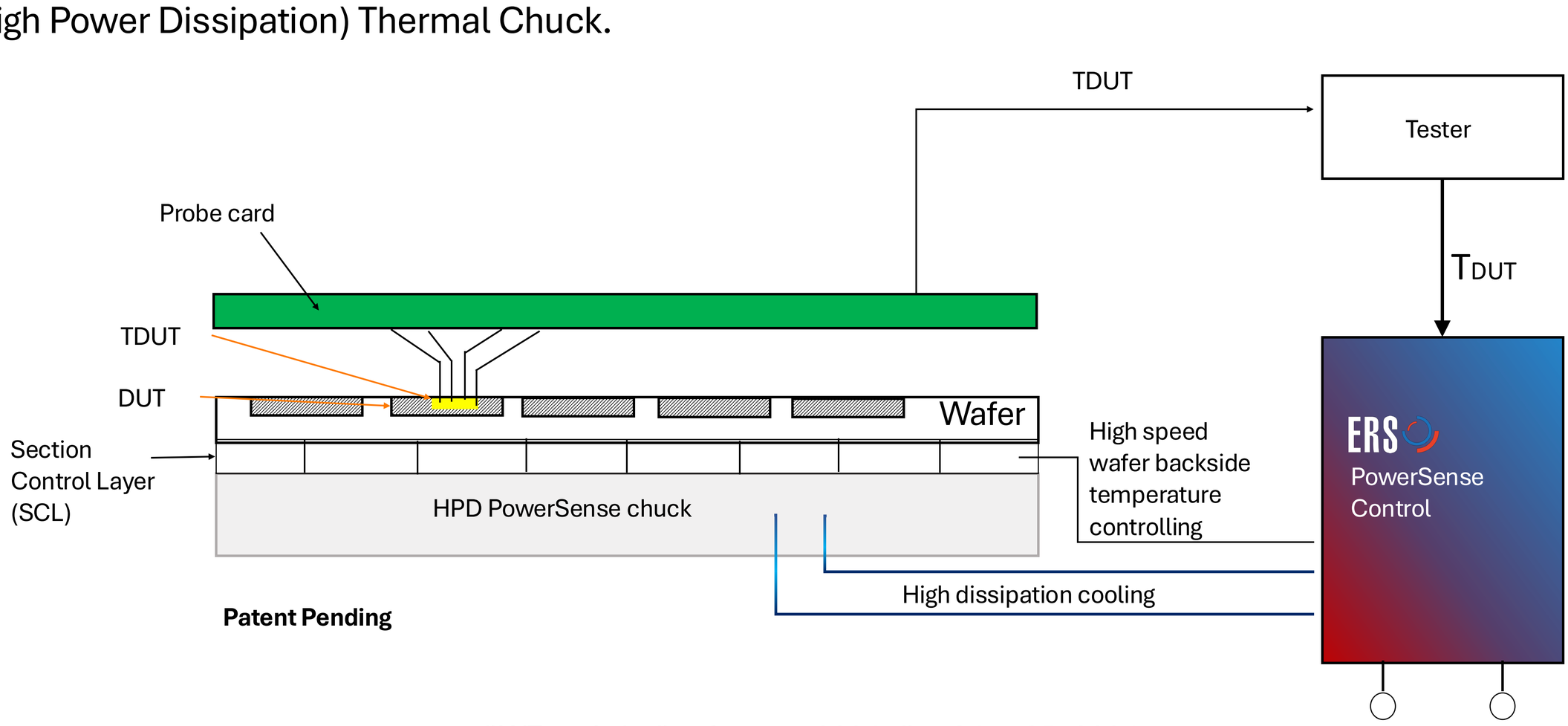




Reitinger, K., «High wattage dissipation under temperature – a new method for test evaluation», SW Test Asia, 2022

New Concept For Wafer Test

The key of the new method will be a very dynamic heating element with isolated sectional sensor and controlling capability (means individually controlling the temperature below each die) integrated in a HPD (High Power Dissipation) Thermal Chuck.



Patent Pending

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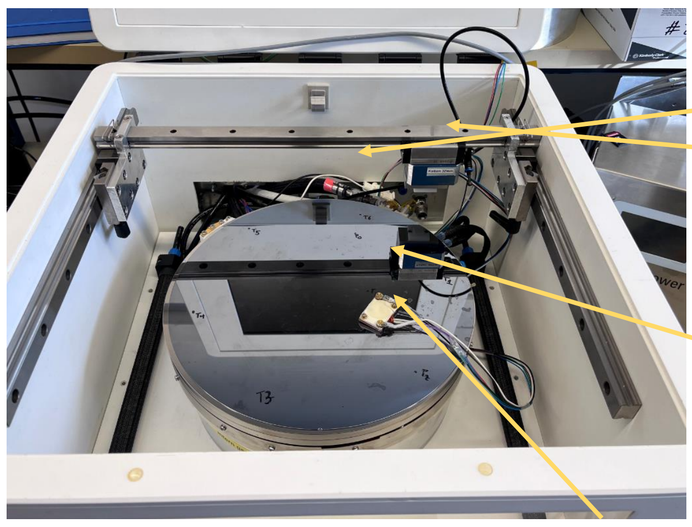
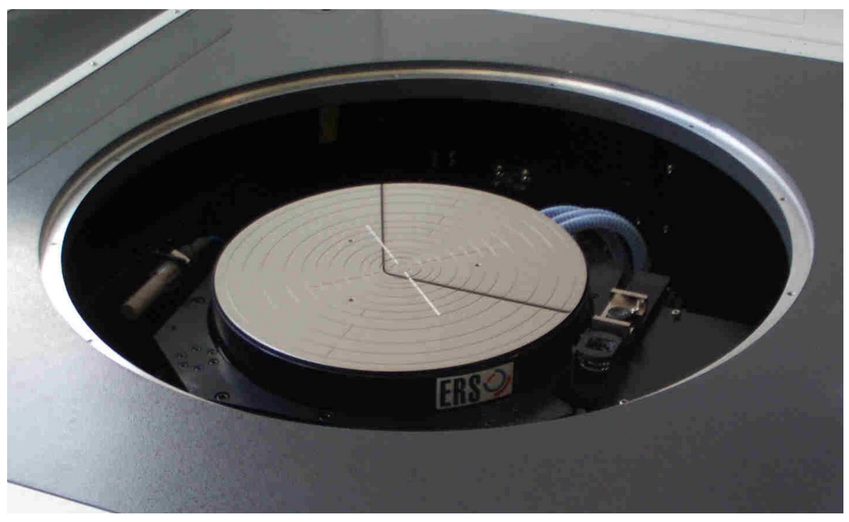
Test Set Up:

Workbench Test

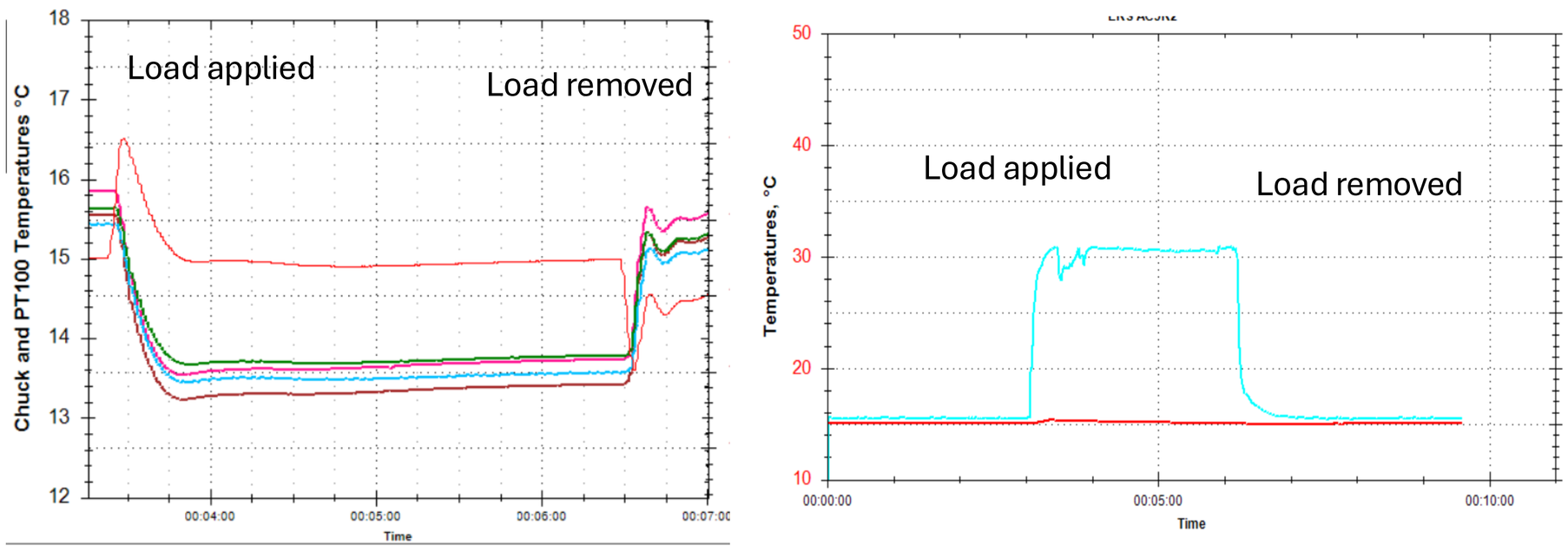


Chuck in Auto Prober



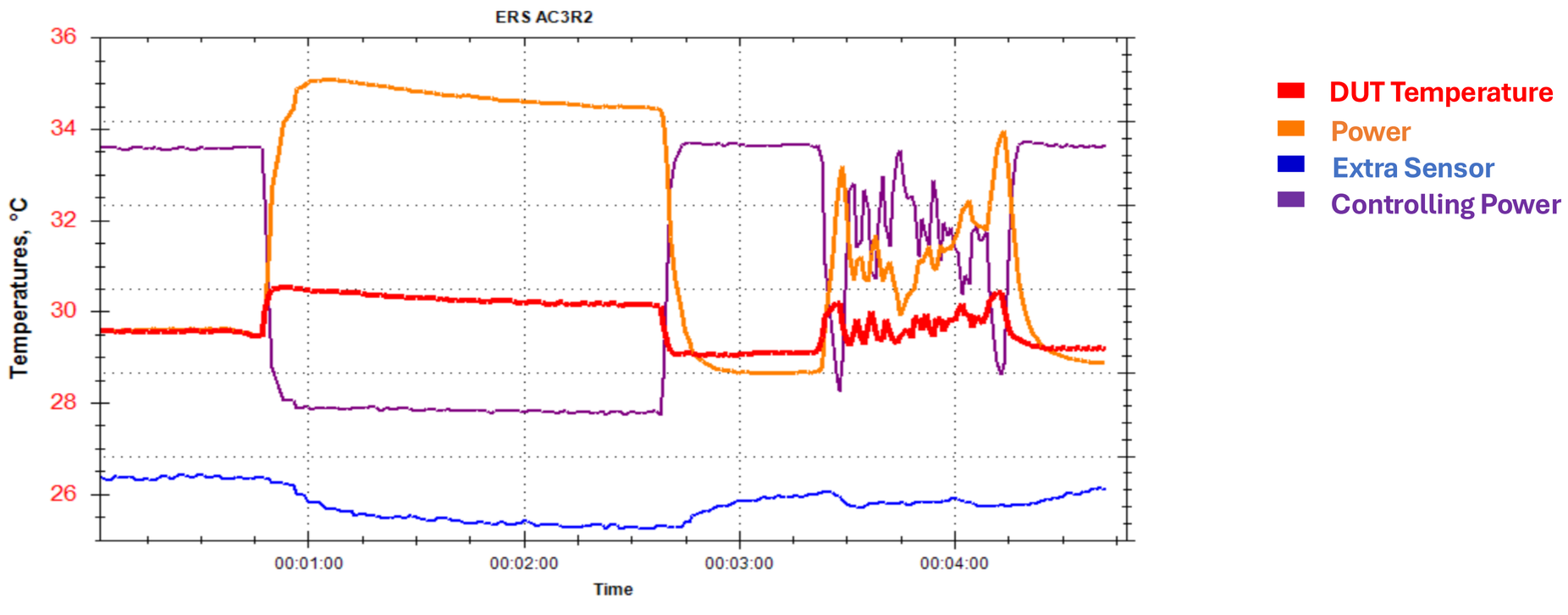
Results:

Temperature Controlled by Chuck Only



Temperature Difference DUT Power OFF – ON = 32-15 = 17°C

Temperature Controlled By Section Control Layer:



Temperature Difference DUT Power OFF – ON = 35-30 = 5°C

POSTER #

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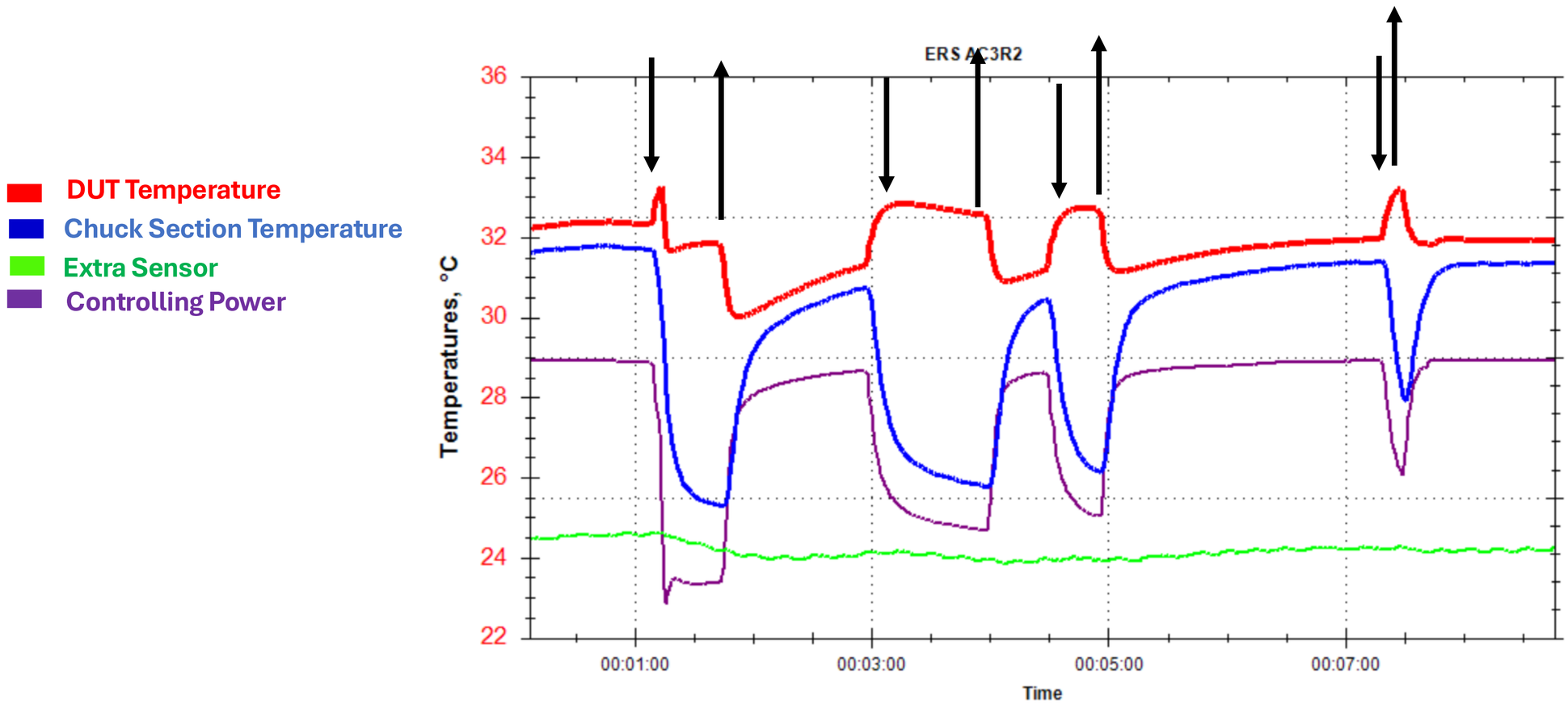
Temperature Controlled By DUT:



Temperature Difference DUT Power OFF – ON = 33,1-30,5 = 2,6°C

Discussion:

- With sectional temperature control, DUT backside can change temperature quickly (like in singulated die test)
- With DUT thermal control, thermal resistance can be compensated
- Maximum Power per section is about 600W at the present, bundling of sections may allow significant higher power dissipation
- Full temperature range -40°C up to +150°C can be used
- Integration effort into fully auto prober has potential to be made more seamless

High Power Dissipation

Follow On Work:

- Second generation of chuck system under evaluation now, will address higher power dissipation up to 1kW for a small and 2kW for a larger die
- DUT temperature controlling will be improved
- Full temperature range -40°C up to +150°C in preperation
- Smarter integration into prober

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