# Advanced DUT protection during Avalanche testing on wafer level

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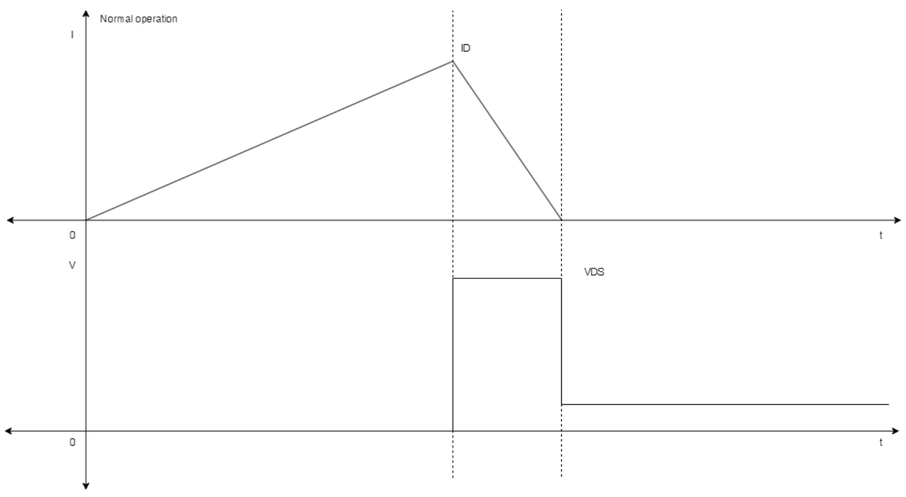
## Introduction

There are several methods how to perform avalanche stress testing on power semiconductors. Most common tests are Unclamped Inductive Switching (UIS) and Unclamped Inductive Load (UIL). Both of them combine forcing of high voltage and current to the device under test (DUT). During testing on wafer, this accumulated avalanche energy can be released not only through the predefined path to the DUT but in case of failure of the DUT, also through adjacent die (dice) and cause a damage to the prober card or to a wafer chuck. UNITES has developed advanced active protection which can send the accumulated energy through a parallel path and at the same time clamp the increasing voltage at the predefined limit. With this combination the accumulated avalanche energy is safely discharged through the parallel path and no harm is caused to the surrounding die or a wafer chuck.

## Avalanche testing – basic terms

- Single pulse avalanche current IAS
  Single pulse avalanche current "IAS" means the maximum current capacity under break down condition. If avalanche current exceeds it, the device can be broken regardless of channel temperature or energy.
- Single pulse avalanche energy EAS
  The avalanche energy "EAS" that shown on datasheet is the maximum guaranteed value calculated from the defined "IAS" and channel temperature. Therefore, the avalanche energy also changes according to the avalanche current. Avalanche energy is calculated as following:




$$E_{AS} = \frac{1}{2} . L . I^2{}_{AS} . \frac{B_{VDSS}}{B_{VDSS} - VDD}$$

*$B_{VDSS}$ : Break down voltage*
*$I_{AS}$ : Single pulse avalanche current*

## Avalanche testing – problems (in general)

**Avalanche testing -> Hard-switching (high energy) - can be be a destructive test!**

- If the device has some manufacturing defects, the Avalanche test can destroy not just the device but in case of testing on wafer, also **surrounding devices (dice) and the wafer chuck**

**Additional costs**

- This fact leads to additional costs for maintenance and decreasing the overall yield of a wafer fab

**Solution**

- To implement a safety feature on a tester **to prevent surrounding dice and chuck damage**

## Avalanche testing – problems (closer look)

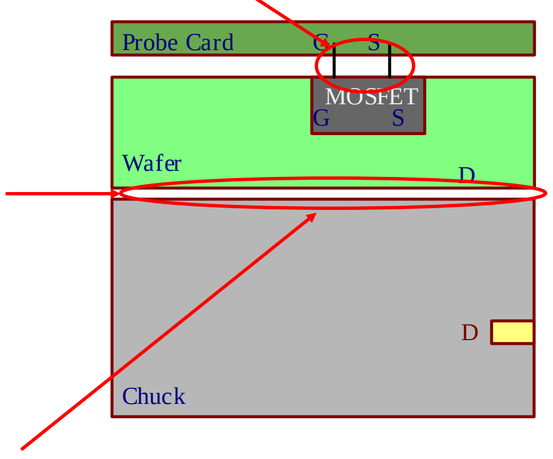
**Higher resistance between the probe tip on the probe card and a die on the wafer – caused by in time by probe wear due to contacting**

- This fact subsequently creates higher voltage between the probe tip and the probe die -> arcing effect
- The more often arcing occurs the worse this effect is
- This can lead to excessive damage of completely OK wafer

**Higher resistance between the wafer and the chuck – caused by improper vacuum suction on the chuck or chuck gold plated layer wear**

- This fact subsequently creates higher voltage between the wafer and the chuck -> can create sparks, or burned spots on either chuck or wafer during the avalanche test

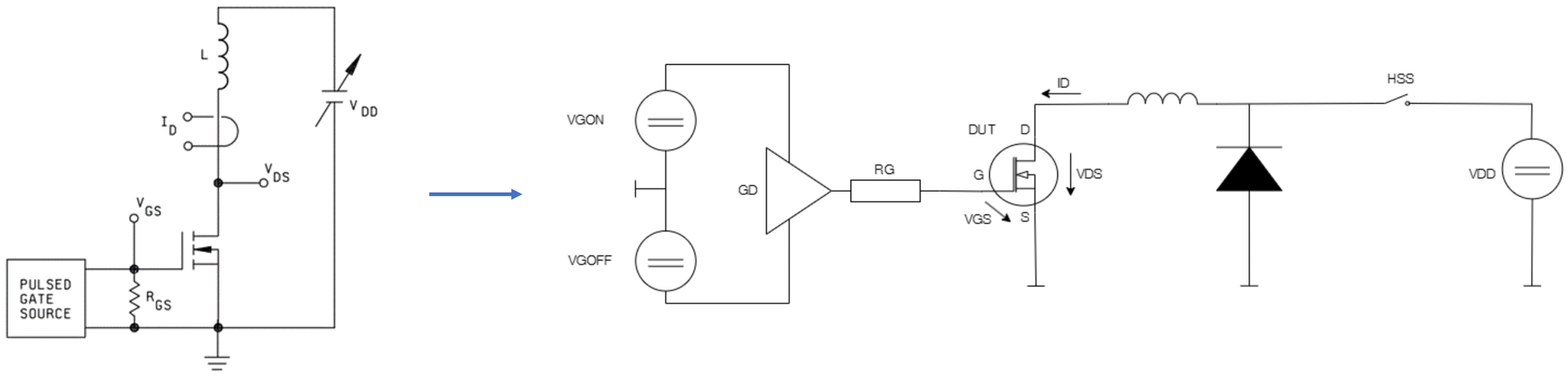
**Uneven conductance between the wafer and the chuck – usually happens on already worn off chuck on which is the gold plated layer damaged**



# Principle of avalanche DUT protection

- **Test methods for avalanche testing**

  In order to implement the parallel energy path, the existing MIL-STD-750, 3470.2 test method for avalanche testing has to be improved (as shown on the schematics below).

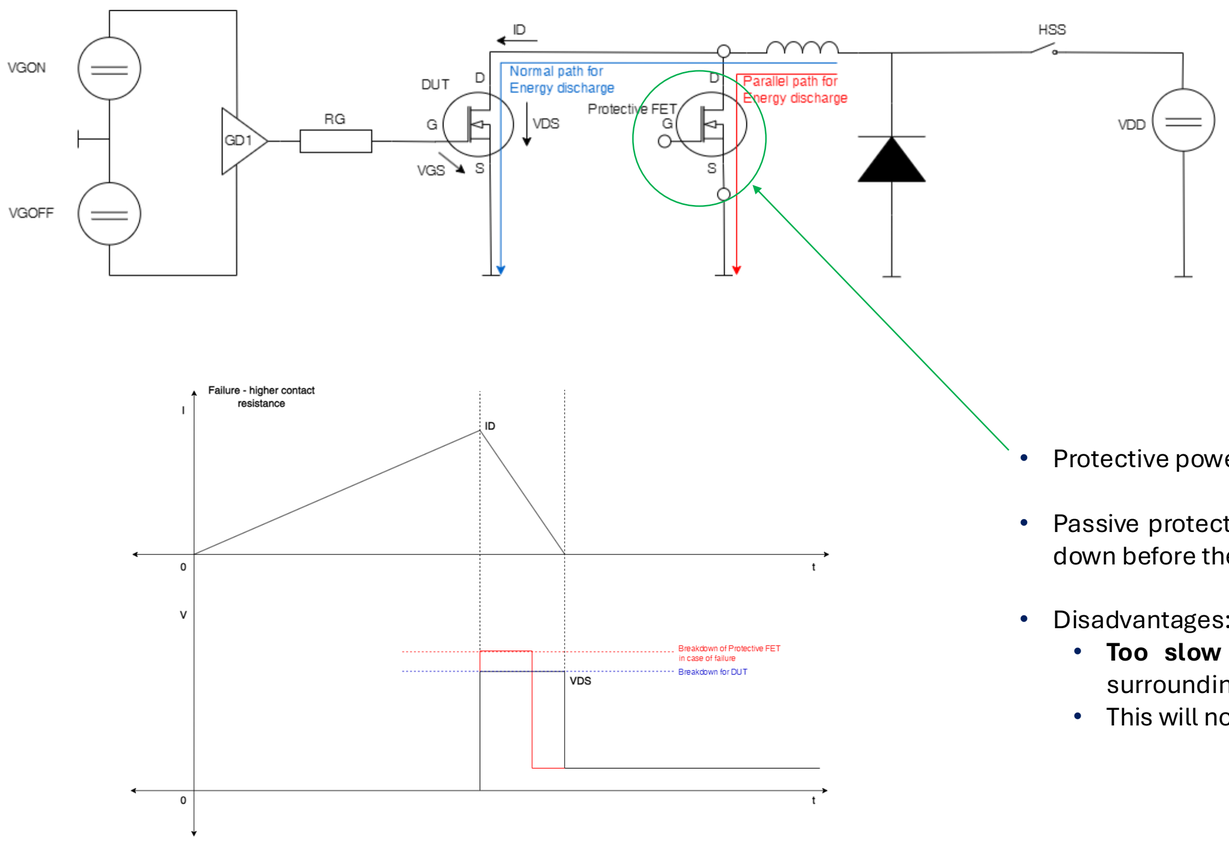



*Test method 3470.2 according to MIL-STD-750*

*Effitest Power UIL test method*

- **Principle of basic DUT protection**

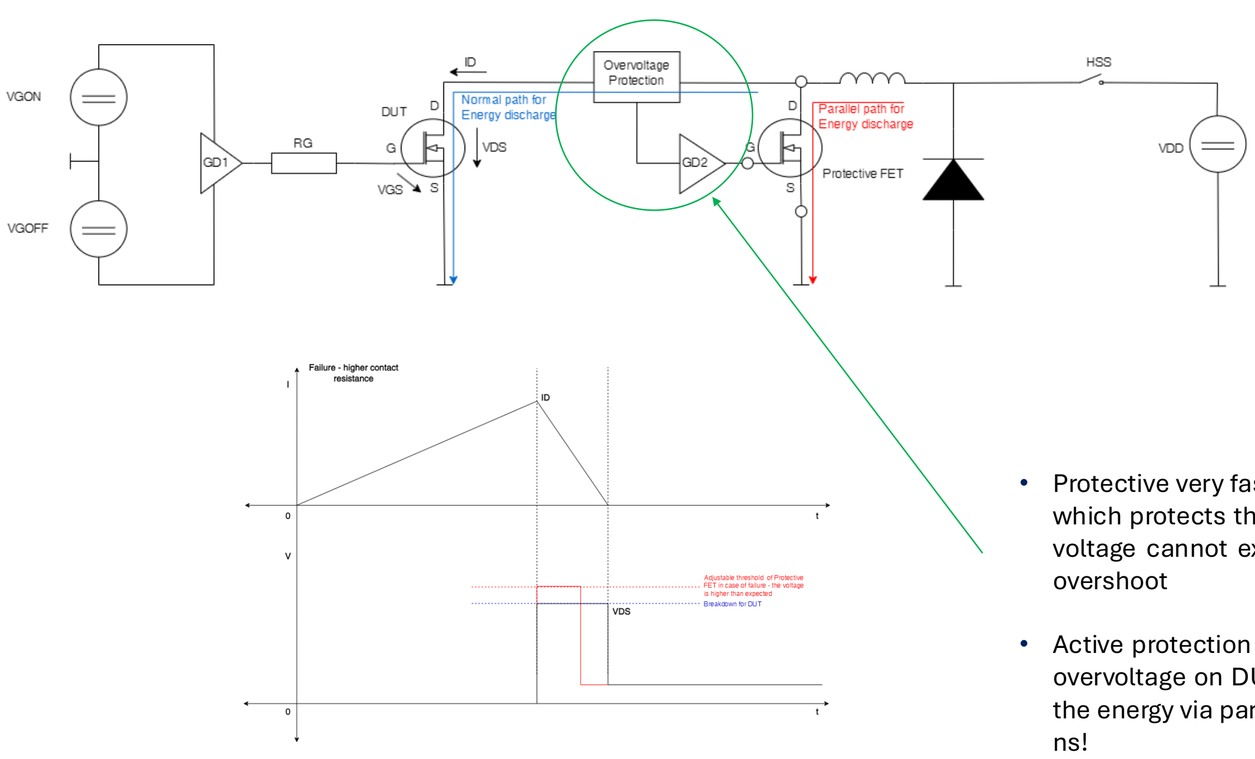
  Creating parallel energy path with power FET with fast switching




- Protective power FET (with higher breakdown) in parallel to DUT
- Passive protection – higher breakdown than the DUT -> the protective FET breaks down before the voltage can increase to a dangerous level
- Disadvantages:
  - **Too slow (>300ns)** – transient will happen and it can still damage the surrounding dice
  - This will not prevent the creation of residual random arcs in the original path

- **Principle of advanced DUT protection**

  Creating parallel energy path with SiC FET with fast switching and fast overvoltage detection

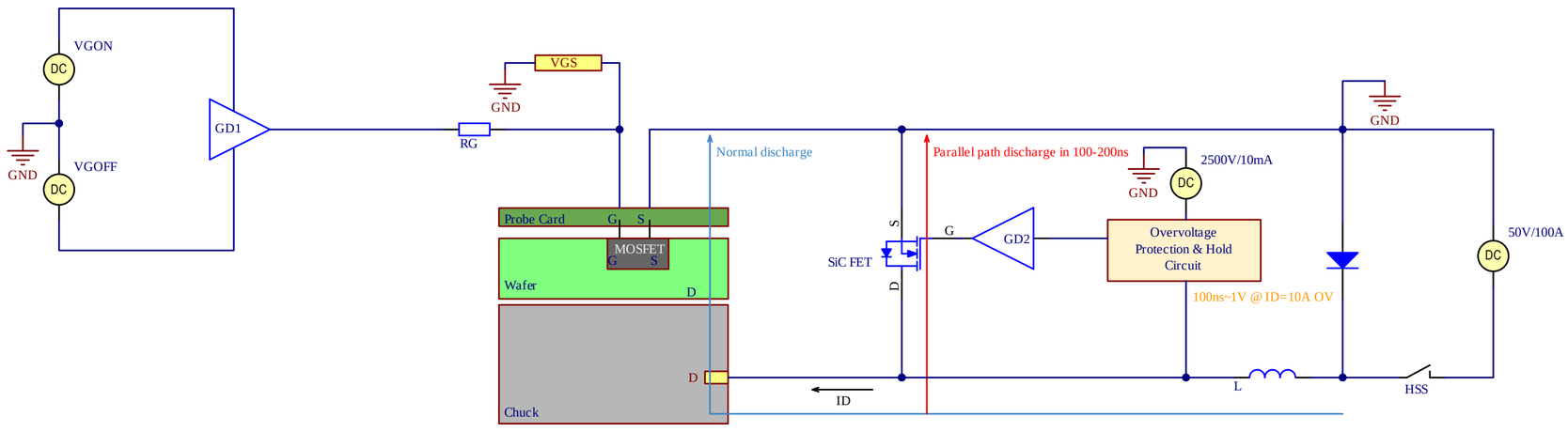


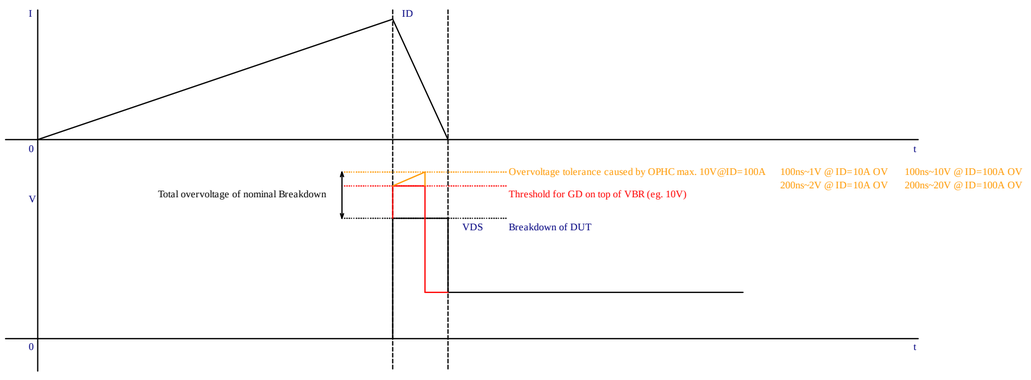

- Protective very fast SiC FET in parallel to DUT and programmable Gate Driver (GD2) which protects the DUT in case of failure. Together with Overvoltage protection the voltage cannot exceed more than 10% of the set limit – there will be no voltage overshoot
- Active protection – Protective FET is switched-on by the GD2 in case of failure (eg. overvoltage on DUT); the voltage threshold is adjustable in SW SCADUS – red line; the energy via parallel (Protected FET) path needs to be discharged in less than 300 ns!

# Results – implementation of Avalanche protection

- **Implementation and further improvement of Advanced protection**

  Creating parallel energy path with SiC FET and holding the Avalanche Energy. The advanced principle is to create not only Parallel energy path but also hold the Energy until the parallel path is fully open




**Theory of operation with example**

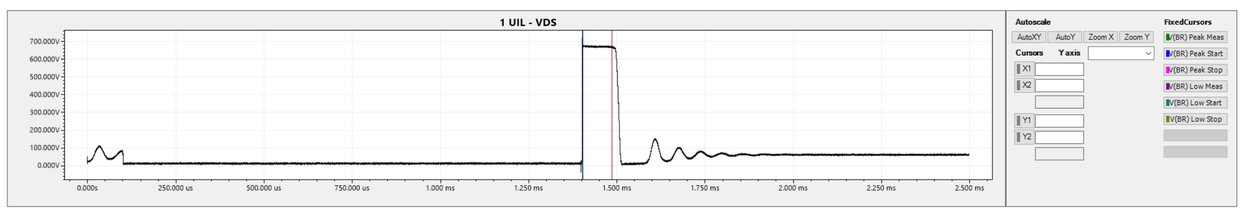
1. Set the threshold to 10V (above the nominal device breakdown, e.g., 1250V), so the threshold will be 1260V.

2. If the ID = 10A and the overall time it takes to switch on the parallel energy path is, e.g., 150ns, then the Overvoltage Protection & Hold Circuit (OPHC) will hold this energy with an increase in voltage of 1.5V over the set threshold.

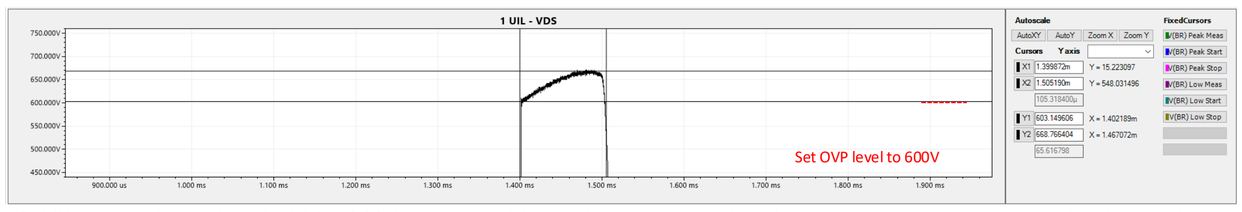
3. The maximal voltage overshoot will be 1261.5V until the parallel energy path is switched on.

4. The accumulated energy will discharge through the protective MOSFET

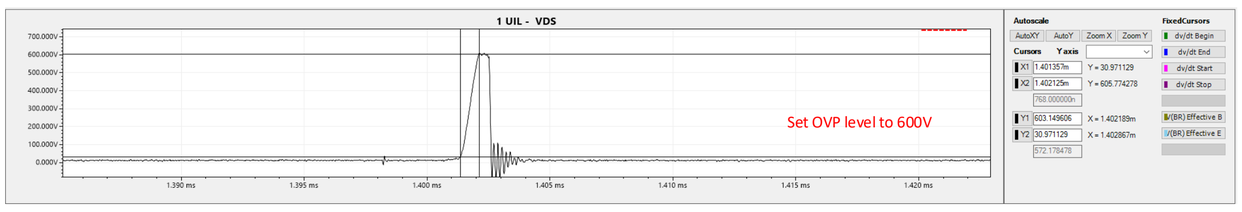
- **Measured results**




1. UIL test without any OVP level threshold – 650V nominal breakdown




2. UIL test with set threshold for 600V without additional protection – detail on increasing voltage over the threshold




3. UIL test with set threshold for 600V with additional protection – won't get over 600V, no increasing voltage

1) Waveform with normal UIL breakdown of the DUT - 650V

2) Waveform with capacitance bank (OVP protection) but without additional gate driver to switch the parallel path – detail – 65V over the threshold

3) Waveform with capacitance bank (OVP protection) with additional gate driver to switch the parallel path – detail – no voltage above the set threshold

# Conclusion

**Avalanche testing -> Hard-switching (high energy) - can be a destructive test!**

But can be eliminated by using parallel path of the Avalanche energy

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**Additional costs**

Reduction of additional costs of new plate layers on chuck or new probes on a probe card

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**Solution**

Recommendation is to use Automatic Test Equipment (ATEs) with such protection (STOP function)

# Contact information


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