SWTEST ASIA
PROBE TODAY, FOR TOMORROW

A Cost-Effective Test Solution for Parametric Test & Reliability Lab

Chroma Advancing Excellence x CELADON A Wholly Owned Subsidiary of MPI CORPORATION

Author Details

Ching-Too Chen
Adam Konicek
Jeff Gruszynski
Jonathon Lee
Chintankumar Patel

5th Annual SWTest Asia | Fukuoka, Japan, October 24 - 25, 2024

Parametric Testing Ecosystem from 2009 to 2024

Presentation in SWTest 2009

DC Production Parametric Testing Overview

Upwards of 1000 facilities worldwide do semiconductor wafer processing. Around 2000 parametric testers are used in those sites, 750 of which are obsolete. That is, the system vendor has stated they no longer provide new versions, no longer update software, and will only repair on a best-effort basis.

Reedholm 8/2009

Technology Drives Innovations & Demand

HP 4062

Keysight 4070

Keysight 4080

Technology accelerates phasing out Legacy Models

Presentation in SWTest Asia 2024

1,515 facilities worldwide in 2024

2023 - 2024 26 New Fabs Build
2024 - 2030 58 New Fabs Builds
2024 - 2027 19 Advanced Fabs (≤10nm)

More than **1,000** new systems demand in the market
Request for the **cost-effective & innovative solutions**

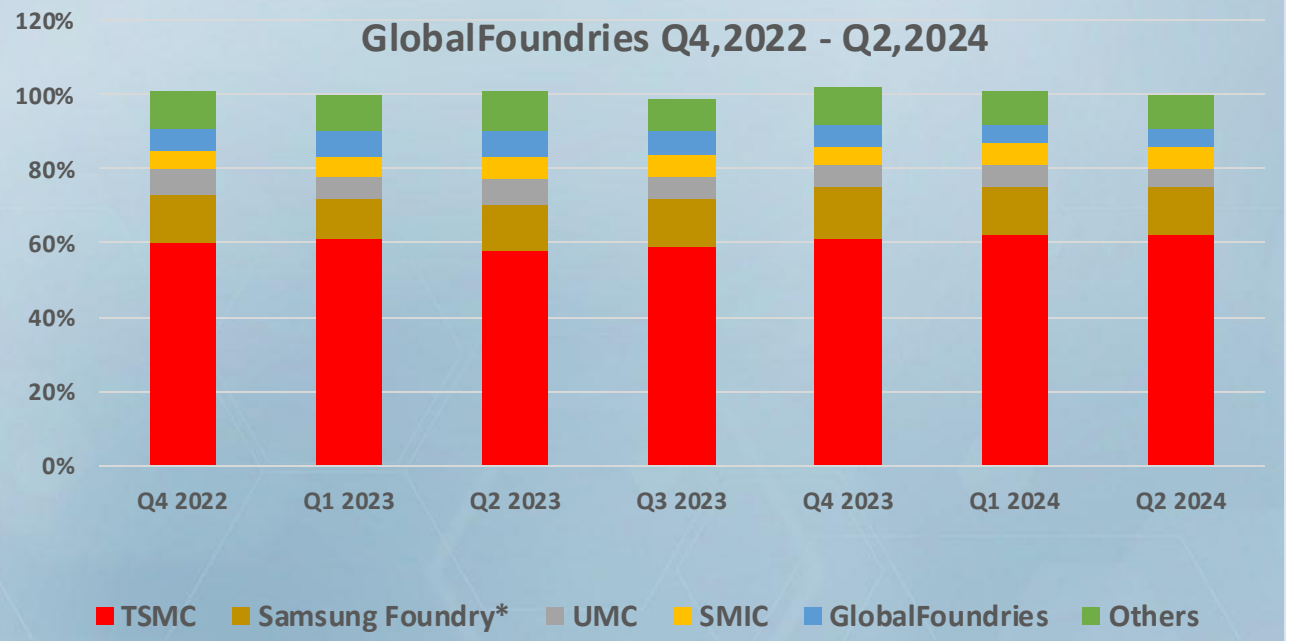
300mm Fab Outlook to 2027, 3Q24 (September 2024) Update, Published by SEMI

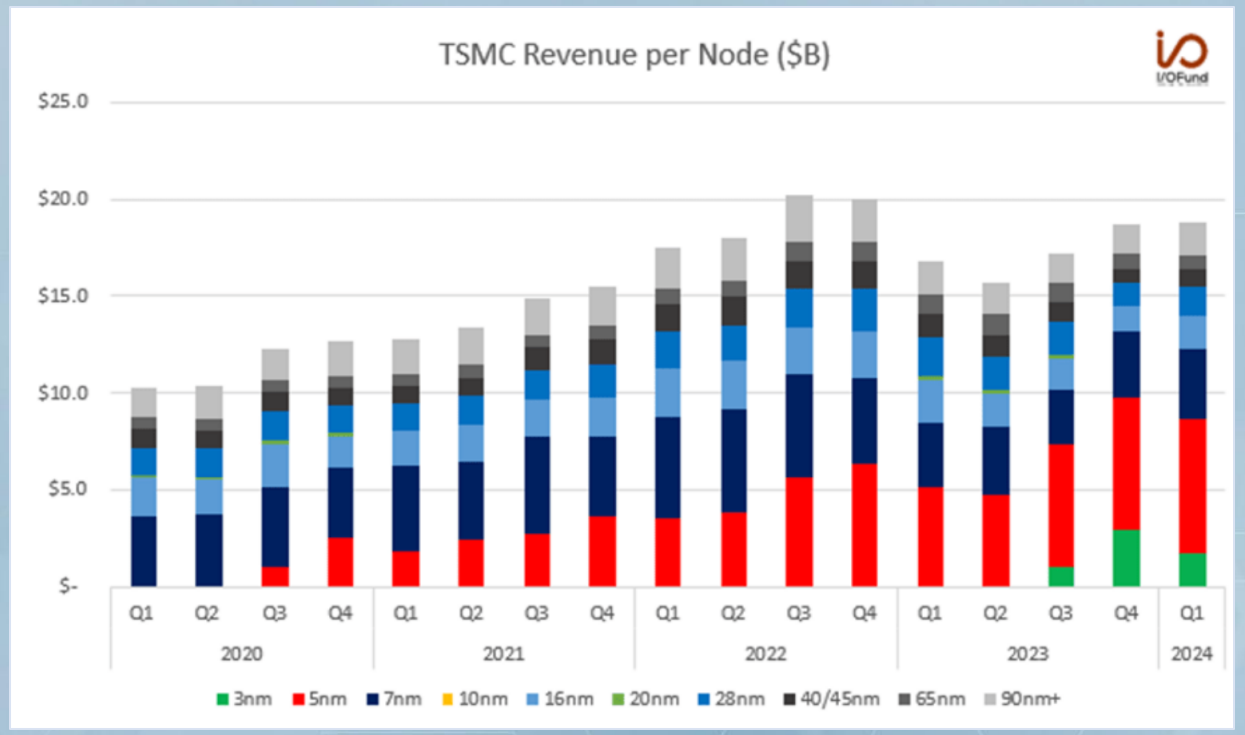
300mm Equipment Spending

Will Reach to $123.2B in 2025 and $140.8B in 2027

Total $400B from 2025 to 2027 ***Semi Report 9/26/24***

More than 40% of Global Foundry are in Advanced Nodes in 2024





Beth Kindig June 04,2024 Tech Inside Network / Seeking Alpha

TSMC's advanced nodes (3nm to 7nm) contributes 65% of revenue of Q1, 2024

TSMC owns market shares from 59% to 62% in Global Foundries between Q4 2022 and Q2,2024

19 New Advanced FABs Are Being Built Between Now and 2027
About Total $286 Billion

The World 's Most Advanced Semiconductor Fabs (10nm- 1.4nm) Being Built till 2027					
Company	Start Date	Investment (USD Billion)	Time for Completion	QTY of Plants	Location
Intel	2021-2022	20	2025	2	Arizona, US
	1/21/2022	20	2026	2	Ohio, US
	3/15/2022	36	2027 (Postpone)	1	Magdebury, German
Micron	10/4/2022	20	2025 -2026	1	New York, US
	9/1/2022	15	2025 -2026	1	Idaho, US
	2022-2023	5	2025-2026	1	Hiroshima, Japan
Rapidus	2023 - 2024	17	2027	1	Hokkaido, Japan
	2025-2026	20	2027	1	Hokkaido, Japan
TSMC	12/6/2022	20	2025	1	Arizona, US
	2024-2025	20	2026-2027	1	Arizona ,US
	2024-2024	12	2025	1	Kaohsiung, Taiwan*
	2024-2024	12	2026	1	Baoshan, Taiwan*
	2025-2025	12	2027	1	Taichung, Taiwan*
Nanya	6/23/2022	10	2025	1	New Taipei, Taiwan
Samsung	11/24/2021	17	2024-2025	1	Texas,TI
	2020-2021	20	2024-2025	1	Pyeongtaek, S Korea
SK Hynix	9/6/2022	10	2025	1	Cheongiu, S Korea
Total		286		19	Cheongiu, S Korea

**** Estimated Number***

Note: Modified from Z2Data Solution published on April 11,2024 and Semi Report (logic and memory total $293 B) on 9/26/24

Estimate from now to 2027

19 Advanced Nodes Foundries (FAB)
5 - 8 SiC/GaN/ Power FABs
16 – 22 Foundries & FABs

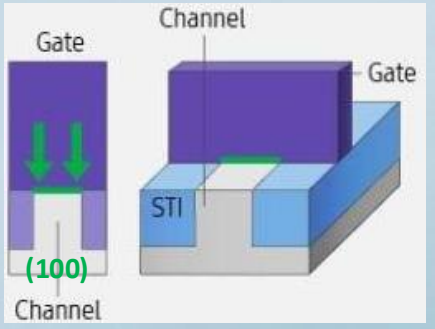
More than 1000 Labs need to be upgraded

Advanced Process foundry capacity by region

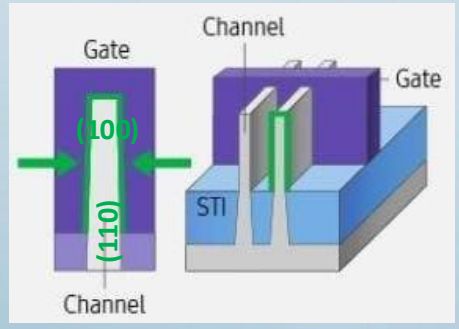
Advanced	2022	2024	2027
TW	70%	66%	55%
KR	11%	11%	8%
US	10%	10%	22% ★
JP	0%	0%	3%
CN	8%	9%	6%
Others	0%	4%	5%
Total	100%	100%	100%

Source: TrendForce, Apr., 2024

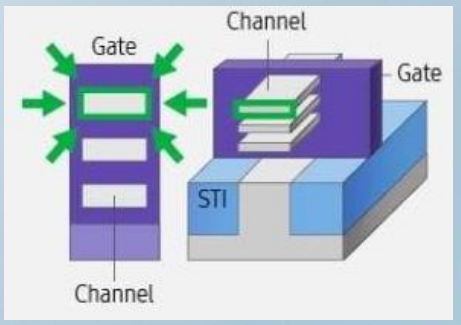
Technologies Require Innovations in FABs



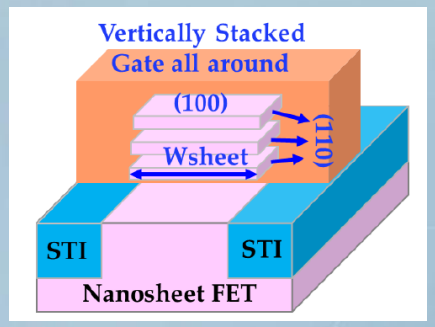
Planar FET
1 Gate on channel

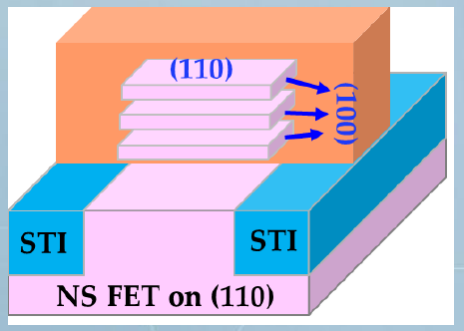


FinFET
3 Gates on channel



Gate-All-Around
4 Gates on channel





GAA Nanosheet FET's (100) and (110)
Conduction Surfaces Orientation – [3] Wang, M

	Planar FET	FinFet	GAA FET
Logic Nodes	> 22nm	22nm- 3nm	3nm - 1nm
Logic Transistor Density Million Transistors/mm square	15.3 - 16.5 (22nm) Intel	130 - 170 (7nm) Samsung/TSMC	330 (2nm) IBM
Failure mode & Reliability Degradation examples for the different nodes and devices	Gate Leakage Currents* Short Channels Effects Quantum Tunneling Variability Mobility Degradation	Tolerance and buffer shrink** Short Channels Effects Need more area to increase speed Higher switching speed caused Dielectric breakdown, leakage and thermal damage	New Device Structure Corner field crowing effect Self-heat effect More conduction surface areas Inner spacer TDDB Si channel geometry
	*Ref: ED Sperling Dec 8, 2020 *Predicting Reliability at 3/2nm and beyond* **Semiconductor Engineering**	**Ref: Ann Steffora Mutschler 9/10/2020 *Dealing with device aging at advanced nodes* **Semiconductor Engineering**	[3] Wang, M. 2/13/2024 *A Review of Reliability in GAA Nanosheet devices* **Micromachines 2024, 15, 269**

Innovations come with New Challenges in Lab & FAB

	Planar FET	FinFet	Gate-All-Around FET
Logic Nodes	> 22nm	22nm- 3nm	3nm - 1nm
Logic Transistor Density Million Transistors/mm^2	15.3 - 16.5 (22nm) Intel	130 - 170 (7nm) Samsung/TSMC	330 (2nm) IBM
Hardware & Software Requirements for the different nodes and devices in Lab and Fab	Robust probe card Switch Matrix System = 48 pins External LCR Meter External Pulse Generator SMU @ 4%+ 504fA current accuracy LAB to FAB data reference	Low leakage & robust probe card High parallel test system > 24 pins CMU > 1-2 MHZ Pulse capability < 1uS to 100nS SMU < 1% + 100fA current accuracy LAB to FAB data correlation	Advanced probe card Higher parallel test System > 48 pins CMU > 10MHZ Pulse capability < 50nS SMU < 0.5% + 80fA current accuracy Software & Hardware integration

Celadon VersaCore™ Family

Applications

- Wafer-level Reliability (WLR)
- Modeling & Characterization
- Parametric Test from lab to production

VC20E™ Specifications

- Rated from -65ºC to 200ºC
- <5fA/V leakage @ 10s and 100V
- Ability to probe pads as small as 20x20µm

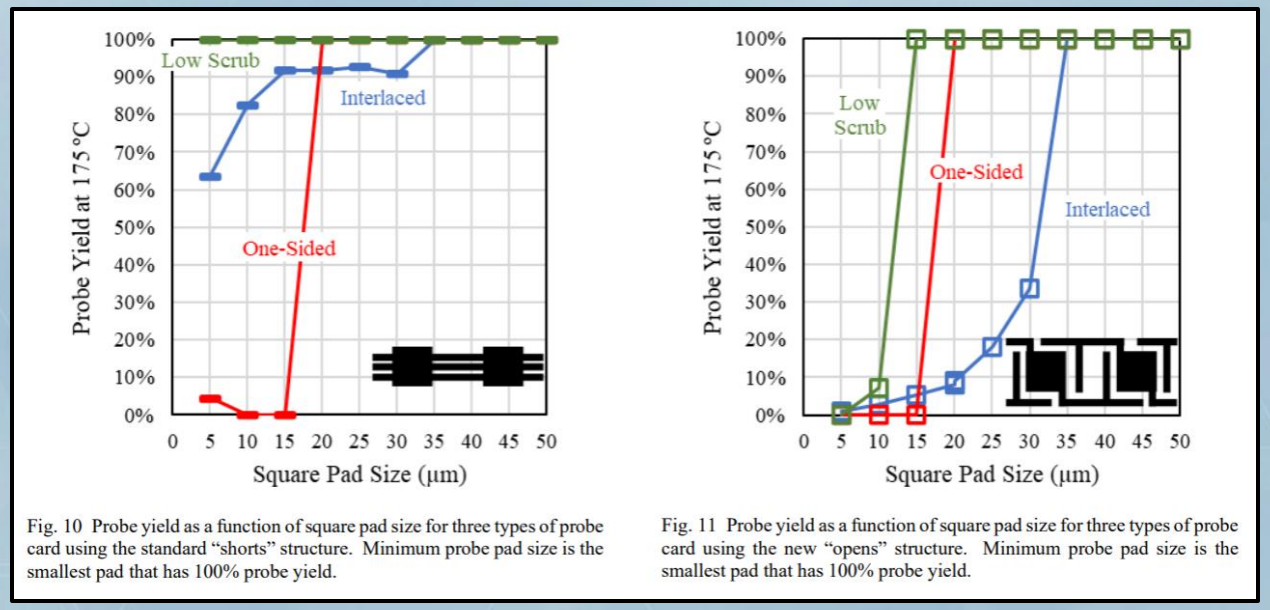
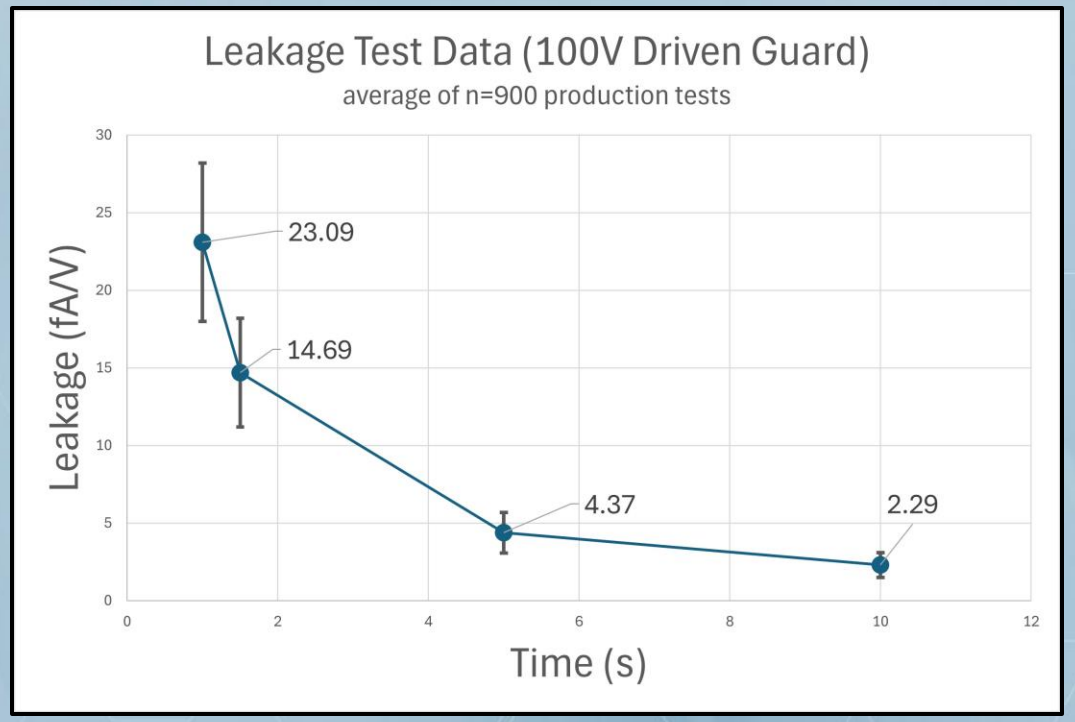


Fig. 10 Probe yield as a function of square pad size for three types of probe card using the standard "shorts" structure. Minimum probe pad size is the smallest pad that has 100% probe yield.

Fig. 11 Probe yield as a function of square pad size for three types of probe card using the new "opens" structure. Minimum probe pad size is the smallest pad that has 100% probe yield.

[1] Smith, Hall, and Tranquillo, March 2023

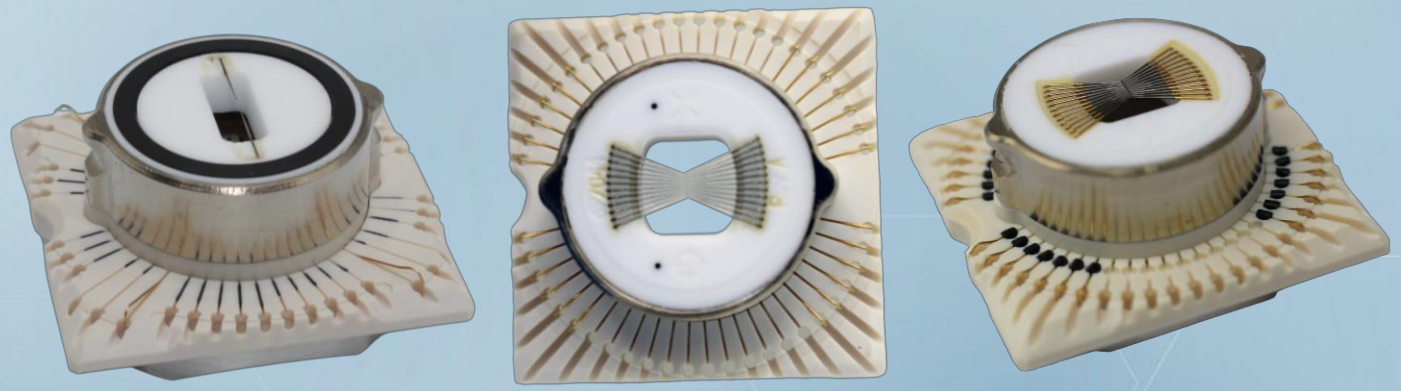


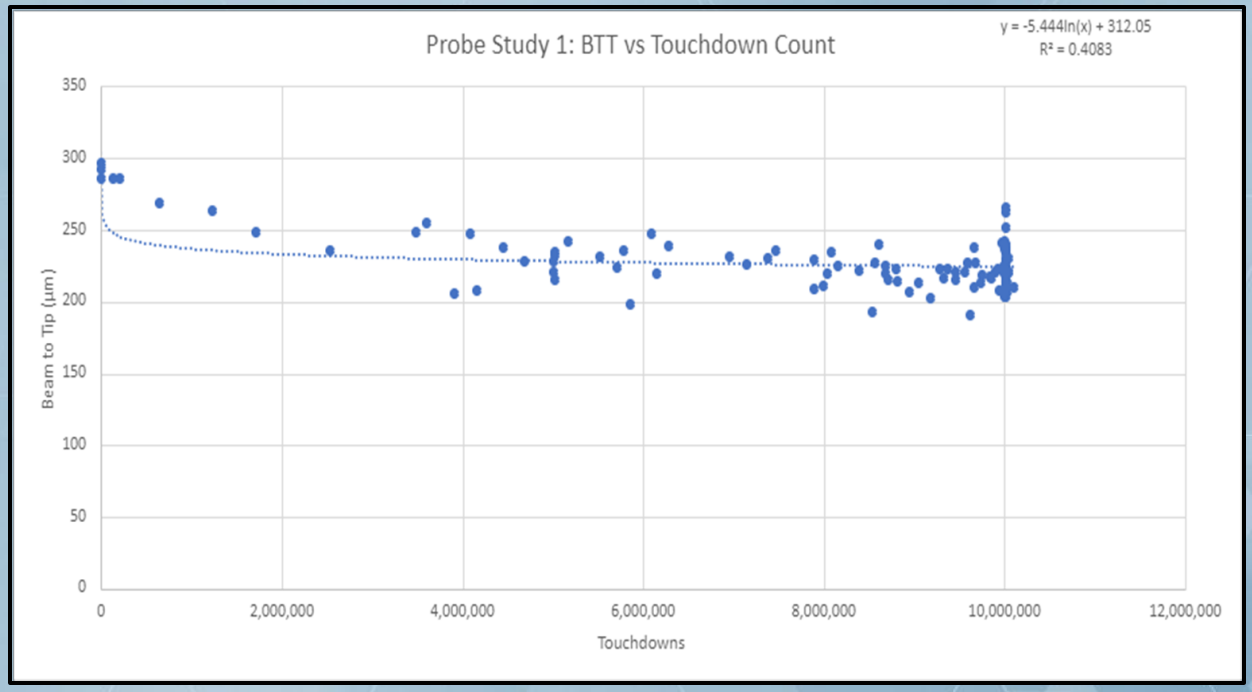
- 48 channels
  - Up to 104 channels with VC43E™
- 3kV option available
- Direct Dock and Cabled Out versions

VersaCore™: Reducing Cost of Test

Advantages

- Modular: many possible layouts, one common interface
- Lab to Fab: the same core can be used in both environments
- Robust: capable of 8-10 million touchdowns or more
- Repairable and rebuildable



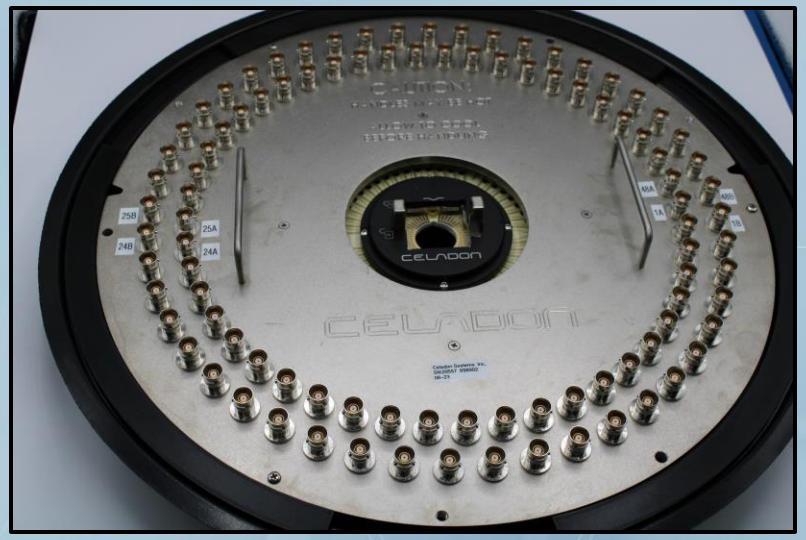


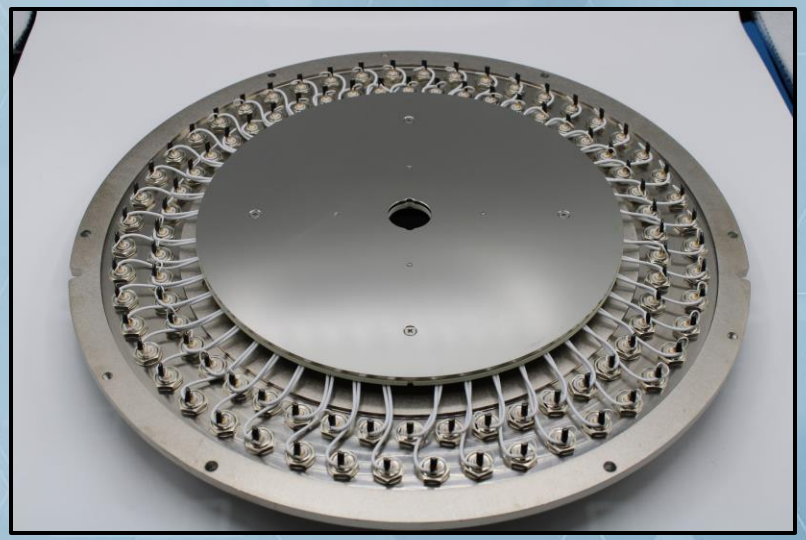
[2] Kaiser, Armendariz, and Hwang, August 2021

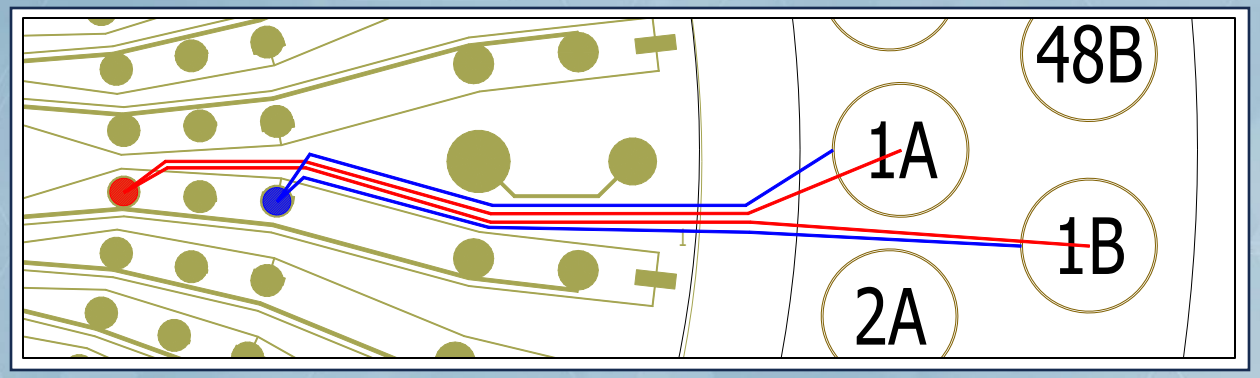
Celadon/Chroma Interface

Custom Probe Card Interface

- 96 triaxial BNC connectors for 48-channel Quasi-Kelvin measurements
- Heat shield for high-temperature testing
- Ample clearance for exchanging VC20E™ probe cards







Hyperion and Cost Impact

Value Proposition

- **Common Tool and Elements for Multi-Vendor Instruments**
  - Test plan
  - Test algorithm code
  - Data output format
  - Software interface
  - User Training
- **Controlling Variables between Test Systems**
  - Test System differences minimized – shorter time to data, decision, debug
  - Predictability of results on different test systems
  - Identify the correct cause of test problems quickly
  - Better Return on Assets/Resources

Experiment Overview

- **Hyperion Test Shell supports both the Chroma 3530 tester and various 19” rack parametric test instruments**

- **Hyperion structure**
  - Plug-in Architecture based on abstraction
  - Common core of API features for interoperability
  - Peaked special purpose API features with more limited interoperability (e. g. Fast BTI)

- **Goal of Experiment**
  - Claimed interchangeability must be validated with measurements on common set of devices on-wafer
  - Recent best performance instruments investigated
  - Legacy instruments are known to have vintage-defined limits

- **Results Summary**

Hyperion and Cost Impact

Value Proposition

Multiple Instruments and Wafer Probers supported

Vendor	SMU	CMU	PGU	FMU	Switches
Chroma	3530				Per-pin - N/A
Keysight	B1500A B1505A E5270A/B E5260A 4142B	4284A, E4980A	81xxA† 81xxxA†	53xxx†	E5250A B2200A 4084A/B
Keithley/Tektronix	4200 2600 2400	4200			707A/B

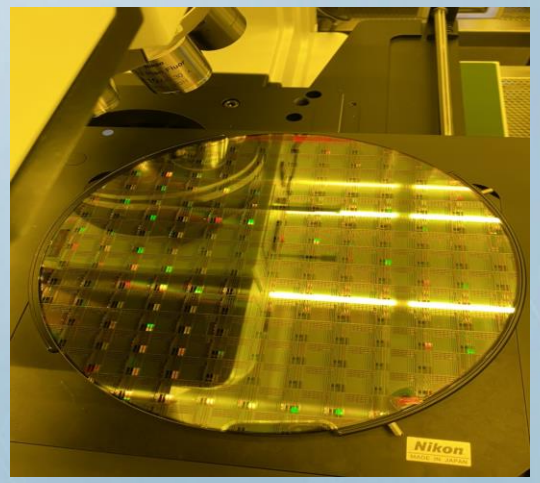
Vendor	Model
Tokyo Electron (TEL)	P8, P12, P12 Precio
ElectroGlas	4080, 4090
Accretech†	UF200, UF300, UF2000, UF3000
MPI	TS2000 (All SENTIO firmware models)
Cascade/FormFactor	All Nucleus and Velox firmware models

† Planned or under development

Experiment Design

- **Correlation of data from the same devices on-wafer (custom TSMC 1.9µm wafer for parametric validation)**

- **Comparative Algorithms**
  - SMU:
  - CMU:
  - Test Time



Chroma (TSMC) Test Wafer

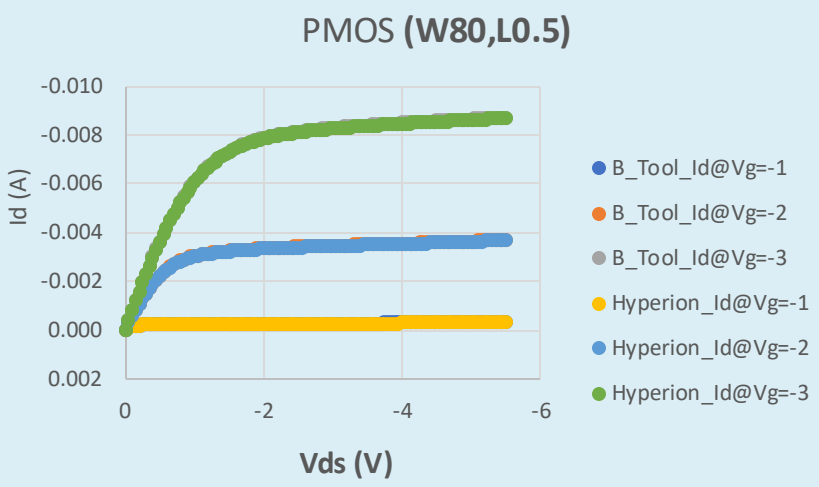
B_Tool and S_Tool are connected to Celadon Probe system (VC20)

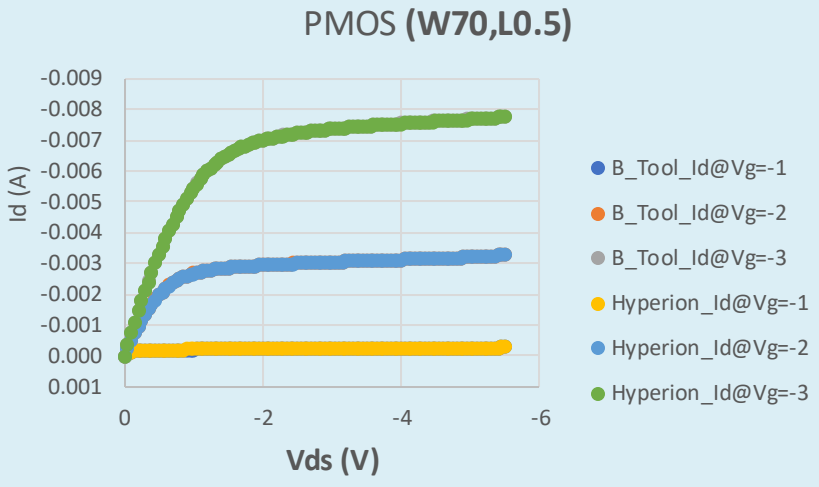
Hardware	Software		Algorithms			
Chroma 3530	Hyperion		SMU	I_d vs. V_{ds}	CMU	C_g vs. V_g
Keysight B_Tool	EasyExpert	Hyperion				
Keithley S_Tool	Clarus	Hyperion				

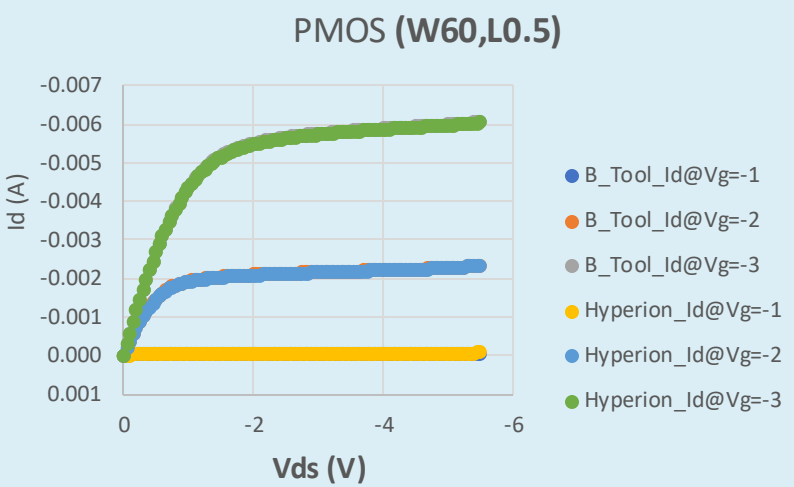
B_Tool EasyExpert vs. B_Tool Chroma Hyperion

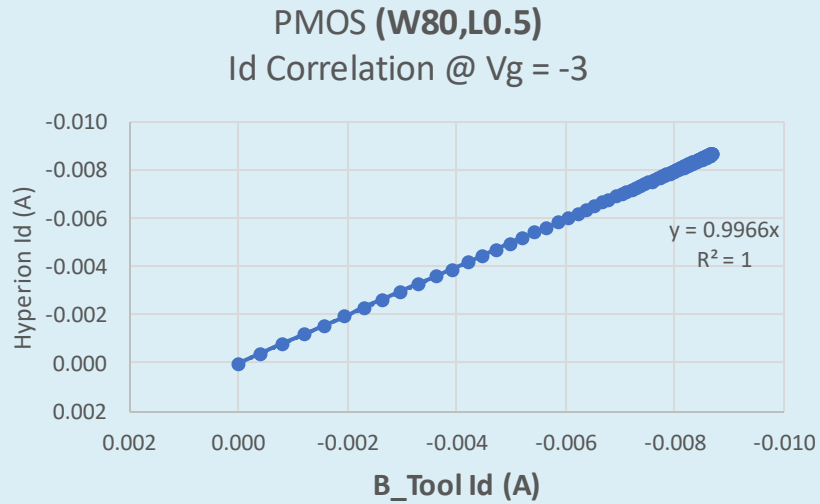
Correlation PMOS T1@ Die75 SEP. 2024

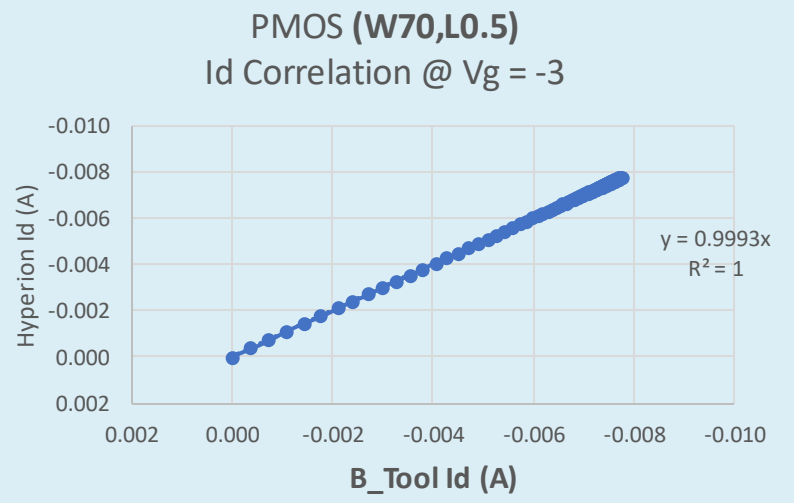
- Id-Vd comparison b/w EasyExpert(ref.) and Hyperion for Id test conditions@ Vg {-1V,-2V,-3V} / Vd {0V to -5V step: -50 mV}

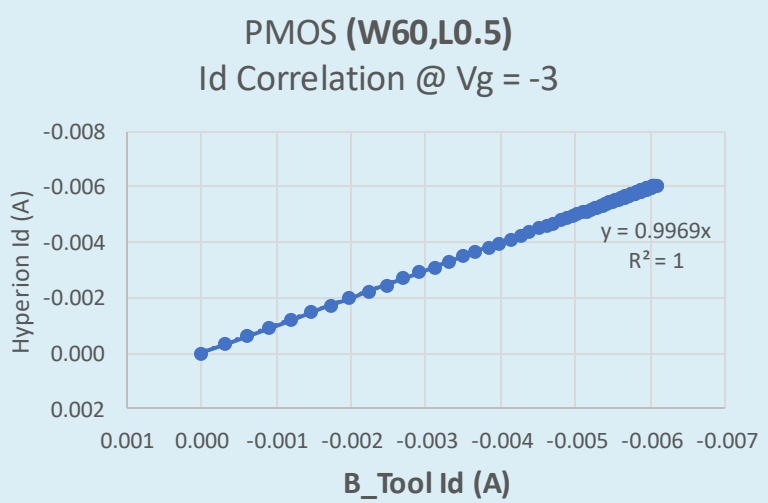












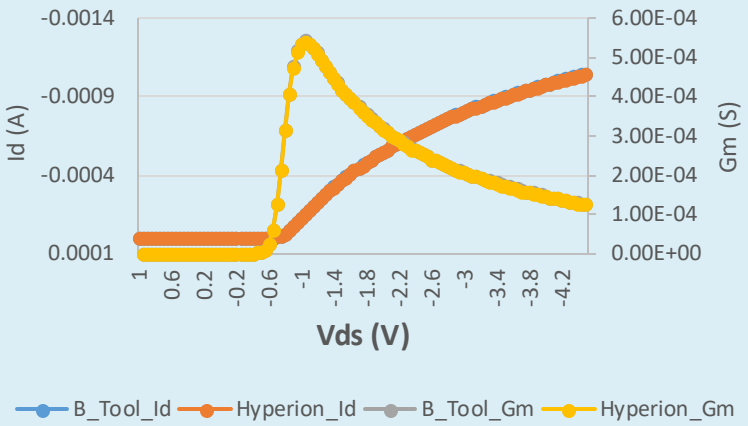
High resolution ADC on drain, 1PLC Integration, Hold/Delay 10ms

B_Tool EasyExpert vs. B_Tool Chroma Hyperion

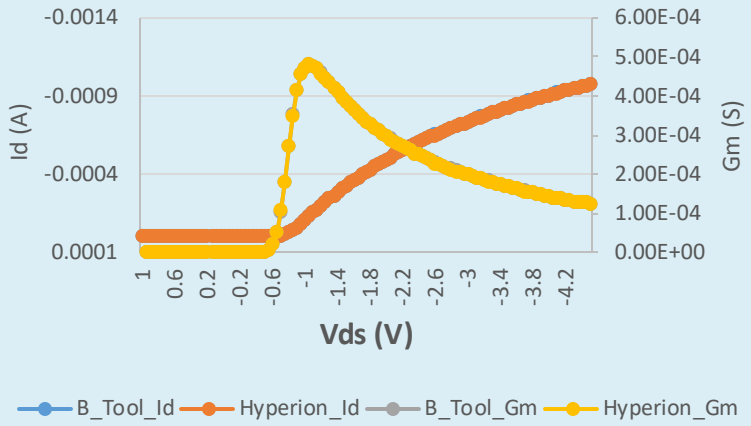
Correlation PMOS T1@ Die75 SEP. 2024

❑ Id-Vg comparison b/w EasyExpert (ref.) and Hyperion for Id test conditions@ Vg {1 to -5V, step:-50mV} / Vd {-100mV}

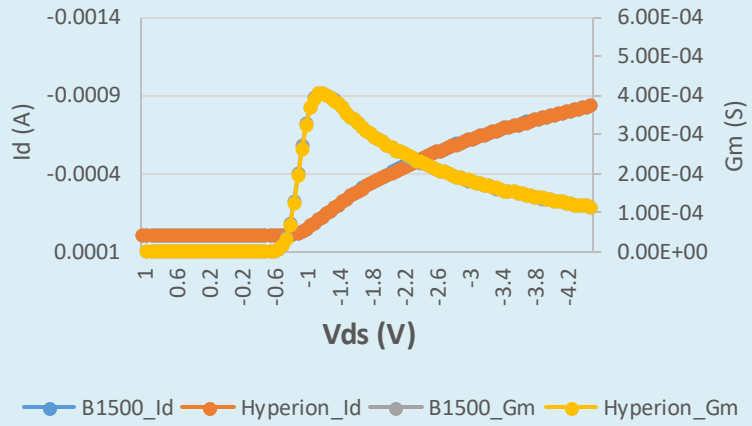
PMOS **(W80,L0.5)**



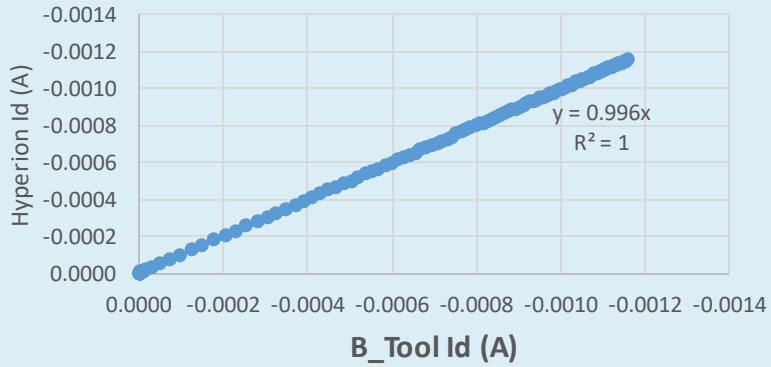
PMOS **(W70,L0.5)**



PMOS **(W60,L0.5)**

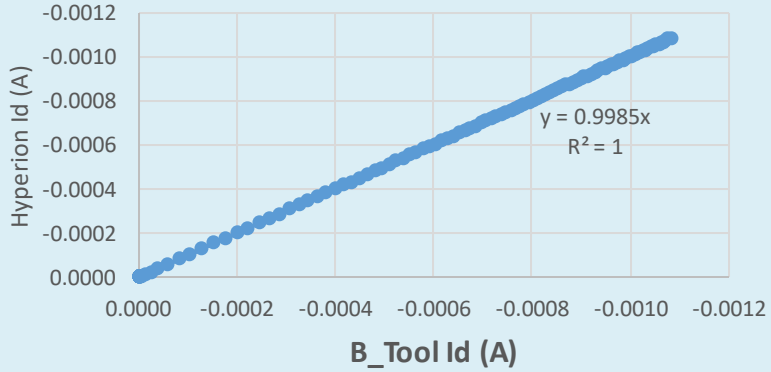


PMOS **(W80,L0.5)**
Id Correlation

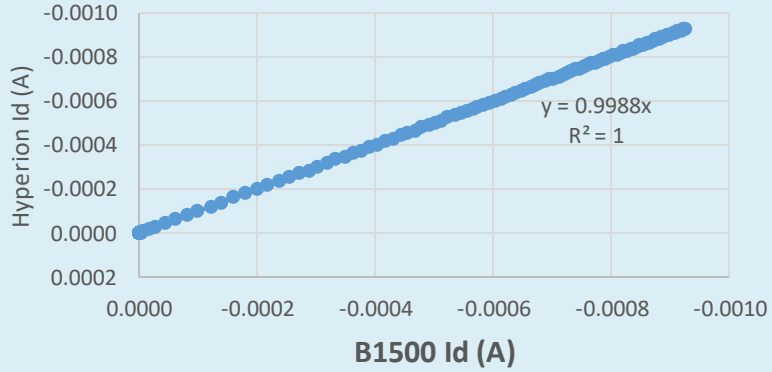


High resolution ADC on drain, 1PLC Integration, Hold/Delay 10ms

PMOS **(W70,L0.5)**
Id Correlation



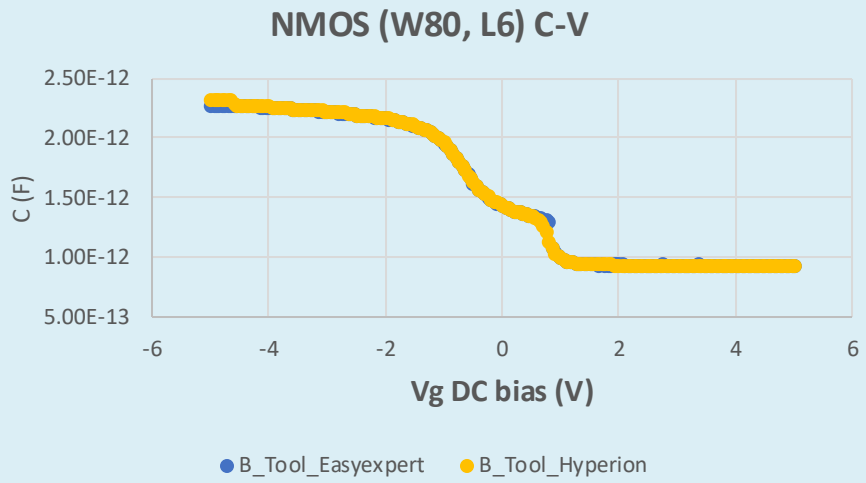
PMOS **(W60,L0.5)**
Id Correlation

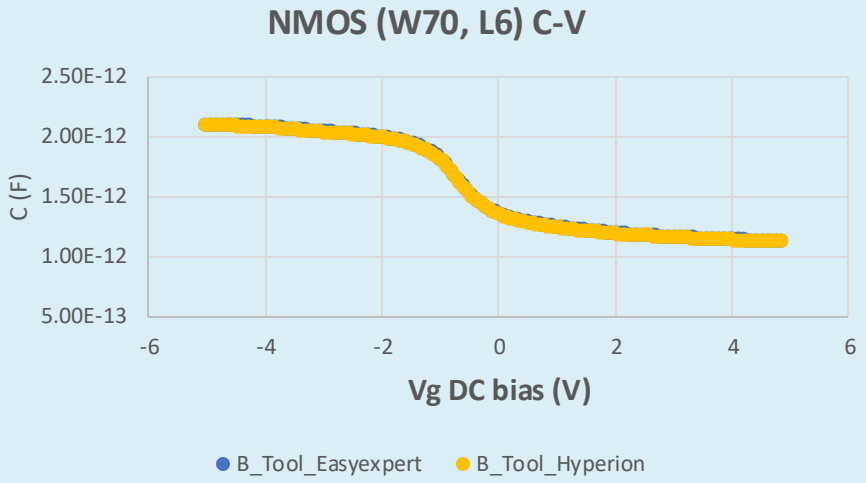


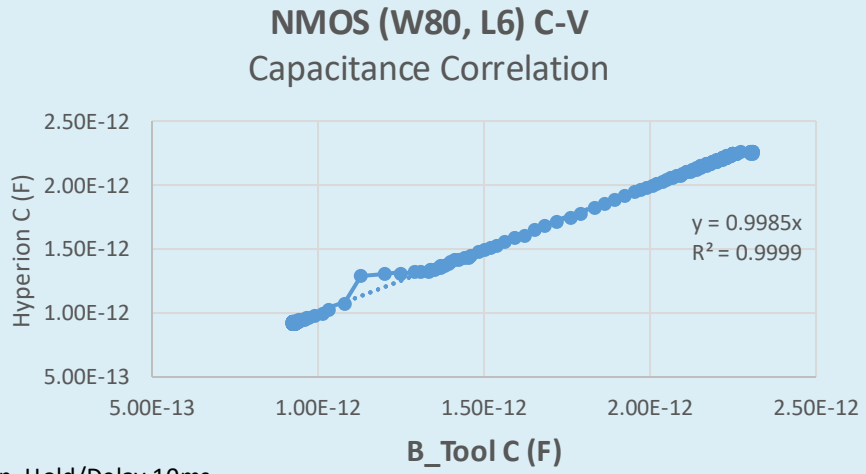
B_Tool EasyExpert vs. B_Tool Chroma Hyperion

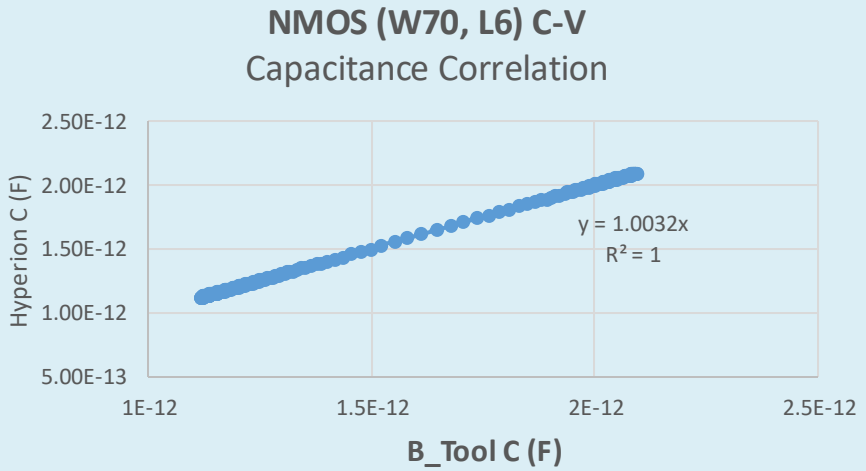
Correlation NMOS T3@ Die75 SEP. 2024

- C-V comparison b/w EasyExpert (ref.) and Hyperion @ Vg {-5 to 5V, step:-50mV, AC level 50mV, Frequency 100KHz}







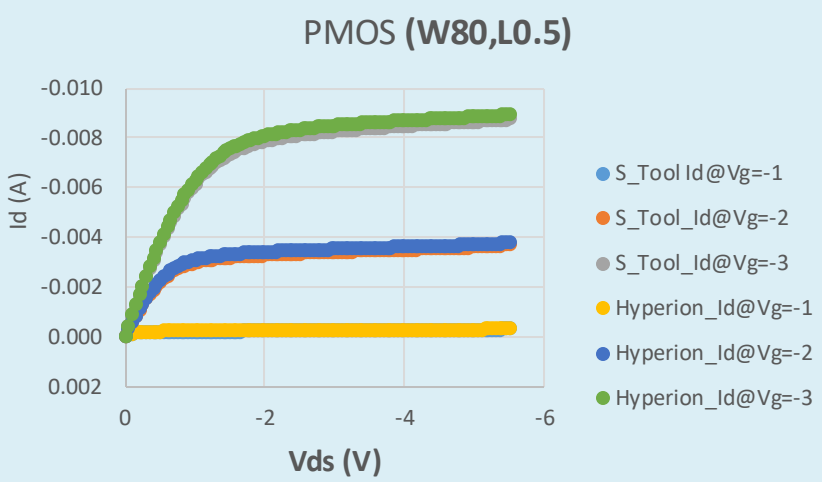


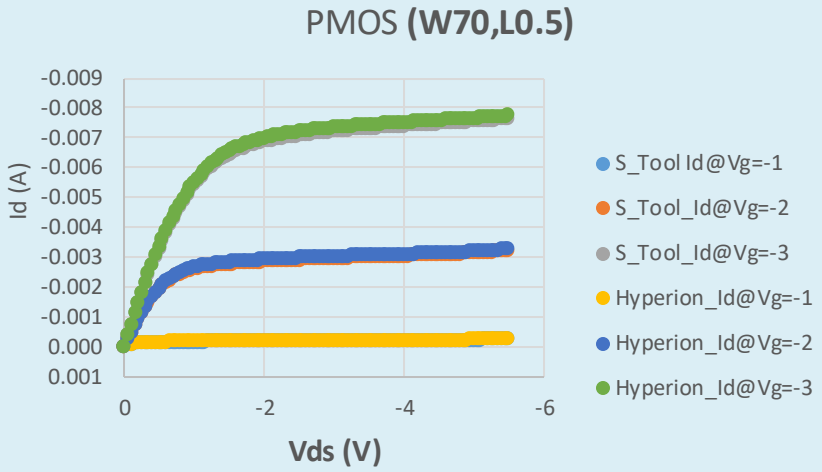
1PLC Integration, Hold/Delay 10ms

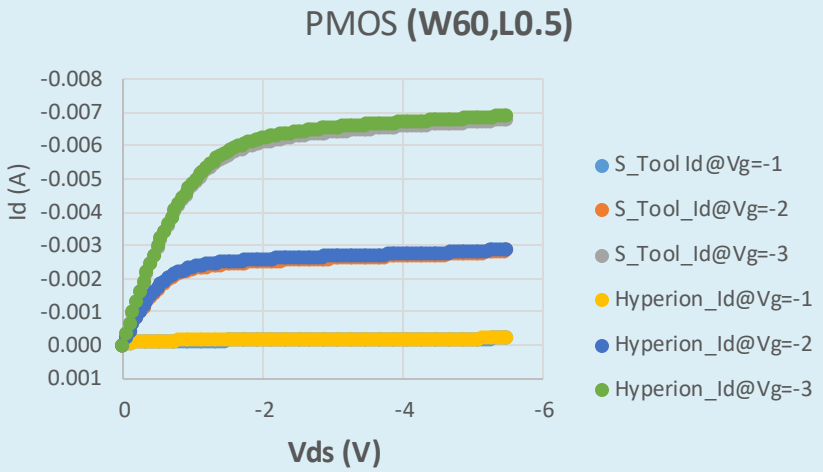
S_Tool Clarius vs. S_Tool Chroma Hyperion

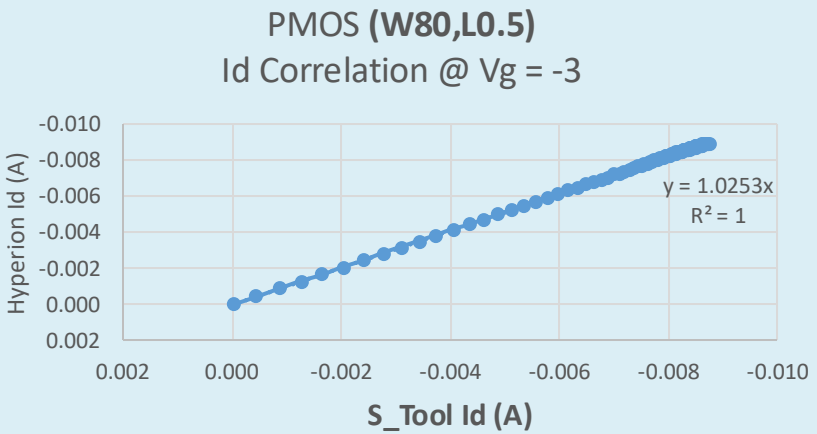
Correlation PMOS T1@ Die75 SEP. 2024

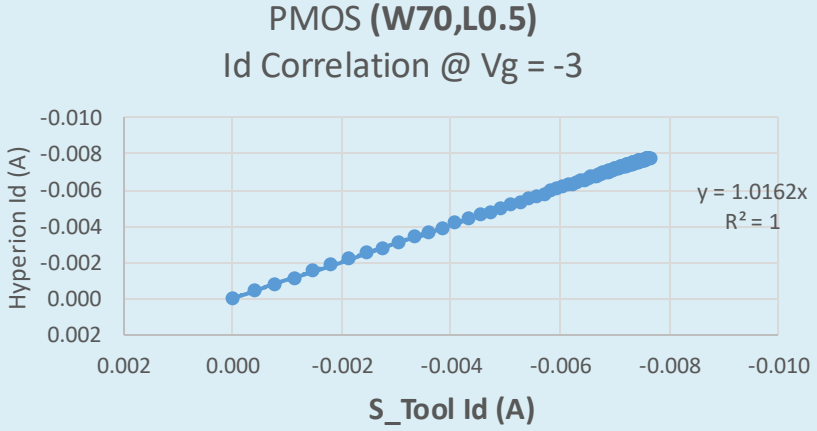
- Id-Vd comparison b/w Clarius (ref.) and Hyperion for Id test conditions@ Vg {-1V,-2V,-3V} / Vd {0V to -5V step: -50 mV}

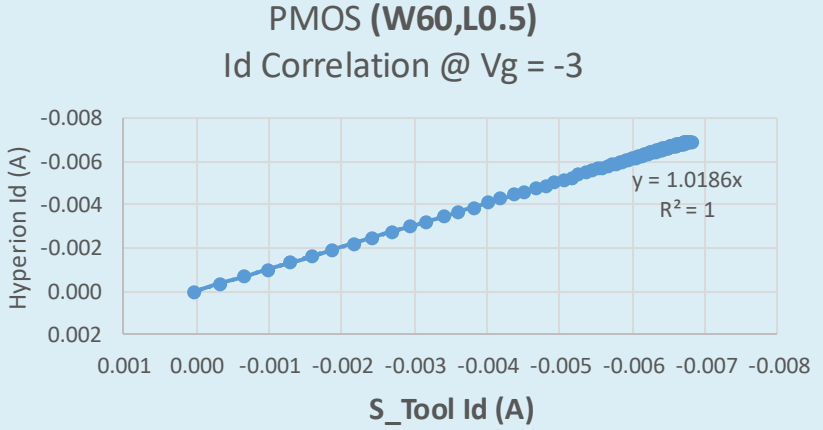












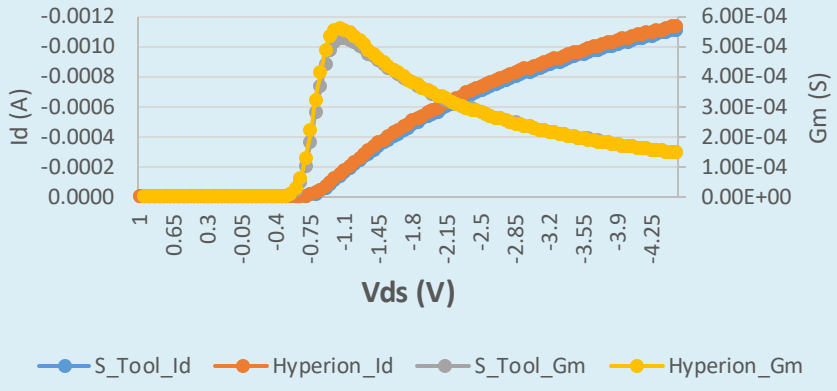
1PLC Integration, Hold/Delay 10ms

S_Tool vs. S_Tool Chroma Hyperion

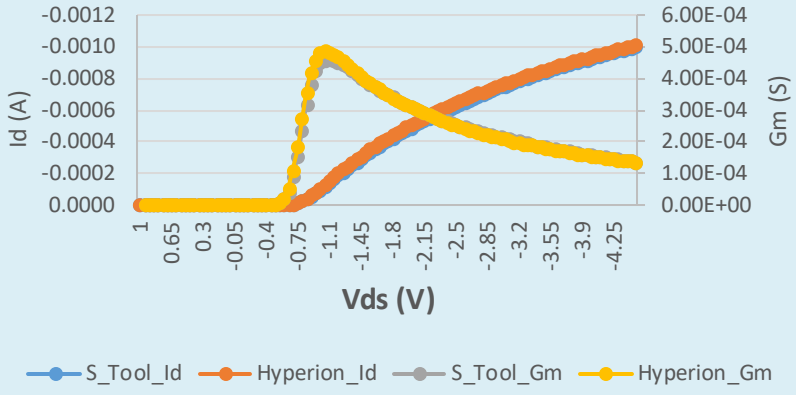
Correlation PMOS T1@ Die75 SEP. 2024

- Id-Vg comparison b/w Clarius (ref.) and Hyperion for Id test conditions@ Vg {1 to -5V, step:-50mV} / Vd {-100mV}

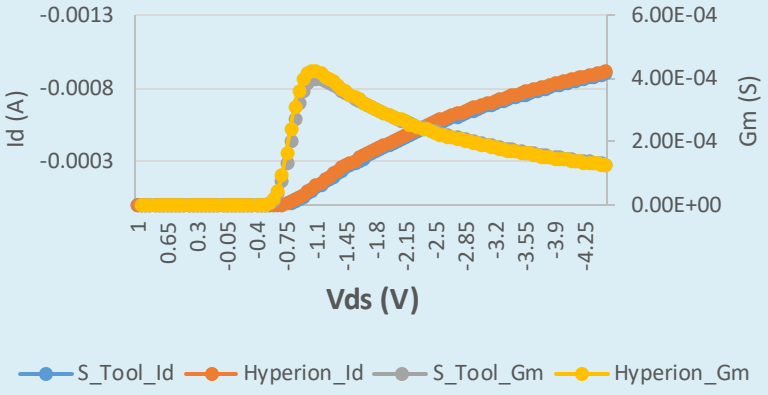
PMOS **(W80,L0.5)**



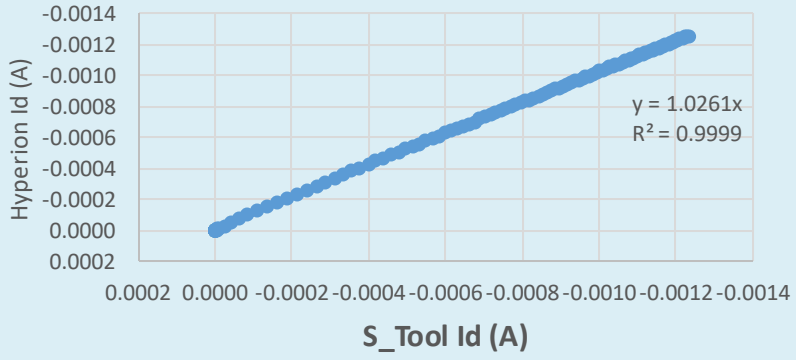
PMOS **(W70,L0.5)**



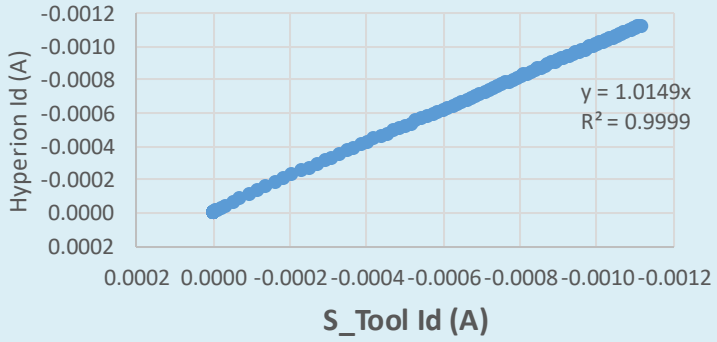
PMOS **(W60,L0.5)**



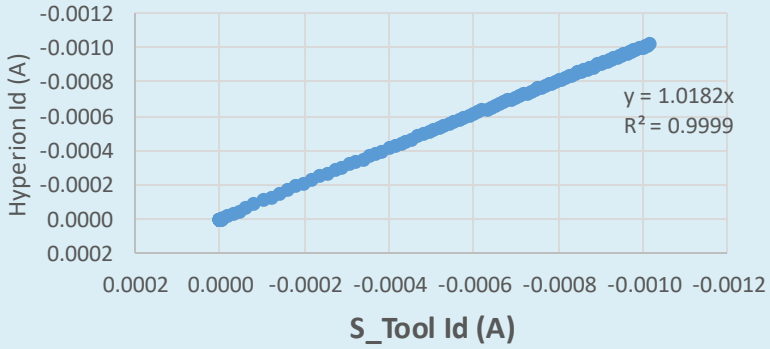
PMOS **(W80,L0.5)**
Id Correlation



PMOS **(W70,L0.5)**
Id Correlation



PMOS **(W60,L0.5)**
Id Correlation

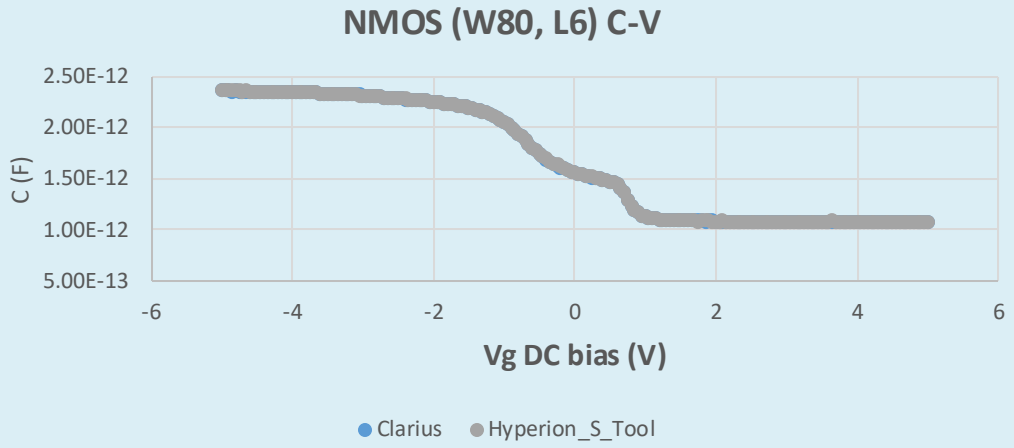


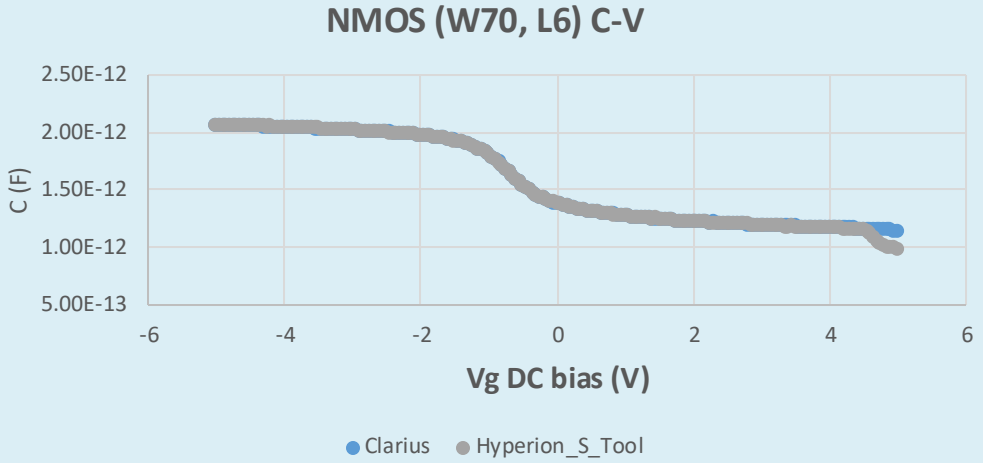
High resolution ADC on drain, 1PLC Integration, Hold/Delay 10ms

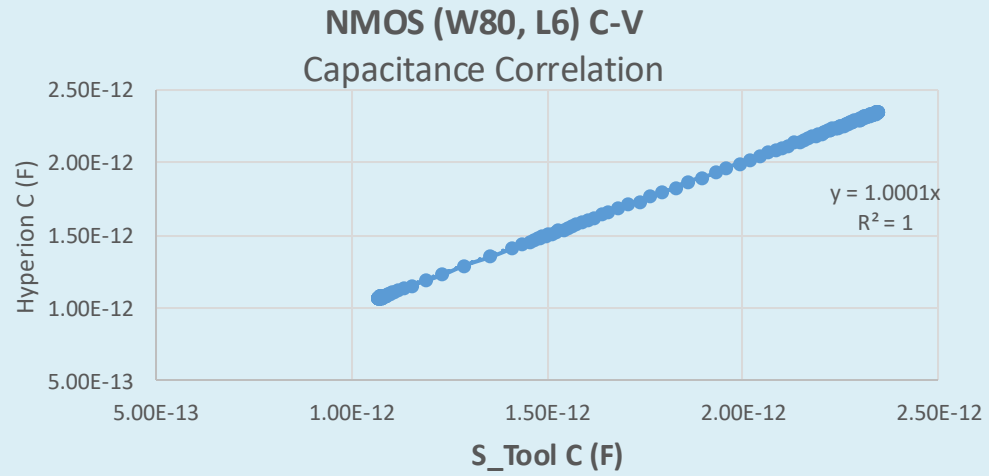
S_Tool Clarius vs. S_Tool Chroma Hyperion

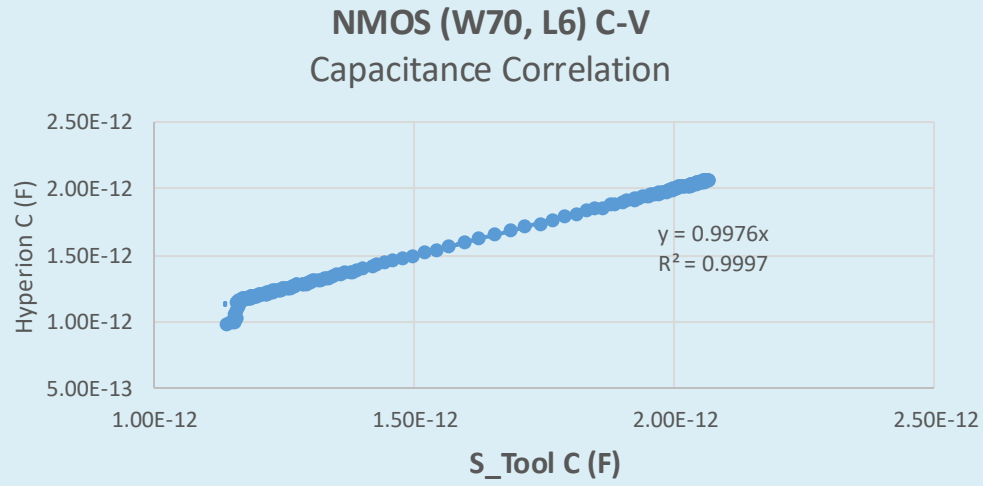
Correlation NMOS T3@ Die75 SEP. 2024

- C-V comparison b/w Clarius (ref.) and Hyperion @ Vg {-5 to 5V, step:-50mV, AC level 50mV, Frequency 100KHz}









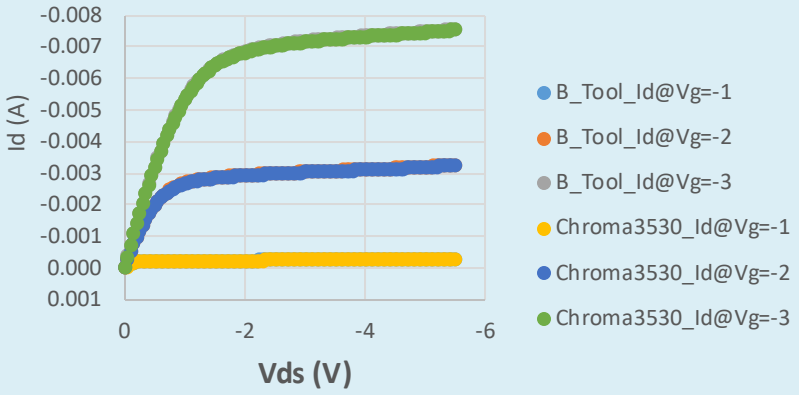
1PLC Integration, Hold/Delay 10ms

B_Tool vs. Chroma 3530 with Hyperion

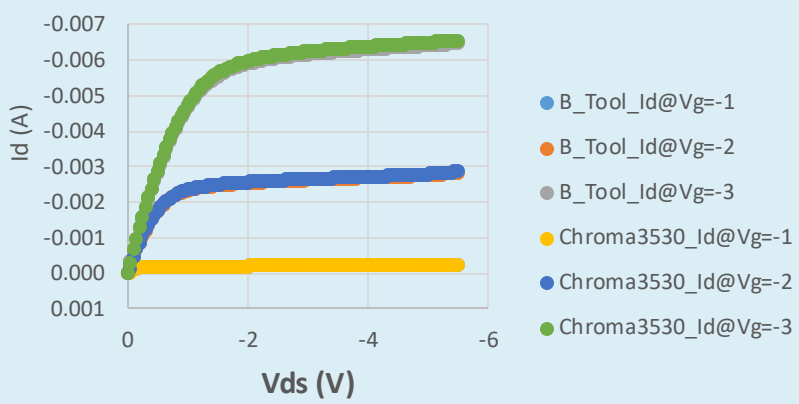
Correlation PMOS T1@ Die12_0 SEP. 2024

- Id-Vd comparison b/w B_Tool and Chroma 3530 for Id test conditions@ Vg {-1V,-2V,-3V} / Vd {0V to -5V step: -50 mV}

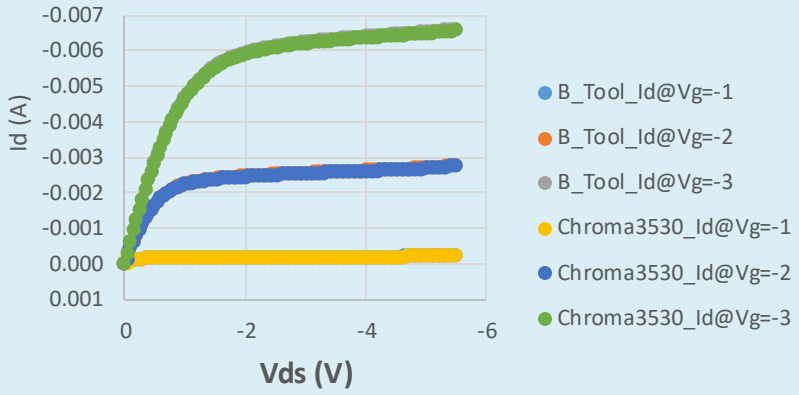
PMOS **(W80,L0.5)**



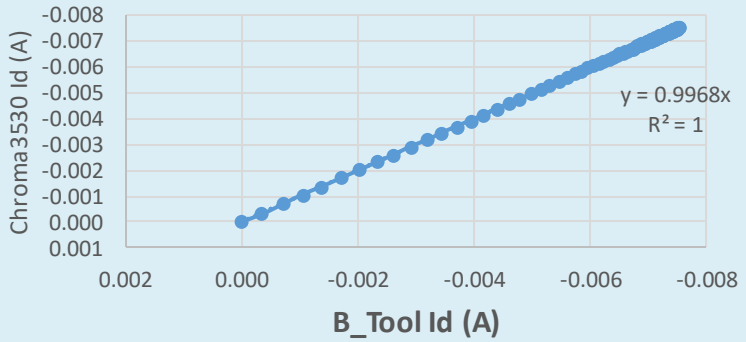
PMOS **(W70,L0.5)**



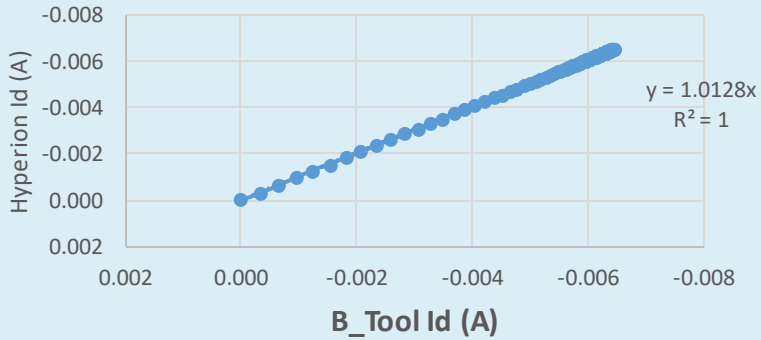
PMOS **(W60,L0.5)**



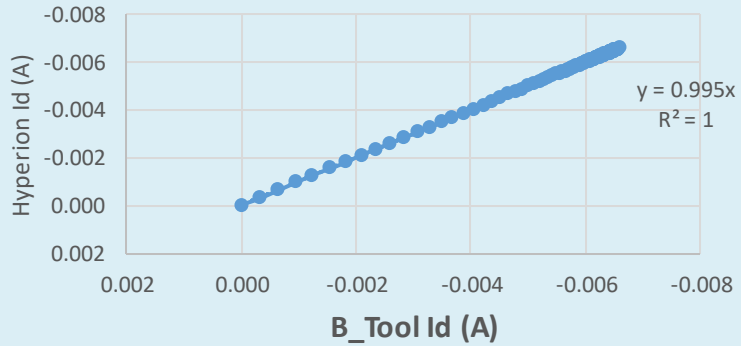
PMOS **(W80,L0.5)**
Id Correlation @ Vg = -3



PMOS **(W70,L0.5)**
Id Correlation @ Vg = -3



PMOS **(W60,L0.5)**
Id Correlation @ Vg = -3

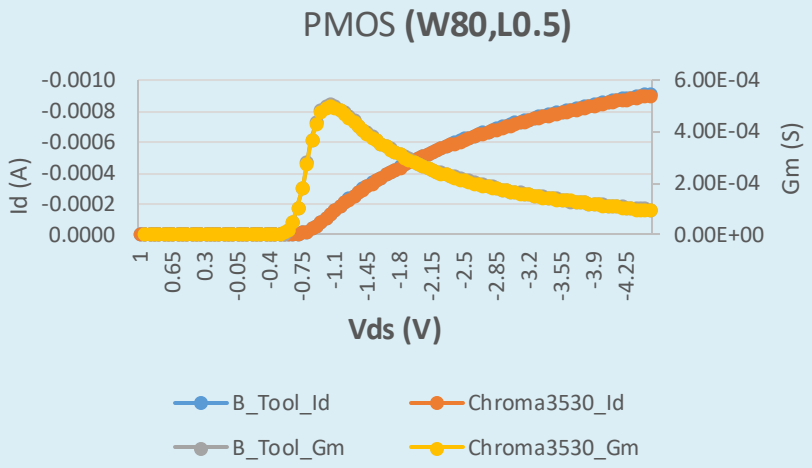


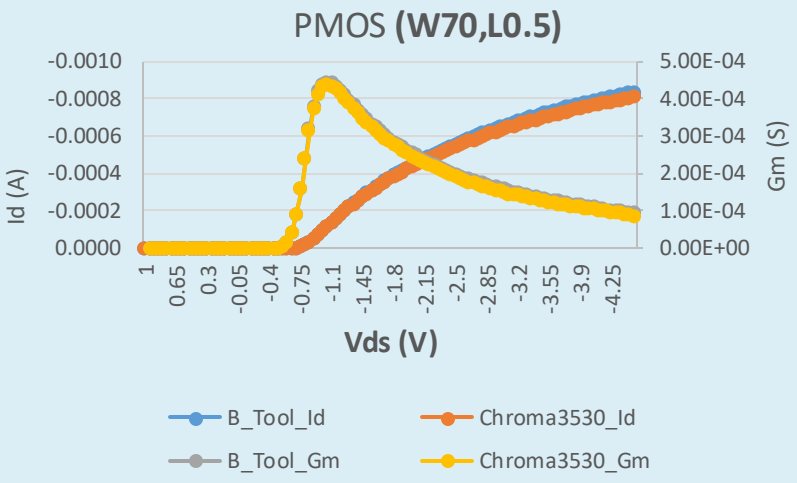
1PLC Integration, Hold/Delay 10ms

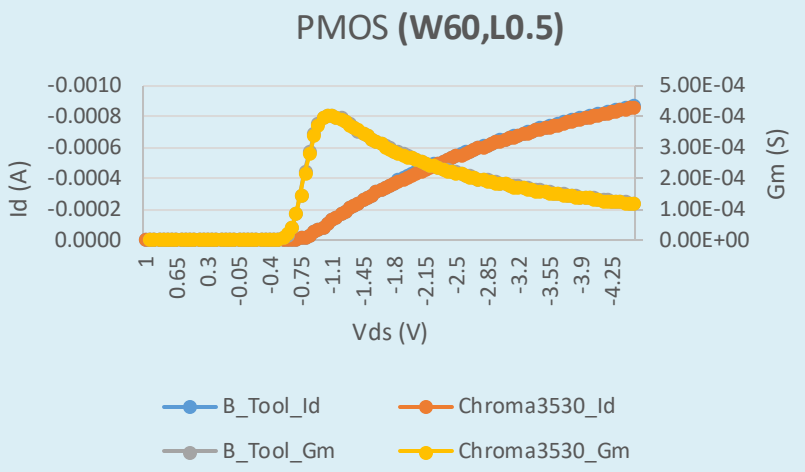
B_Tool vs. Chroma 3530 with Hyperion

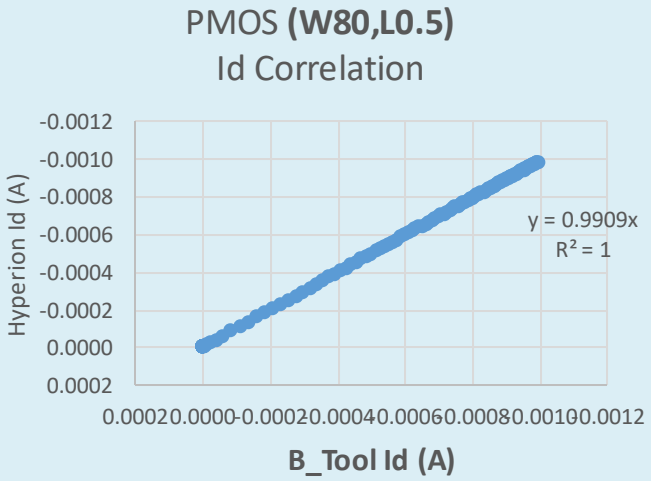
Correlation PMOS T1@ Die12_0 SEP. 2024

- Id-Vg comparison b/w B_Tool and Chroma 3530 for Id test conditions@ Vg {1 to -5V, step:-50mV} / Vd {-100mV}

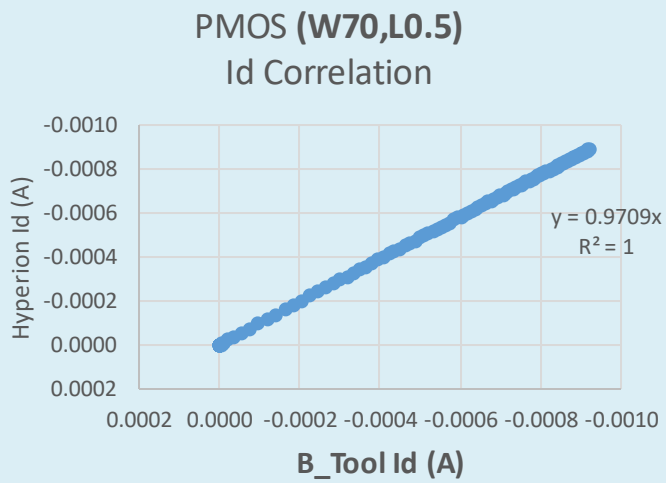


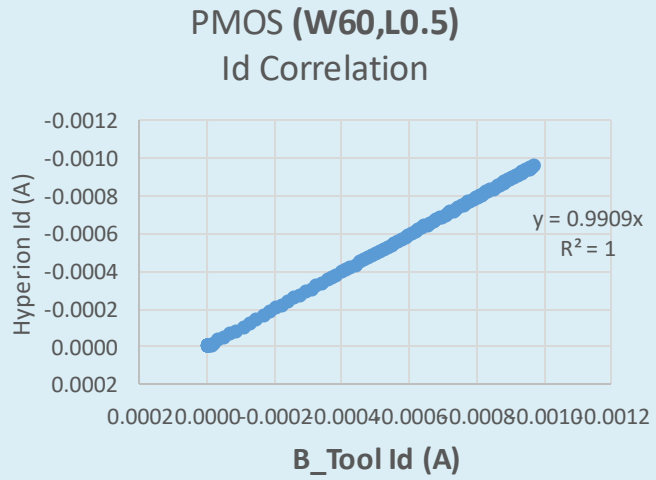






1PLC Integration, Hold/Delay 10ms

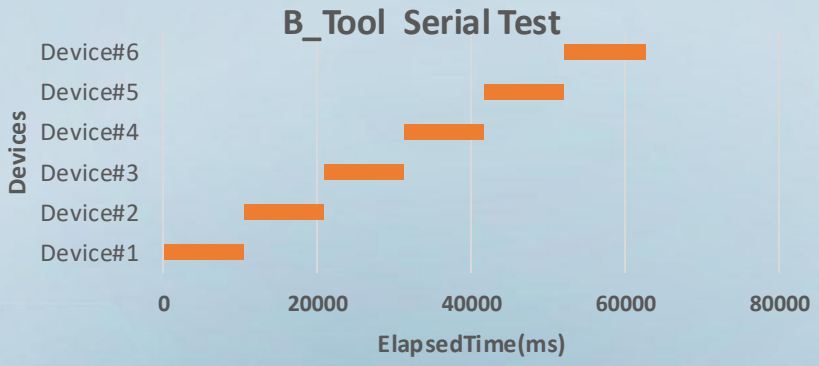


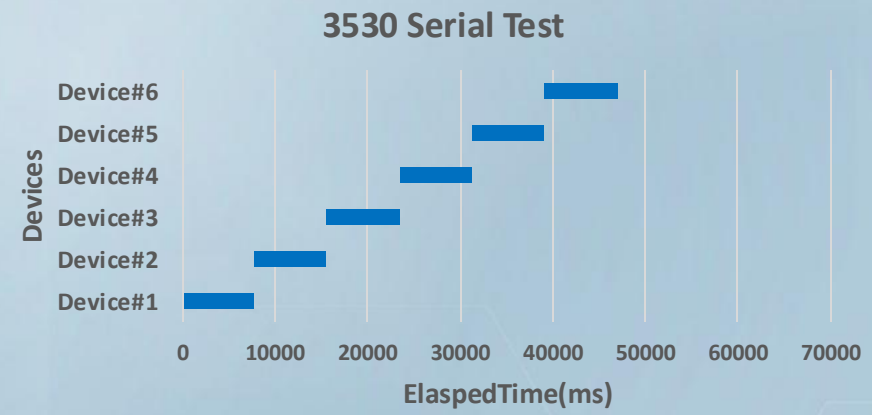


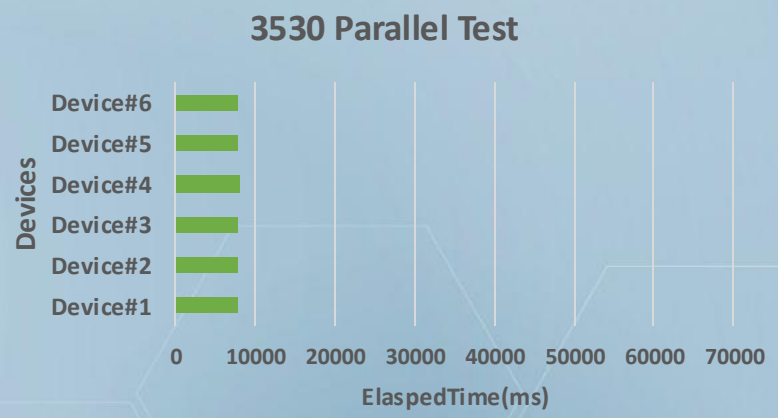
Data Correlation Results Summary

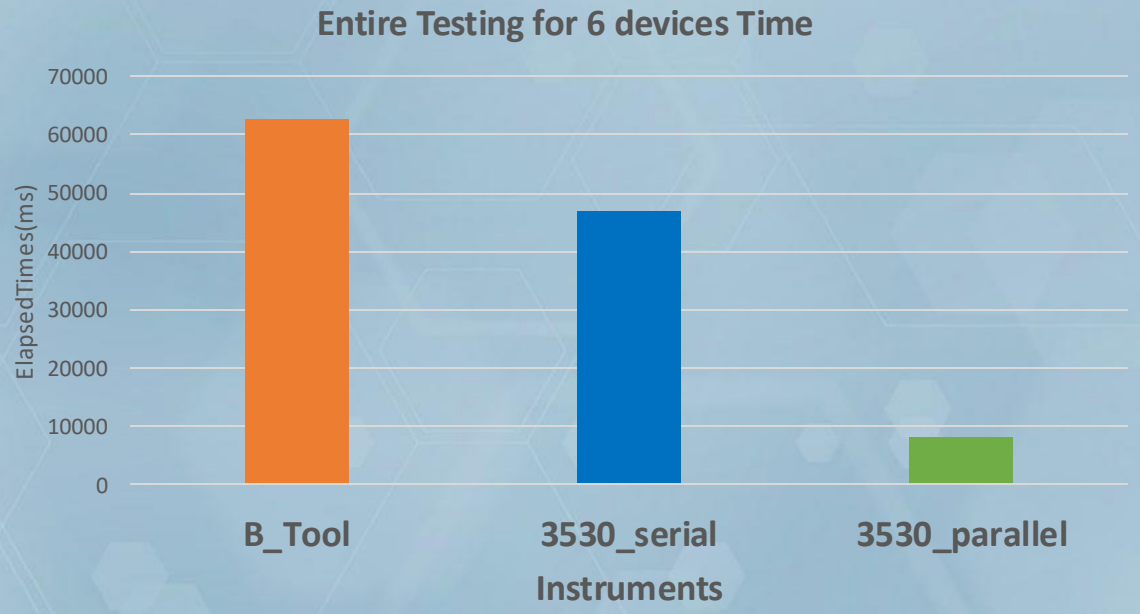
- Descent correlation found…
  - Between vendor GUI interface and Hyperion test algorithms using same test hardware
  - Between each vendor's test hardware using common Hyperion test algorithms
  - Between Hyperion controlling both vendor test hardware and Chroma 3530 serial testing and parallel testing with test throughput advantages
- Some issues seen due instrument-specific differences
  - Good correlation between 3530 and B1500A
- Chroma Hyperion and 3530 Opportunities
  - Investigation of causes differences that affect new technologies
  - Identical algorithms can be used on multiple setups of test hardware
  - Interchange of testing on multiple test hardware is very feasible

3530 Parallel Test Is 7.4 Times Faster Than B_Tool









6 nmos devices
Id from Vd
VD=0 to 5.5V, 0.1V steps
Vg=1,2,3,4,5V

1. Serial test: 3530 is faster than B_Tool **~1.2 times**.
2. 3530 parallel test is **~7.4 times** faster than B_Tool serial test on **6 DUTs** (MOSFET)
3. The throughput comparison between **3530-48P** and **48 pins switch-matrix test system** is estimated **>3 times** better on 12 DUTs (MOSFET)

A Cost-Effective Test Solutions for Parametric Test & Reliability Lab Summary

Keysight B_Tool is connected to Celadon's probe system (VC20) by triaxial cables.

Chroma 3530 is direct docking on the wafer with Celadon Probe System (VC20).

Chroma 3530 is connected to Celadon's probe system (VC20) by triaxial cables.

A Cost-Effective Test Solution for Parametric Test & Reliability Lab

Application	Hardware I	Hardware II	Software Platform	Triax Cable	Probe Card / VC20
Instrument to Instrument	Keysight B_Tool	Keithley S_Tool	Hyperion	Yes	Yes
Discrete <--> Wafer	B_Tool & S_Tool	3530	Hyperion	Yes	Yes
LAB to FAB	B_Tool & S_Tool	3530	Hyperion	Yes	Yes
Serial Between Parallel Test	B_Tool & S_Tool	3530	Hyperion	Option	Yes

References and Acknowledgement

[1] B. Smith, D. Hall, and G. Tranquillo, “Test Structure for Evaluation of Pad Size for Wafer Probing,” ICMTS, March 2023.

[2] R. Kaiser, K. Armendariz, and J. Hwang, “Production Parametric Probe: An Essential Guide to Lowering Cost of Test While Probing Very Small Pads,” SWTest, August 2021.

[3] Wang, M. 2/13/2024 *“A Review of Reliability in GAA Nanosheet devices” Feb 13,2024* Micromachines 2024, 15, 269

Keely Testa and Karen Armendariz, Celadon Systems, Inc. & Jonathon Lee and Chintankuma Patel, Chroma ATE Inc. for helping with the preparation of this presentation

Thank You!


Chroma
Advancing Excellence
x
CELADON
A Wholly Owned Subsidiary of MPI CORPORATION