SWTEST ASIA
PROBE TODAY, FOR TOMORROW

A novel memory test system with an electromagnet for STT-MRAM wafer level testing

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Outline

- Introduction
- Development of test system
- Measurement results using developed STT-MRAM test system
- Conclusion & Future Plan

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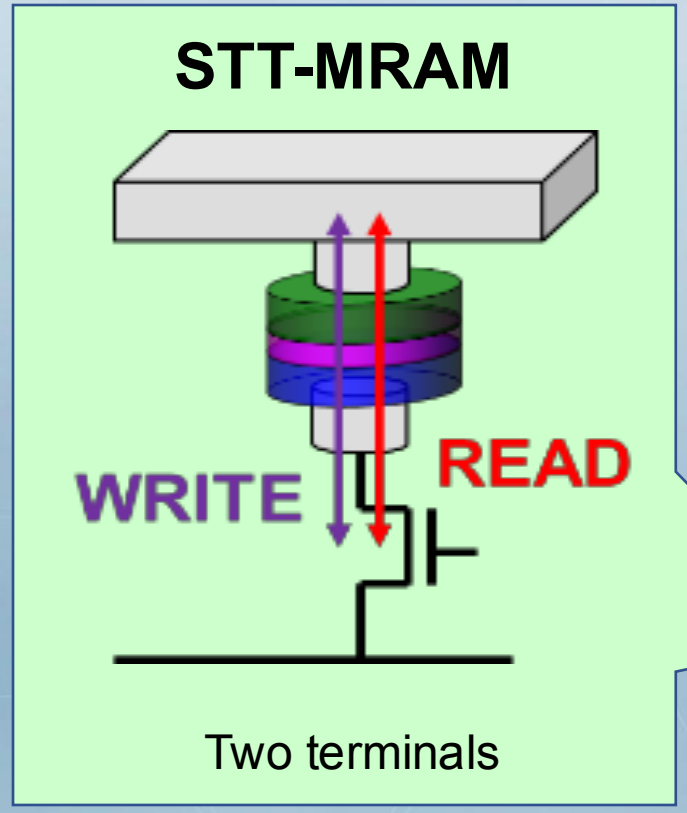
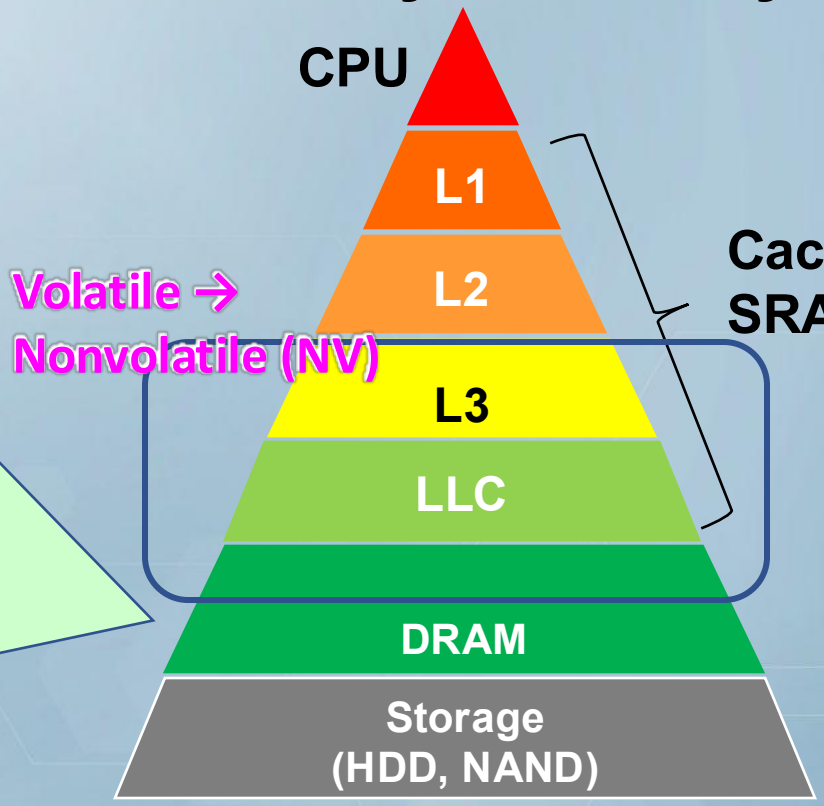
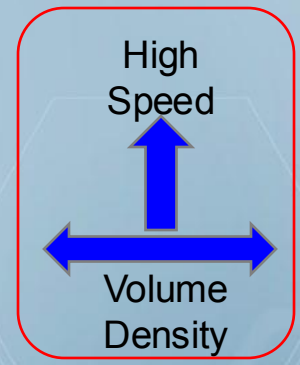
STT-MRAM as NV-Logic and NV-Working Memory



Memory hierarchy



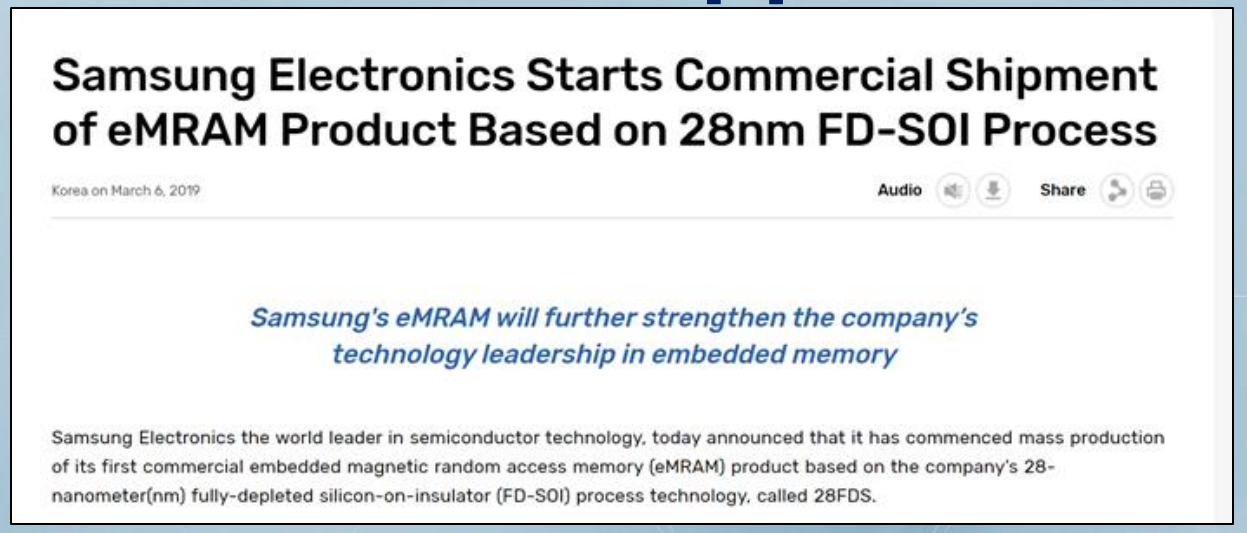


H. Ohno et al., IEDM2010 (Invited),
T. Endoh, ITRS Emerging Research Memory Technologies Workshop 2010,
T. Endoh, STS in SEMICON Korea2010 (Invited)

To reduce power consumption, STT-MRAM is the best choice for memory applications from DRAM to many kinds of embedded memory (SRAM, eFlash, and eDRAM) for Logic , because of nonvolatility, excellent endurance & CMOS compatibility for these MRAMs.

Mass production of STT-MRAM and its applications

https://www.mram-info.com/tsmc-start-emram-production-2018



https://news.samsung.com/global/samsung-electronics-starts-commercial-shipment-of-emram-product-based-on-28nm-fd-soi-process

Wearable devices

Huawei with Sony's SoC

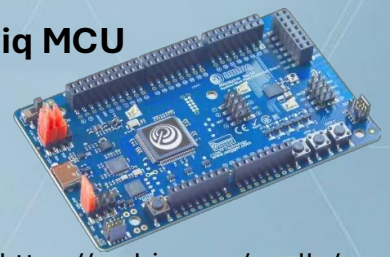
https://medias.yolegroup.com/uploads/2021/02/YINTR21218-emerging-Non-Volatil-Memory-2021-sample.pdf

Fitbit with Ambiq's SoC

https://ambiq.com/apollo4-plus/

IoT edge devices

Ambiq MCU



https://ambiq.com/apollo/

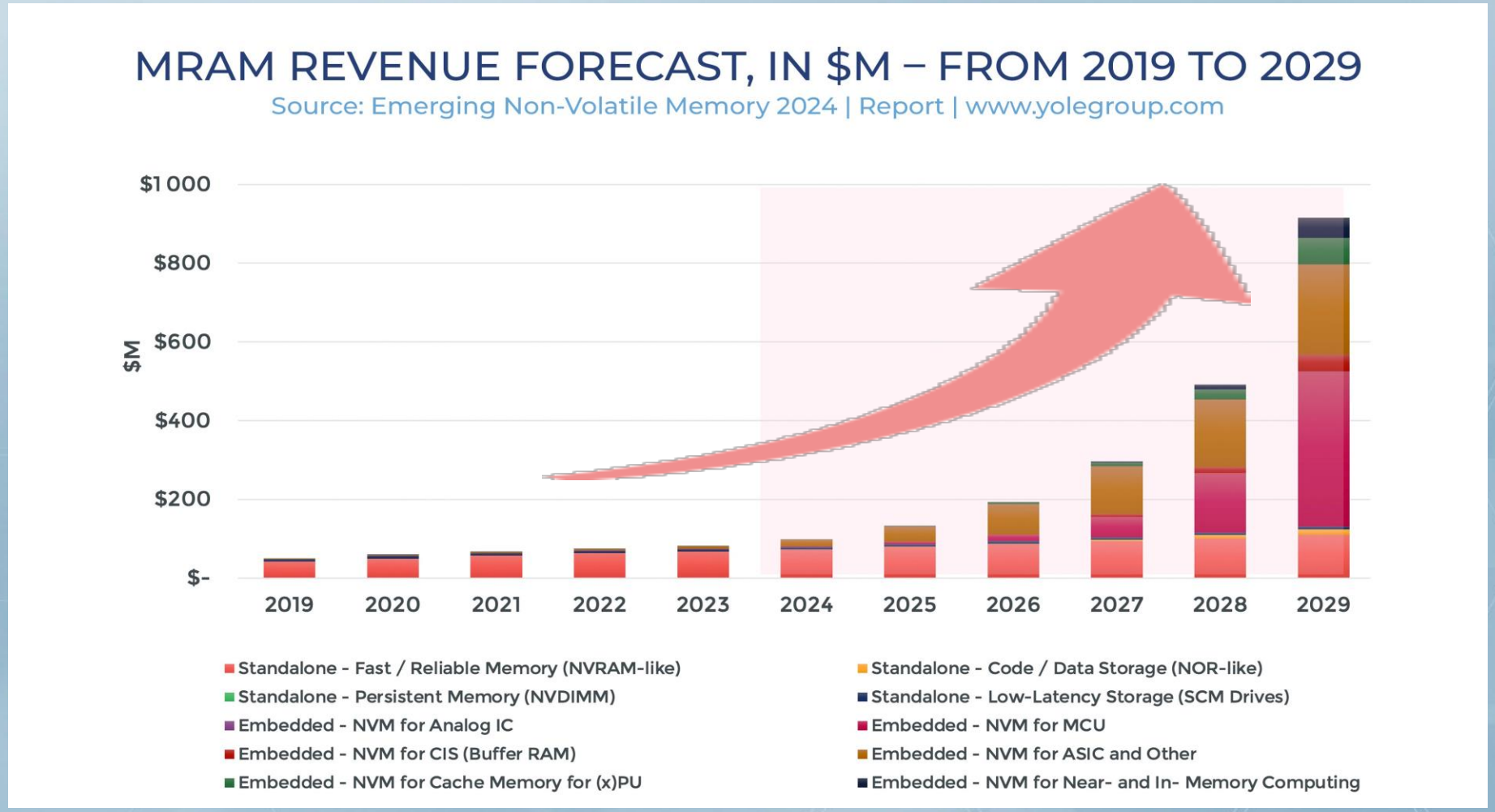
Accelerator @ Gyrfalcon

https://www.mram-info.com/

https://www.techinsights.com/ja/node/34597

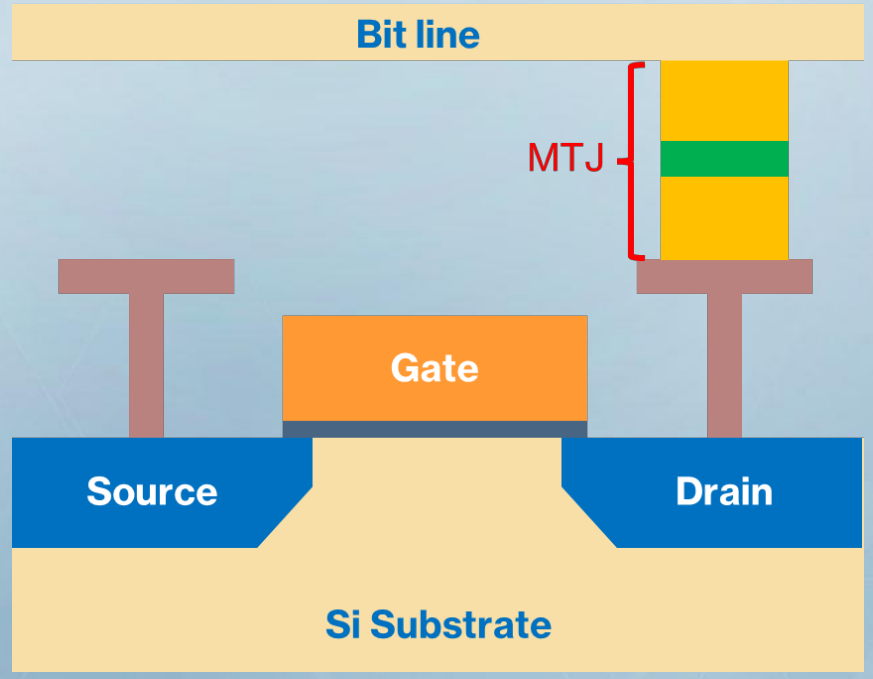
Since the mass production of STT-MRAM at major foundries in 2018, the market for applications such as wearable devices and IoT edge devices has been expanding.

STT-MRAM Market Forecast by Application

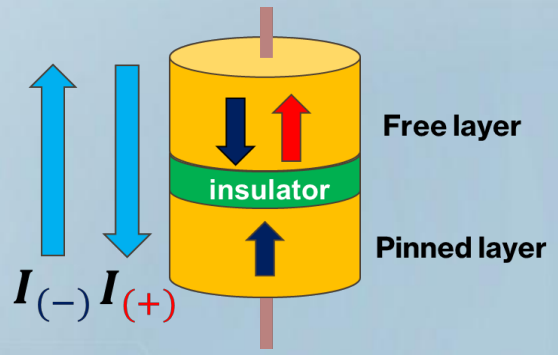


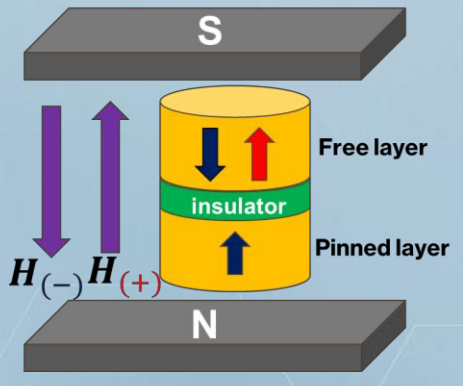
- **Embedded MRAM (eMRAM) is leading the way**
- **The primary applications are for ASICs and MPUs**

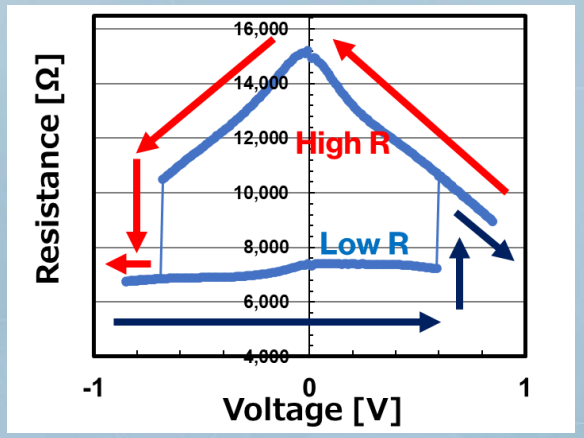
Operation of STT-MRAM



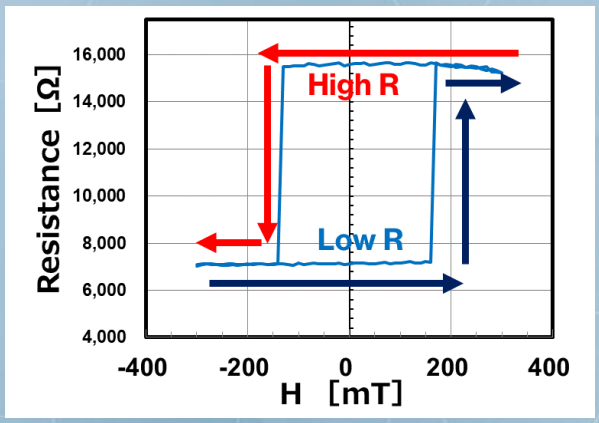
STT-MRAM cell







MTJ R - V Characteristic



MTJ R - H Characteristic

T. Endoh et al., J. Low Power Electron. Appl. 8, 44 (2018).
S. Ikeda et al., Nature Mat. 2010, 9, 721 (2010) , H. Honjo et al., VLSI 2015,

- **MRAM (Magnetoresistive RAM) consists of a MTJ (Magnetic Tunnel Junction) and a transistor**
- **MTJ consists of two ferromagnets, with two states**

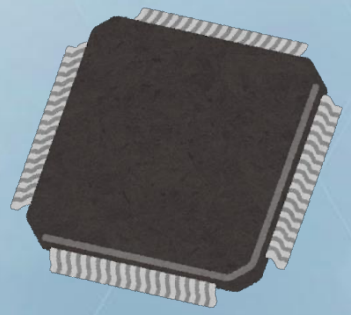
(i) Magnetization parallel ⇒ Low R (ii) Magnetization Antiparallel ⇒ High R

➢ **"1" and "0" is recognized according to the direction of magnetization (R Difference)**

Requirements for STT-MRAM wafer test

■ Current CMOS-based memory
(DRAM, NAND Memory, SRAM, etc…)

Electric Charge

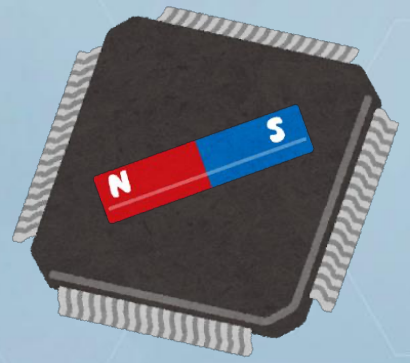


Testing

Memory test system

■ Spintronics-based memory
(STT-MRAM)

Electric Charge
&
Spin (magnet)

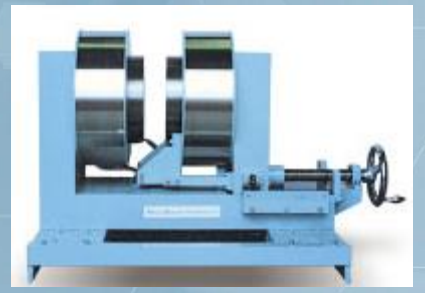


Testing

Memory test system

+

Electromagnet (MRAM special)



R. Tamura et al., NVMTS 2018, NVMTS 2019
H. Sato et al., IEDM 2017

■**To evaluate spintronics devices (STT-MRAM), it is necessary to observe both electrical and magnetic properties at the same time**

➢ **Need to incorporate a magnetic field measurement system**

R&D scheme for spintronics-based LSI testing

TOEI

Electromagnet

ADVANTEST

Memory Tester

STT-MRAM fabrication & analysis technologies

TOHOKU UNIVERSITY

cies

ACCRETECH
TOKYO SEIMITSU

300mm Wafer
Full automatic prober

Development of new memory test system specified for STT-MRAM testing

CIES: Center for Innovative Integrated Electronic Systems

Challenges in the current STT-MRAM test system

T5822ES
Cable-end docking
± 800mT max@10mm□
PC: Φ300mm(Special)
Room Temp.

Proto-type

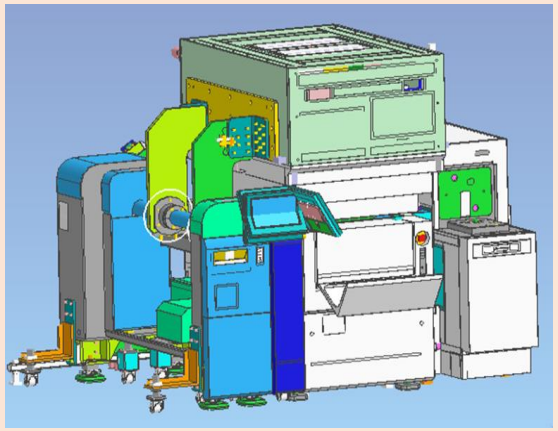
R. Tamura et al., NVMTS 2019

T5822
Direct docking
± 160mT max@50mm□
PC: Φ480mm
Room Temp.

1st Generation

5th CIES Tech. Forum 2019

This Work



Development of 2nd Generation

So far, we have developed Proto-type and 1st -Generation systems. However, to improve evaluation efficiency, the following functionality enhancements are required:

(1) Wider area (120 mm□) magnetic field application function (±100 mT) for mass production evaluation (Wide magnetic field mode)

(2) High magnetic field application function (±450 mT) for detailed evaluation (High magnetic field mode)

In addition, the above functions must be compatible with standard ϕ520mm probe card.

Also, Support for testing over a wide temperature range (-40 to 150°C) is required for reliability evaluation.

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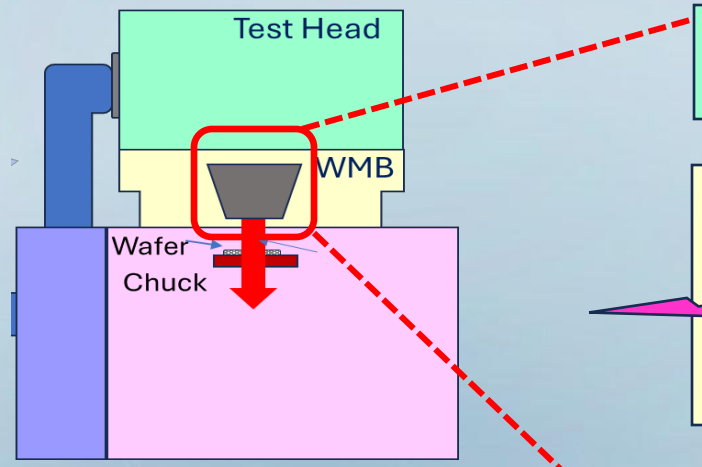
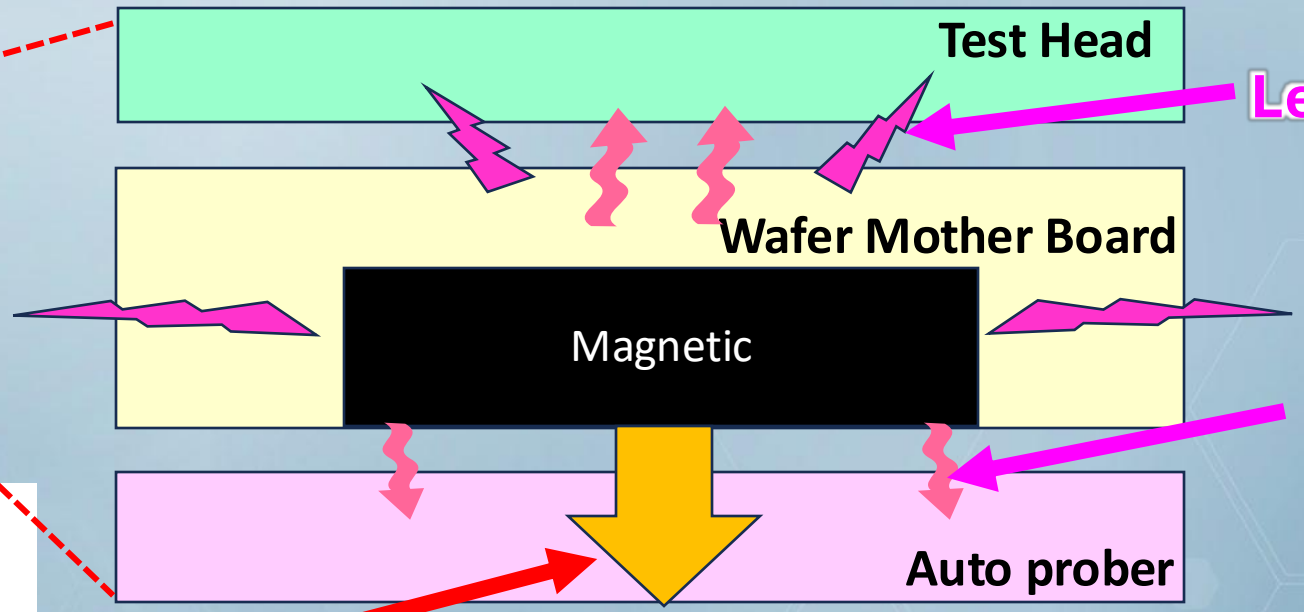
Issues of 1st Generation test system





Prober system consists of
(Test Head)
+ (Wafer Mother Board:WMB)
+ (Auto Prober).

Limits to applying high/wide magnetic

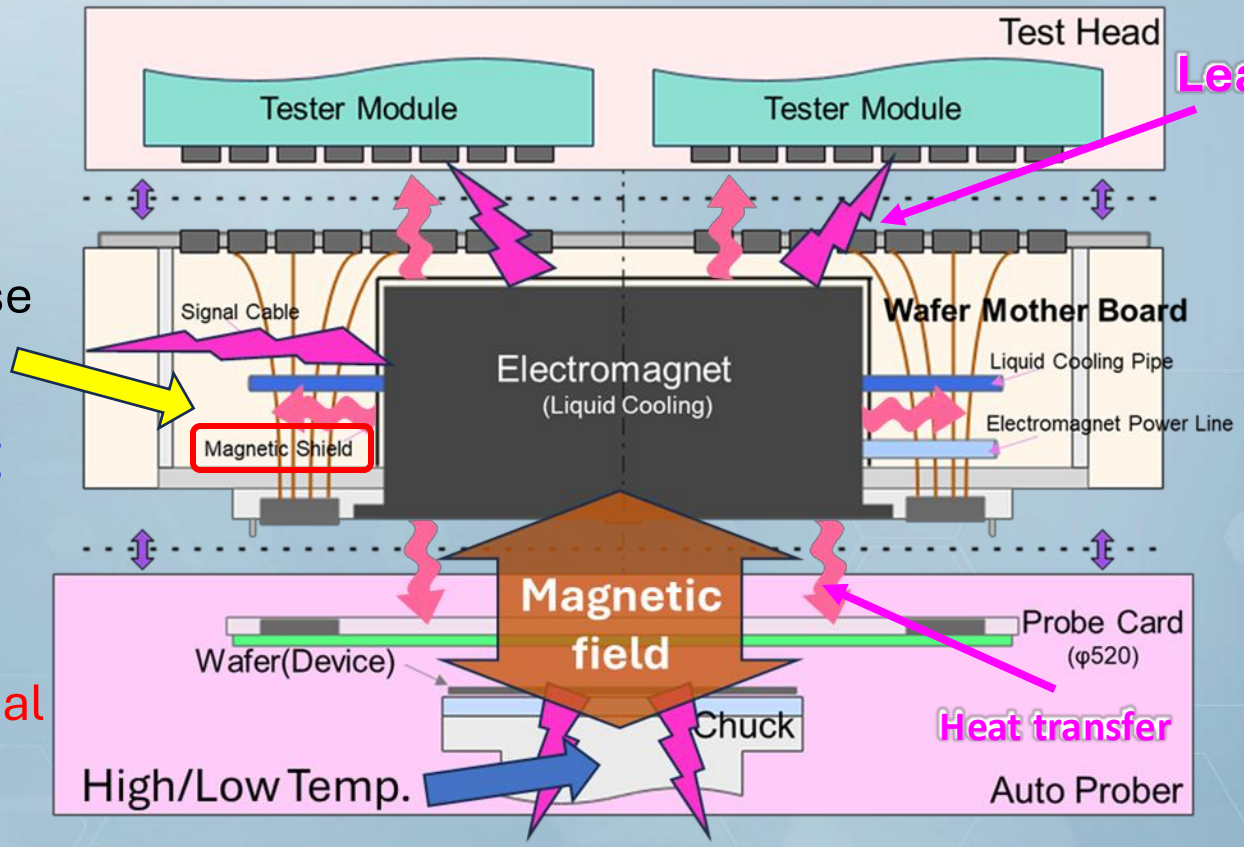
Performance of 1st Generation test system	Issue
Magnetic field applied area : 50 mm □	Because the applied area is small, the number of probe touchdowns increases, resulting in low evaluation efficiency.
Applied magnetic field strength : <160 mT.	Insufficient for detailed device evaluation

When attempting to apply a magnetic field over a wider area or a higher strength, issues such as magnetic field leakage and heat transfer become apparent.

Solutions to Magnetic Field Application Issues

To around tester
- Leak magnetic field
- Magnetic Immunity Noise
  =>Magnetic shield plate
- Heat transfer
  =>Indirect liquid cooling

To Probe Card
- Magnetic field
  =>Non-Magnetic material



To Electromagnet with 2 way mode
- Heating
  =>Indirect liquid cooling

To Prober
- Leak magnetic field
  =>Ceramic spacer
  (Non-Magnetic material)
- Heat transfer
  =>Dry air

To solve Issues when high magnetic fields is applied
- **Leak magnetic field => Magnetic shield, Non-Magnetic material**
- **Heat transfer => Indirect liquid cooling, Dry air**

Developed 2nd Generation Test System Appearance

Tester Main Frame (T5832)

Test Head & Electromagnet

Chiller Unit

Power Unit for Electromagnet

Prober (UF3000LX)

Probe Card

These pictures were taken at CIES

2nd Generation test system consists of some parts to achieve requirements

- **Magnetic field control & Temperature control**

Performance of Developed 2nd Generation Test System

Specification	2nd Generation System - This Work -	1st Generation - Previous Work -
Tester	T5832	T5822
Tester-Prober docking	Direct	Direct
Electromagnet	**2-Mode Support** Wide Magnetic mode: ± 150mT max **@120mm□** High Magnetic mode: ± **450mT max** @ 10mm□	± 160mT max @50mm□
Probe Card Size	ϕ520mm	ϕ480mm
Test Temperature	**-40 ~ 150°C** (Automotive application)	Room Temperature

2nd Generation (with standard ϕ520mm probe card) support 2-field modes

Wide magnetic field mode (for mass production evaluation) : ± 100mT max @ 120mm□

High magnetic field mode (for detailed evaluation) : ± 450mT max @ 10mm□

Also, 2nd Generation support for testing in the wide temperature range (-40~150°C) for automotive devices

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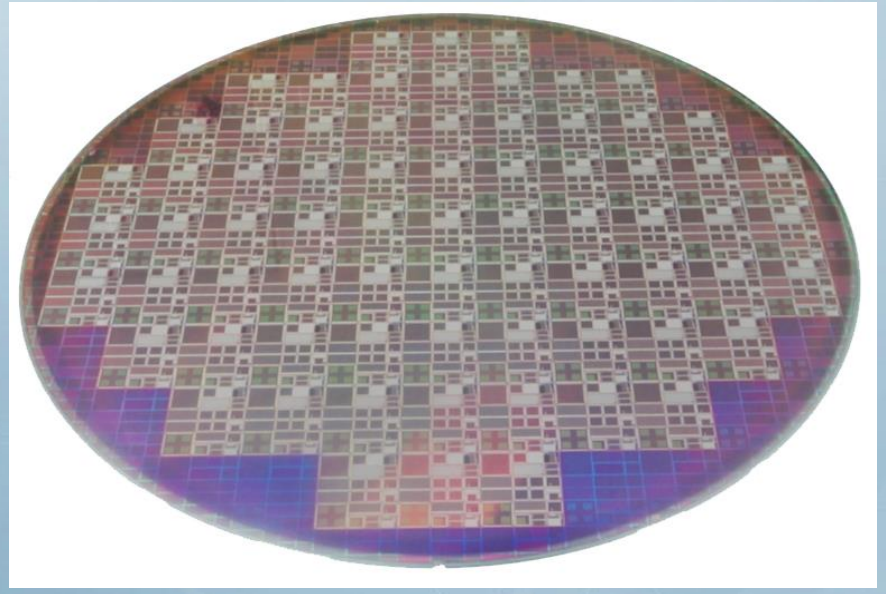
56Mb STT-MRAM Test Chip fabricated by CIES used and Electromagnets with two magnetic field modes



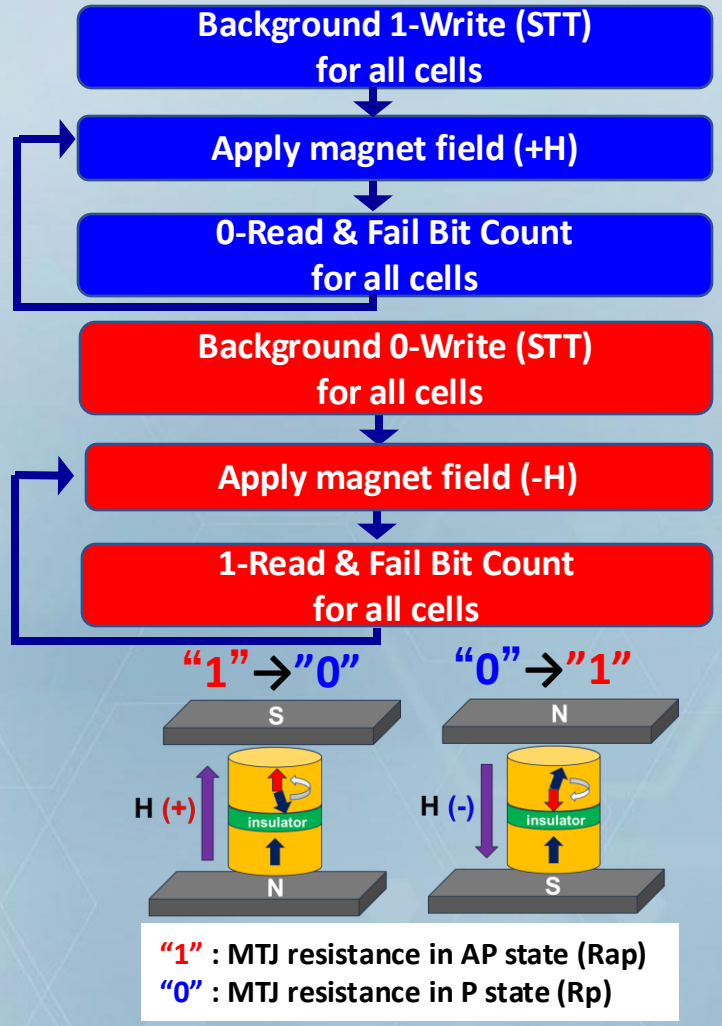
56Mb STT-MRAM chip fabricated in 300mm wafer

Electromagnets with two magnetic field modes installed in the test head

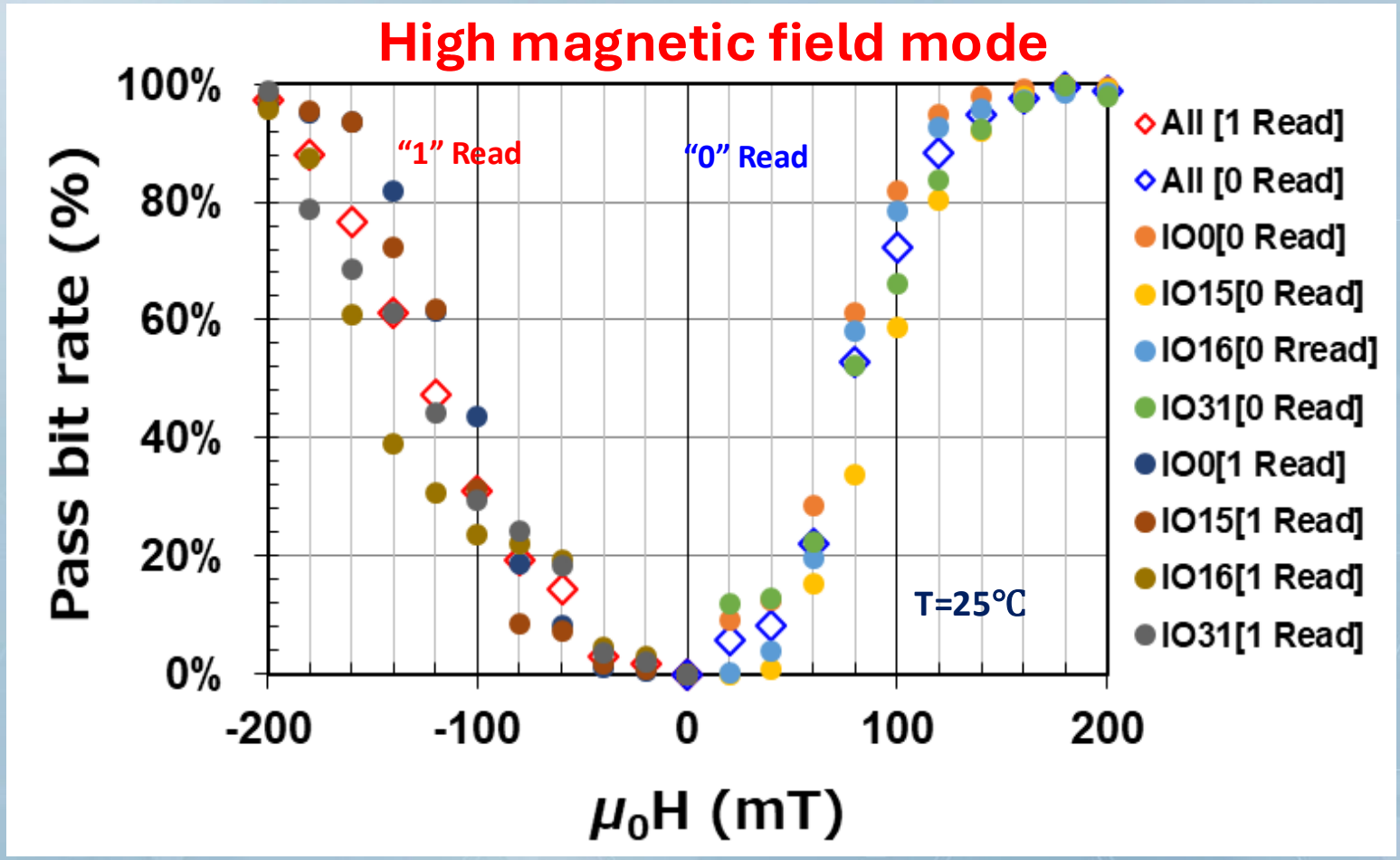
The test chip is fabricated in 300 mm wafer using CIES process line of TU .
We evaluated 56Mb STT-MRAM utilizing memory test system (T5832) installed at CIES.
In the 2nd generation test system, an electromagnet with two magnetic field modes was developed to be installed in the test head.

Pass bit rate as a function of Applied High Magnetic Field

Measurement Procedure



"1" : MTJ resistance in AP state (Rap)
"0" : MTJ resistance in P state (Rp)

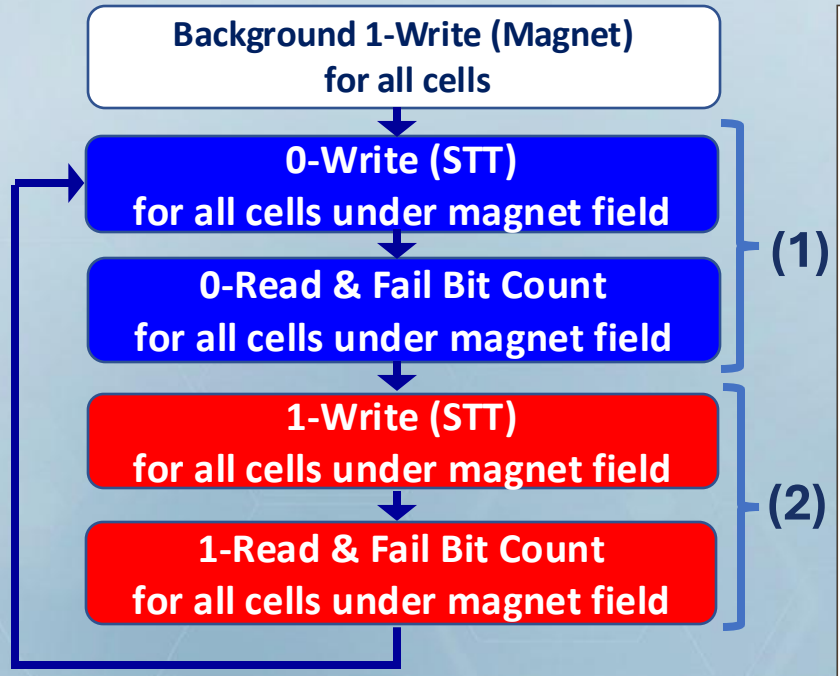


Pass bit rate vs Applied Magnetic field

We evaluated the pass bit rate vs applied magnetic field using high magnetic field mode.
We observed resistance state can be switched between "0" and "1" states using electromagnet.

Write Shmoo measured under Wide Magnetic Field mode

Measurement Procedure



T=25℃
Magnetic field: -100mT to +100mT
Write pulse width range: 1ns - 51ns
Write voltage: 0.8V - 1.3V

(1) "0" Write/Read

H = 0 mT

Write Vdd(V)	Write pulse width (ns) 1	11	21	31	41	51
0.8						
0.9						
1						
1.1						
1.2						
1.3						

H = -75 mT

Write Vdd(V)	Write pulse width (ns) 1	11	21	31	41	51
0.8						
0.9						
1						
1.1						
1.2						
1.3						

H = -100 mT

Write Vdd(V)	Write pulse width (ns) 1	11	21	31	41	51
0.8						
0.9						
1						
1.1						
1.2						
1.3						

(2) "1" Write/Read

H = 0 mT

Write Vdd(V)	Write pulse width (ns) 1	11	21	31	41	51
0.8						
0.9						
1						
1.1						
1.2						
1.3						

H = 75 mT

Write Vdd(V)	Write pulse width (ns) 1	11	21	31	41	51
0.8						
0.9						
1						
1.1						
1.2						
1.3						

H = 100 mT

Write Vdd(V)	Write pulse width (ns) 1	11	21	31	41	51
0.8						
0.9						
1						
1.1						
1.2						
1.3						

We evaluated the Write Shmoo using wide magnetic field mode
For the used test chip, the magnetic field above 75mT affect the write property.

- As described above, we were able to verify the functionality of the two magnetic application modes in our developed STT-MRAM test system.

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Conclusion & Future plan

■ Development of STT-MRAM Test System (2nd Generation test system)

We have developed a **new concept STT-MRAM test system that realizes high evaluation efficiency with two magnetic field application modes (see below)**, based on the 300 mm mass production evaluation equipment technologies of the memory tester, full auto prober, and standard ϕ520 mm probe card.

(1) Wide magnetic field mode (for mass production evaluation) : ± 100mT max @ 120mm □

(2) High magnetic field mode (for detailed evaluation) : ± 450mT max @ 10mm□

■ Device measurement results using 2nd Generation test system

- 56Mb STT-MRAM chip as Practical capacity memory was evaluated using 2nd Generation test system
- In the high magnetic field mode (-200mT to 200mT), the resistance state of the cell could be flipped from "0" to "1" or "1" to "0" with magnetic writing (not STT writing)
- Write Shmoo measurements were carried out in wide magnetic field mode (-100 mT to 100 mT) while applying a magnetic field.

➢ As a result, we were able to verify the functionality of the two magnetic application modes in our developed 2nd Generation STT-MRAM test system.

【Next step】

In the present study, measurements were carried out at a chuck temperature of 25°C.

In the future, evaluation under low temperature (-40°C) to high temperature (150°C) environments will be carried out for in-vehicle device evaluation.

Acknowledgment

- This work was supported by the STT-MRAM Program on the CIES Consortium, JST-OPERA under Grant JPMJOP1611, NEDO under Grant P18014 and P12004, and Ministry of Education, Culture, Sports, Science and Technology (MEXT) Initiative to Establish Next-generation Novel Integrated Circuits Centers (X-NICS) Grants JPJ011438.
- Special thanks to MJC (Micronics Japan) for their cooperation in designing and manufacturing probe cards.
- The authors wish to thank Mr. Mitsuo Yasuhira for his great help in technical support in this project at CIES, Tohoku University.

Thank you