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New wafer testing challenges for leading-edge SoC products

～SWTest Asia 2024 Japan industry vision presentation～

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Product Engineering Division

Socionext Inc.

Agenda

1 About Socionext

2 Technology trends for our leading-edge SoC products

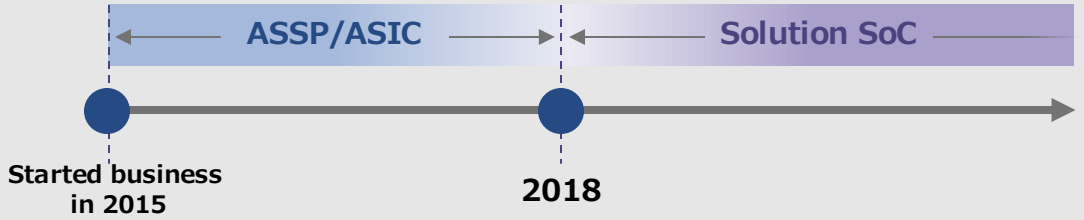
3 New wafer test technology challenges for leading-edge SoC
- High-power control wafer testing
- High-speed wafer testing
- Linking and further utilizing big data
- Yield control by real-time adaptive testing

4 Conclusion

A “Solution SoC” company with rich experience in diverse markets leading innovations with customers around the world.

Company Overview

History



Business Description

Fabless Custom SoCs

Capital
(As of March 31, 2024)

32.6 billion yen

Employees*1
(As of March 31, 2024)

Global Employees	Approx. 2,500
Engineers*2	Approx. 1,900

Key Financials FY24/3

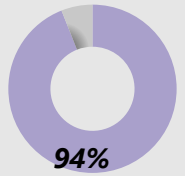
Net Sales	Net Sales Growth (YoY)	OP Margin
221.2 billion yen	14.8%	16.1%

Business Overview (Ratio is NRE revenue breakdown for FY24/3)

Business Model

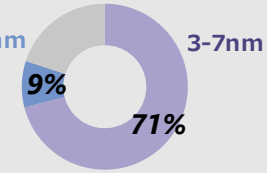
Solution SoC
(Optimal Custom SoC)

Primary Areas

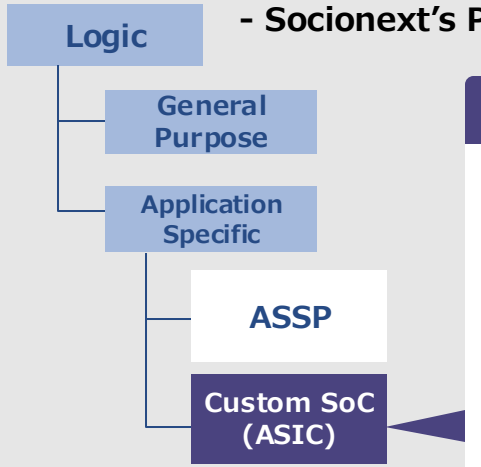


“Automotive” “Data Center & Networking” “Smart Devices” ”Industrial”

Process Node



- Socionext’s Positioning in Semiconductor Market -



Market Size
$25bn*4 in 2023

Types of Custom SoC(ASIC) Business Models*3

- Strength within the Automotive, Data Center & Networking and Smart Devices applications
- New and distinctive business model
- Provides cutting-edge custom chips for innovative customers

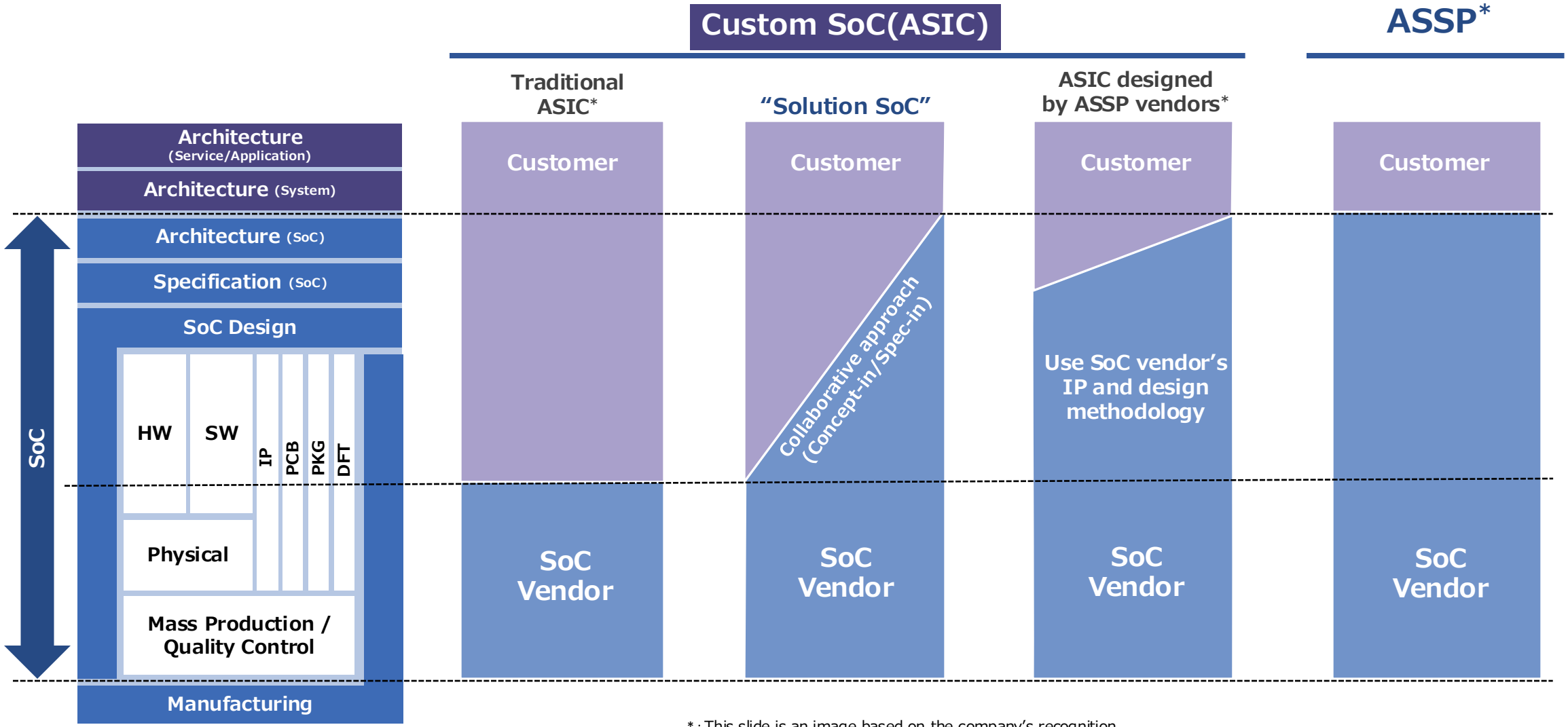
Three business models

- Traditional ASIC
- Solution SoC — New and distinctive business model
- ASIC designed by ASSP vendor

*1: Numbers of employees and engineers are on a consolidated basis
*2: Number of staff working in divisions relating to technical development and analysis in and outside Japan
*3: Classifications of these business models are based on our own assessment
*4: Market Size estimated by Socionext based on Omdia data ”Competitive Landscaping Tool CLT, Annual- 4Q23”. All market sizes are calculated in terms of USD-based revenue

1. About Socionext (“Solution SoC” Business Model)

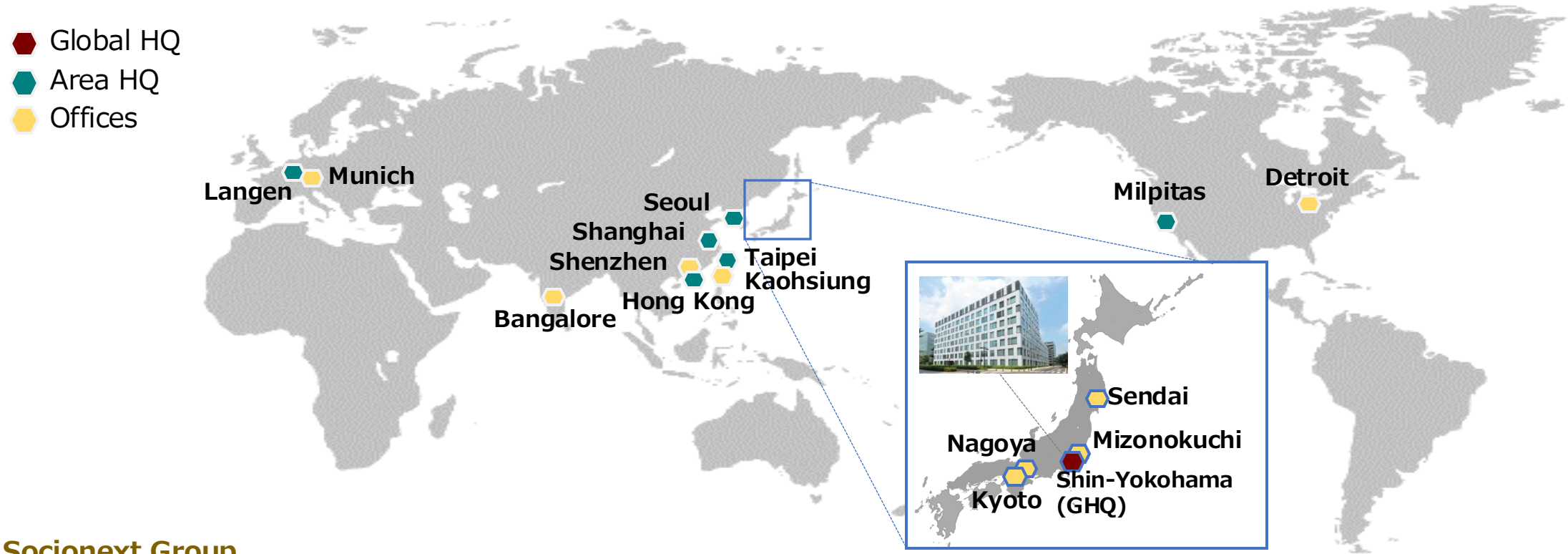
- The primary difference between “traditional ASIC”* and “Solution SoC“ is how to interface with customers
- The primary difference between “Solution SoC” and “ASIC designed by ASSP vendors”* is the breadth of optional customization



*: This slide is an image based on the company’s recognition.
This graphic provides an illustrative framework of the types of industry players based on the company’s classifications.

1. About Socionext (Locations Japan and Global)

Worldwide Support Organization Provides High Quality Service to Customers



Socionext Group

Socionext Inc.
Shin-Yokohama(GHQ), Kyoto, Nagoya, Mizonokuchi, Sendai, Taipei, Kaohsiung

Socionext America Inc.
Milpitas(CA), Detroit(MI), Bangalore(India)

Socionext Europe GmbH
Langen, Munich(Germany)

Socionext Technology Pacific Asia Ltd.
Hong Kong

Socionext Technology (Shanghai) Co.,Ltd.
Shanghai, Shenzhen

Socionext Taiwan Inc.
Taipei

Socionext Korea Ltd.
Seoul

2. Technology trends for leading-edge SoC products (HPC)

■ Focus segment for Data Center & Networking

Multi Core CPU

AI Accelerator

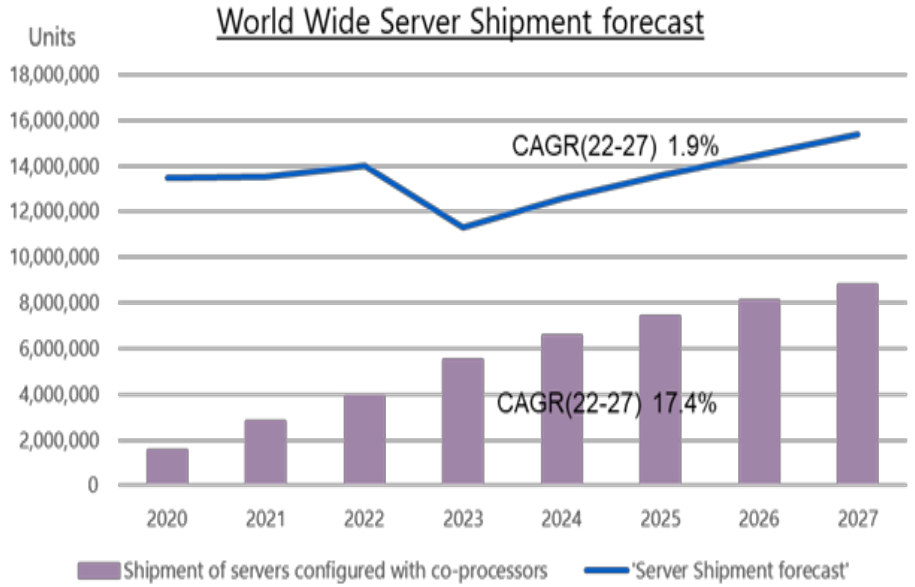
5G Wireless

Wired Network

Storage

Optical Transporter

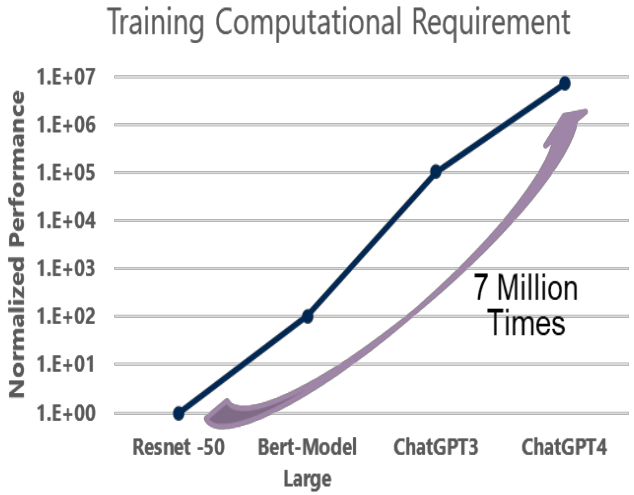
■ The market of server with co-processor is a growing market for CAGR(22-27) 17.4%

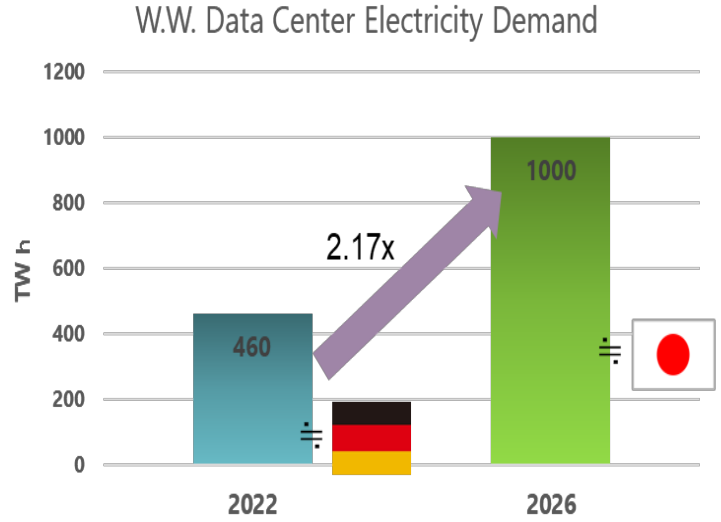


Created by SOCIONEXT based on OMDIA Long range server forecast -2H23

■ Power consumption issues due to the spread of AI

	2015	2018	2022	2023
AI Model	Image recognition Resnet	Natural language BERT model	ChatGPT-3	ChatGPT-4





Created by SOCIONEXT based on
1 Tom B. Brown et. Al [2005.14165] Language Models are Few-Shot Learners (arxiv.org)
2 Shreyas Saxena et al. [2303.11525] Sparse-IFT: Sparse Iso-FLOP Transformations for Maximizing Training Efficiency (arxiv.org)
3 https://lambdalabs.com/blog/demystifying-gpt-3

Created by SOCIONEXT based on IEA "Electricity 2024 Analysis and forecast to 2026"

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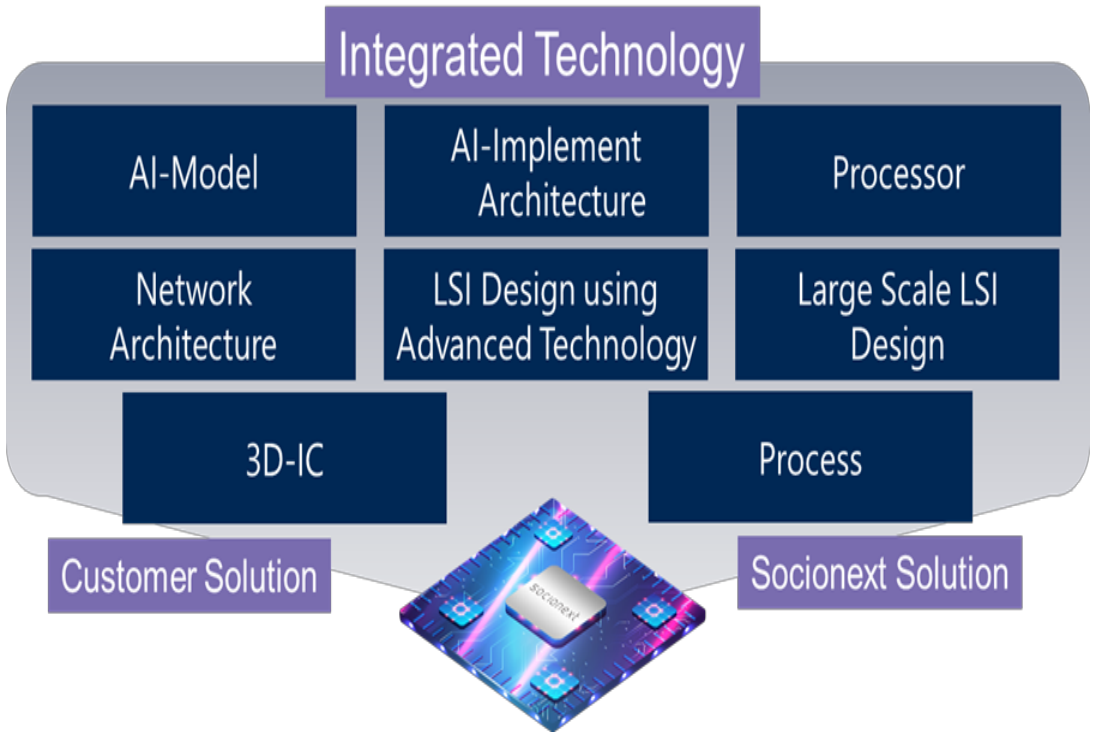
2. Technology trends for leading-edge SoC products (HPC)

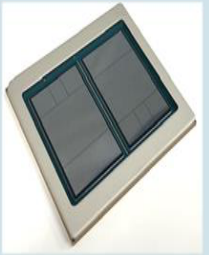
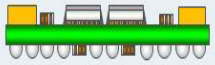
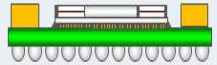
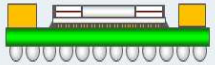
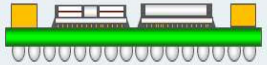
■ AI & Network trend

- ✓ Data center semiconductors will continue to drive technology.
- ✓ On the other hand, it is also a factor contributing to the global power challenge.
- ✓ Socionext aims to balance technology evolution and power challenges with Integrated Technology.

■ Symphony of technological breakthroughs



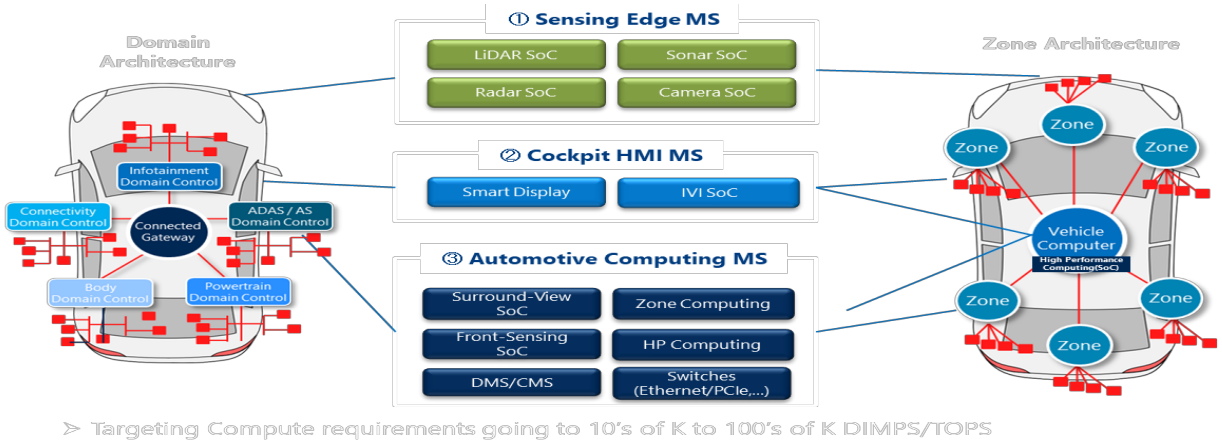
■ Chiplet package experiences

	Device-1	Device-2	Device-3	Device-4
Appearance				
Structure	 2x SoC Die Capacitor	 1x SoC Die 4x HBM2E Si interposer w/ capacitor	 1x SoC Die 4x HBM2E Si interposer	 4x SoC Die 4x HBM3 Bridge/RDL interposer
Package	MCM-FCBGA	2.5D-FCBGA	2.5D-FCBGA	2.5D-FCBGA

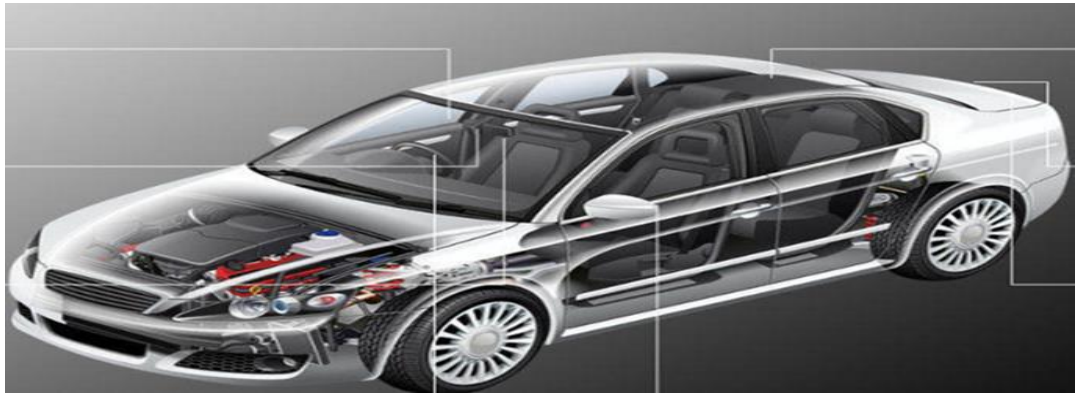
2. Technology trends for leading-edge SoC products (Automotive)

■ Automotive architecture evaluation

- ✓ As autonomous driving levels evolve, E/E architecture shifts from distributed to domain/zone architectures.
- ✓ An increasing need for high-performance, leading-edge SoC is increasing with customers (OEM, new ventures, etc.) seeking differentiation and # of ECU optimization

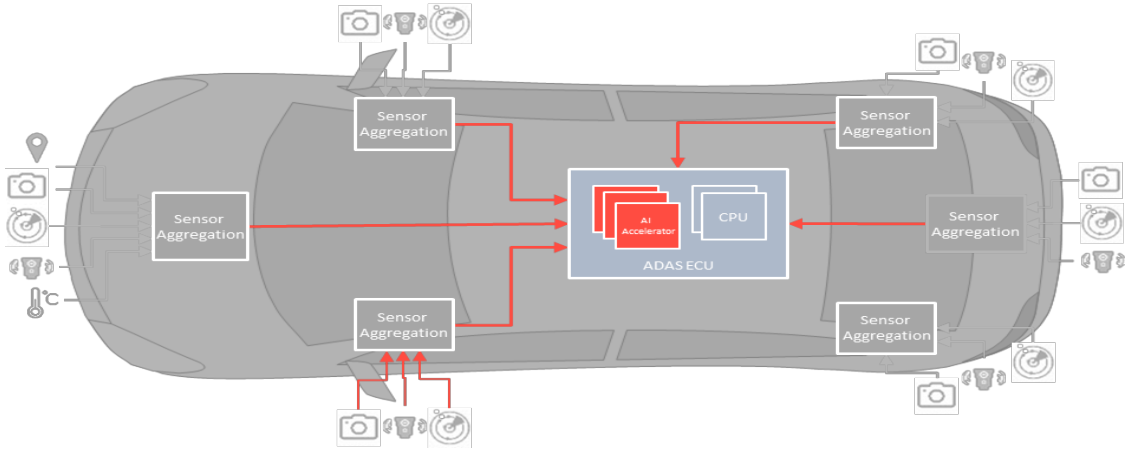


➢ Targeting Compute requirements going to 10's of K to 100's of K DIMPS/TOPS



■ ADAS-compute architecture

- ✓ Automotive ADAS is Datacenter in CAR with Camera/LiDAR/Radar Sensor fusion
- ✓ Automotive ADAS requirements similar to Datacenter: Customers requiring leading foundry technology node



■ Custom SoCs for Automotive

- Create and manufacture dedicated SoC to Automotive application with customer requiring specifications
- Cooperate to define SoC architecture together so that only one SoC and No overhead and suitable functionality and performance
- Integrate customer designed logic in to SoC
- Available to use Si confirmed IP and edge packaging technique used in other Automotive Center SoC

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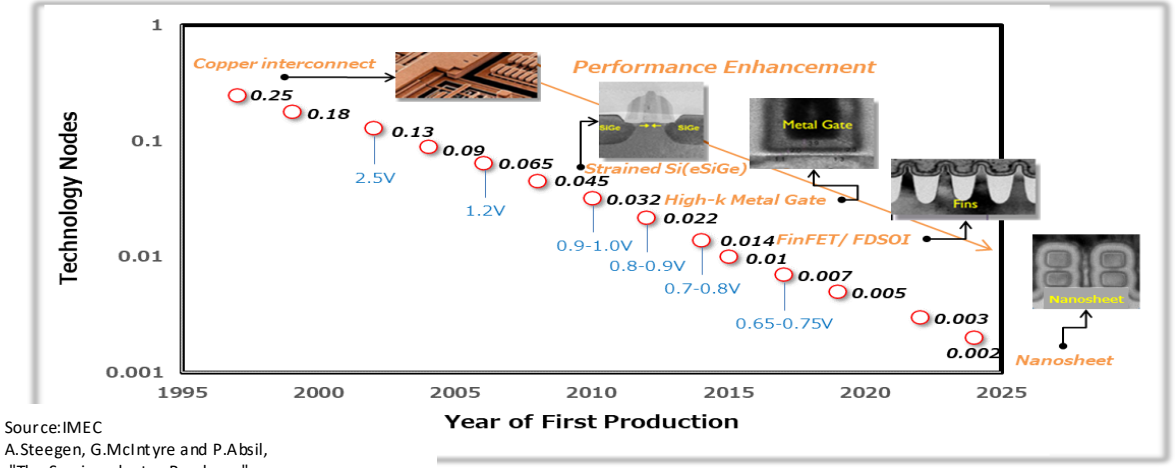
2. Technology trends for leading-edge SoC products

■ Deep dive into leading-edge process technology

Scaling roadmap of device architecture

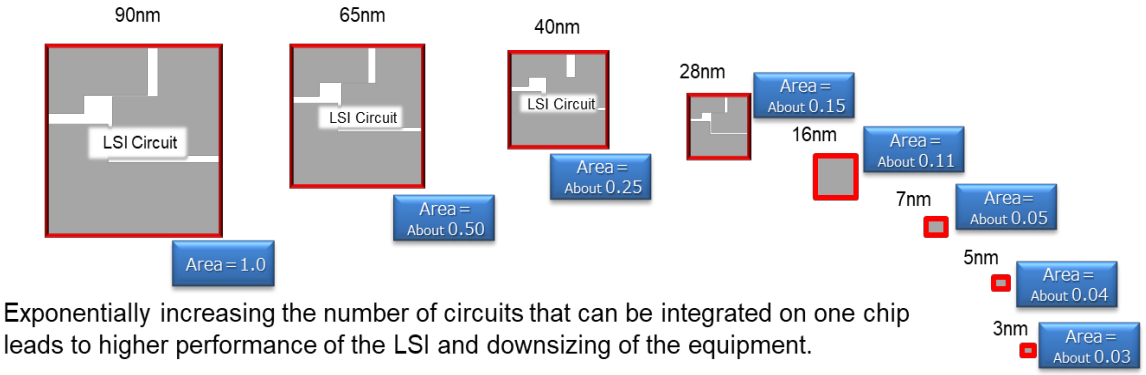


Source:IMEC
A.Steegen, G.McIntyre and P.Absil,
"The Semiconductor Roadmap",
IMEC Technology Forum Japan, Nov. 2014

■ Drive SoC scaling with leading-edge technology

Boosting circuit density by technology node migration

■ Area trend where the same function is realized (Area of 90nm is 1).

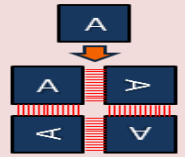
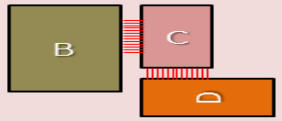
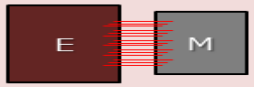


Exponentially increasing the number of circuits that can be integrated on one chip leads to higher performance of the LSI and downsizing of the equipment.

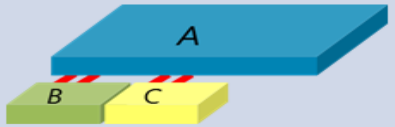
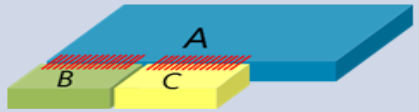
■ Chiplets concept

Breaking the limits of a single chip performance with optimized combination of dedicated chips

■ System Configuration with Multiple Chips

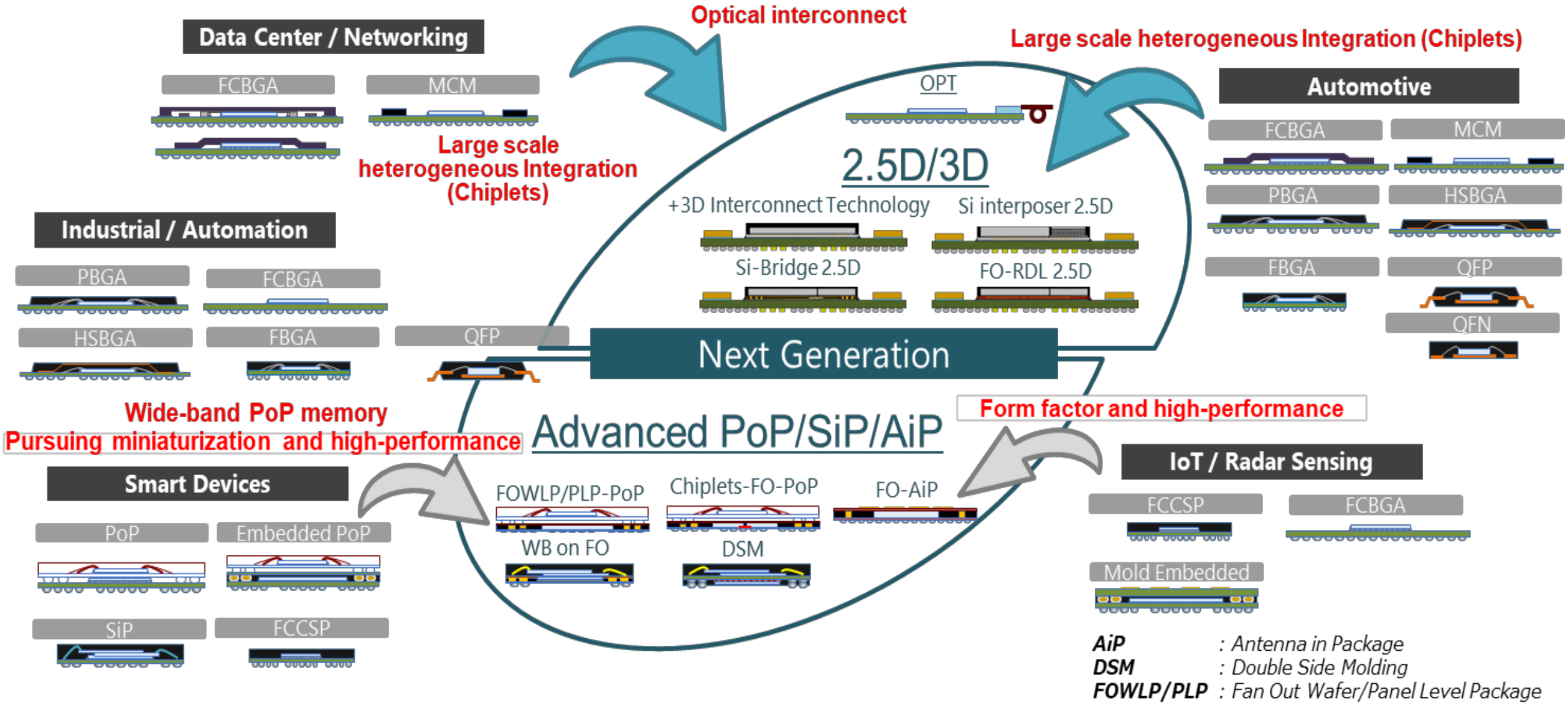
Large scaling integration	Optimal selection by performance	Logic/ memory configuration
		
Multiple die break through the monolithic scaling limitation.	System integration by using advanced logic technology and legacy analog chip combination.	System configuration with logic LSIs and memory LSIs on a package.

■ Chiplets Concept

	Conventional SiP	Chiplets
Structure		
IF between chips	Conventional IF	Specific IF with low power and low latency
Interconnect technology	Wire or Bump interconnection on the conventional package substrate	Wide bas parallel interconnection with fine pitch interposer and TSV-3D stack or High speed serial interconnection on the conventional package substrate
Performance	≦ Monolithic SoC * Worse power efficiency and latency	≧ Monolithic SoC * To compensate the demerit of SiP by specific IF and to enable low-cost solution

2. Technology trends for leading-edge SoC products

■ LSI packaging technology trend　Packaging technologies for application requirements



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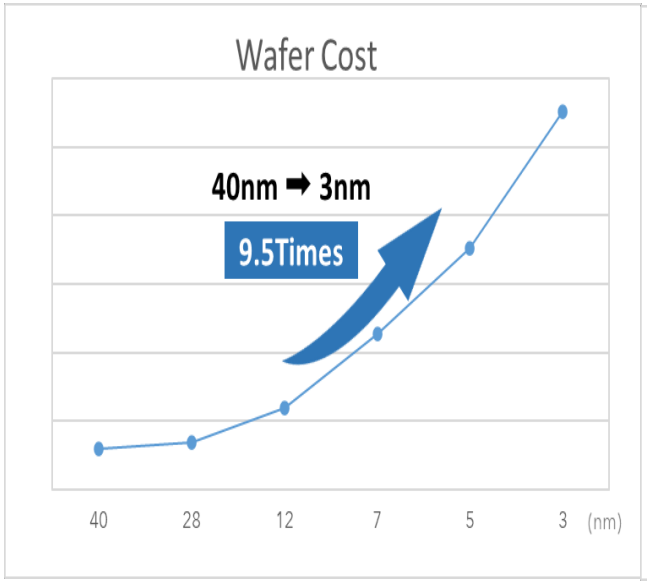
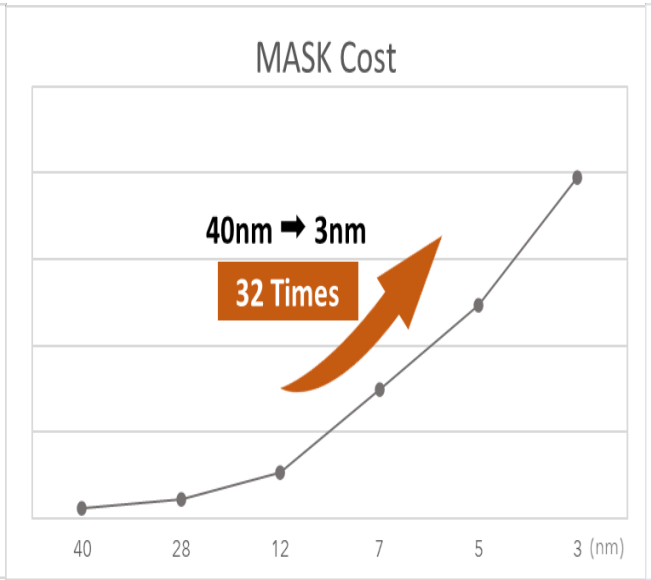
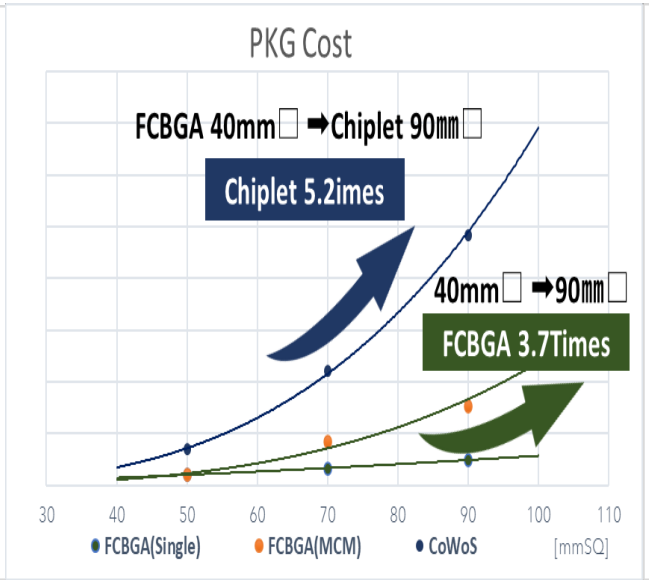
3. New wafer test technology challenges for leading-edge SoC products

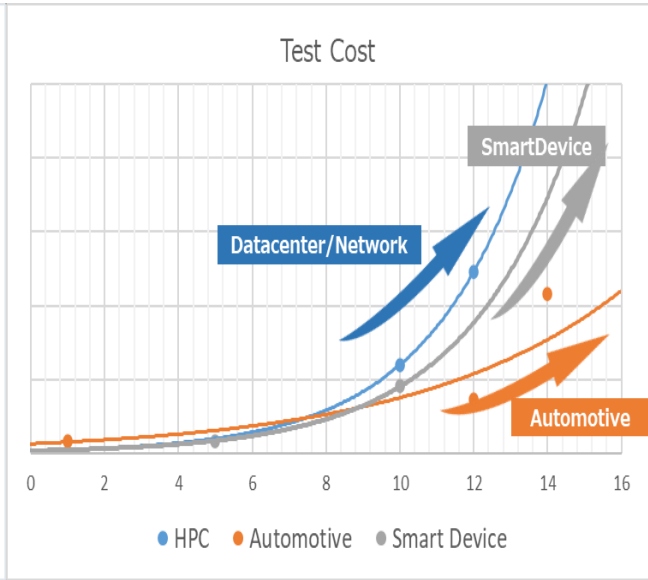
■ Yield improvement is key

Analysis of failure factors by test and early feedback to design/manufacturing is important.
For this purpose, advanced test technology for leading-edge SoC is required.





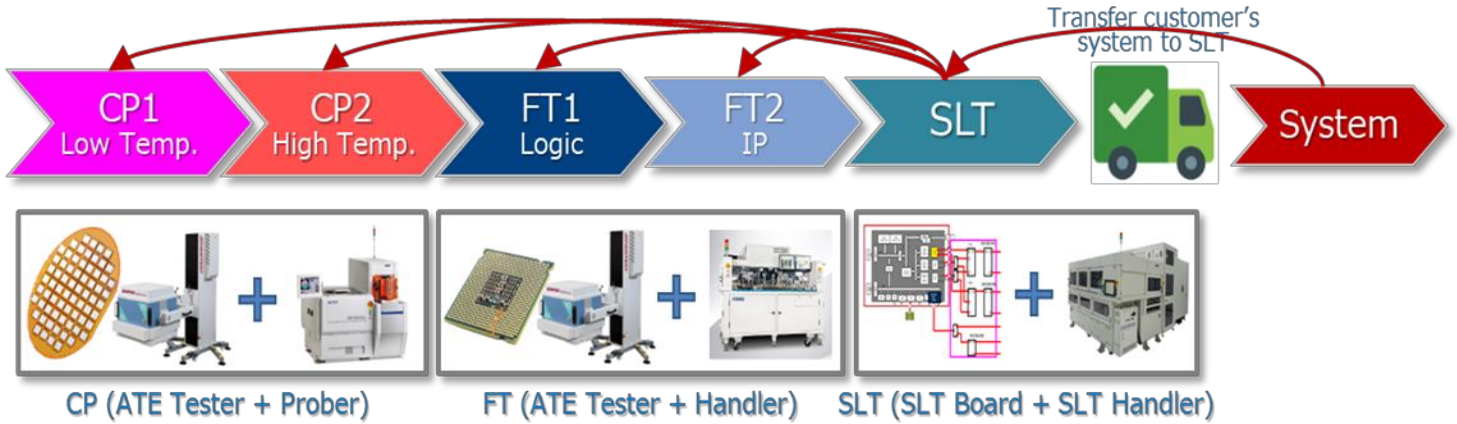




★**Ex. Production cost ratio** Yield improvement effect：Test cost improvement effect → **10：1**

■ Requirements for leading-edge SoC testing

- High-pin count, high-power control, high-speed, high precision and high-quality test in wafer test process.
- Reduction of production cost by feed forward (shift left) test contents from SLT/FT result to wafer test process.



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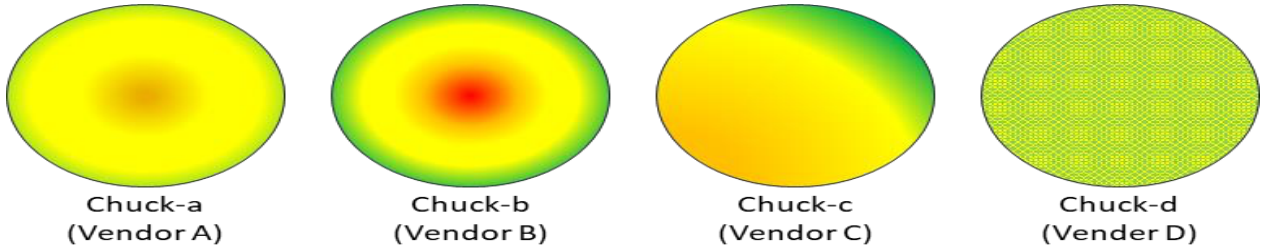
3. New wafer test technology challenges for leading-edge SoC products

■ High-power control wafer test (leading-edge SoC temp control issues 1)

Test temp guarantee for advanced SoC's large temp(Tj) variations.

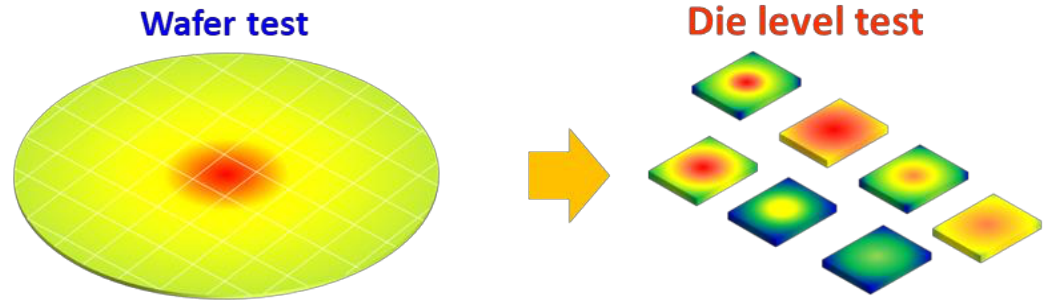
Solution ①.Evaluating new Prober/Chuck ②.Evaluating Die Level Test Solution
③.Test guard band compensation ④.Using ATC(Active Thermal Control) Handler during FT

① Ex. Evaluating new prober/chuck



	Chuck-a	Chuck-b	Chuck-c	Chuck-d
Temp accuracy	+/- 1.0C	+/- 2.0C	+/- 1.0C	+/- 0.5C
Temp sensor	1	16	16	5
Temp residence	0.5C/W	0.4C/W	0.2C/W	0.5C/W
Flatness	20um	25um	40um	40um

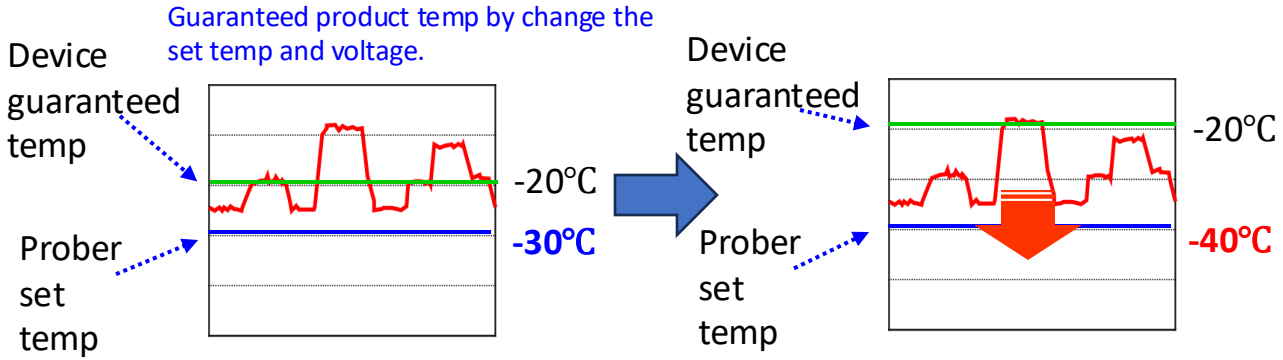
② Ex. Die level test solution



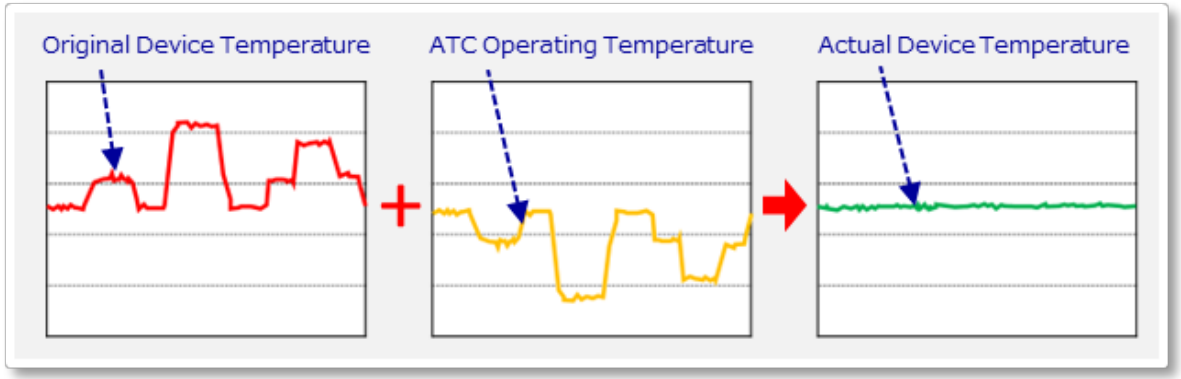
When the temp of the die being tested increases, the temp of the surrounding die also increases.

The dies with different temp tendencies can be tested separately.

③ Ex. temperature guarantee case



④Ex. FT ATC use case



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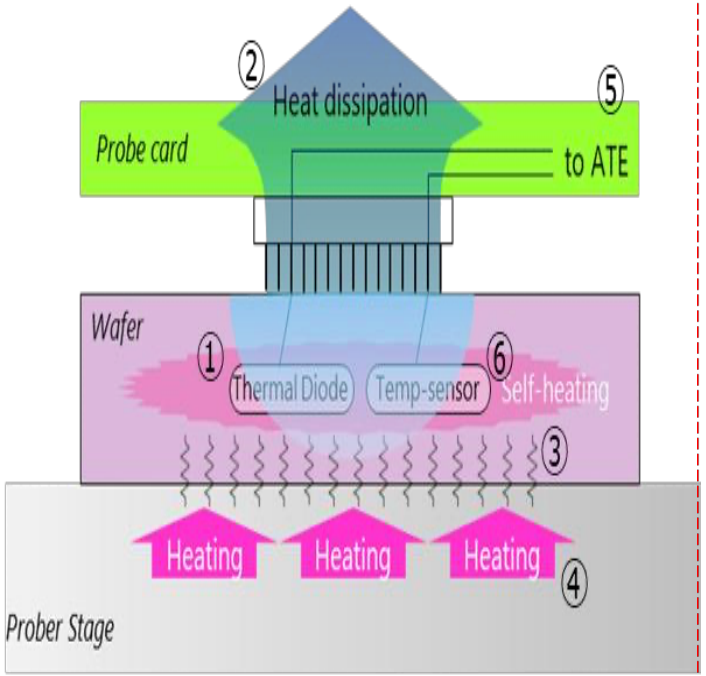
3. New wafer test technology challenges for leading-edge SoC products

■ High-power control wafer test (leading-edge SoC temp control issues 2)

Accurate measure of temp sensor IP (write temp trimming result to E-fuse in SoC)

Several temp environmental errors occur in the wafer test process during temp sensor measurement (①,②,③ have variation errors and ④,⑤,⑥ have fixed errors). The temp sensor can correct the result by the trimming function, but if there is an error in the temp measurement, it cannot correct accurately.

Error types and elements



Write the optimum temp sensor value considering the error to E-fuse.

①Thermal Diode accuracy
・process variation

②Heat dissipation by Probe Card
・Pin count
・Test Temperature

③Contact thermal resistance
・Contact resistance

④Prober temperature accuracy
・Prober/Chuck accuracy
・Temp measurement point,
・Temp feedback function

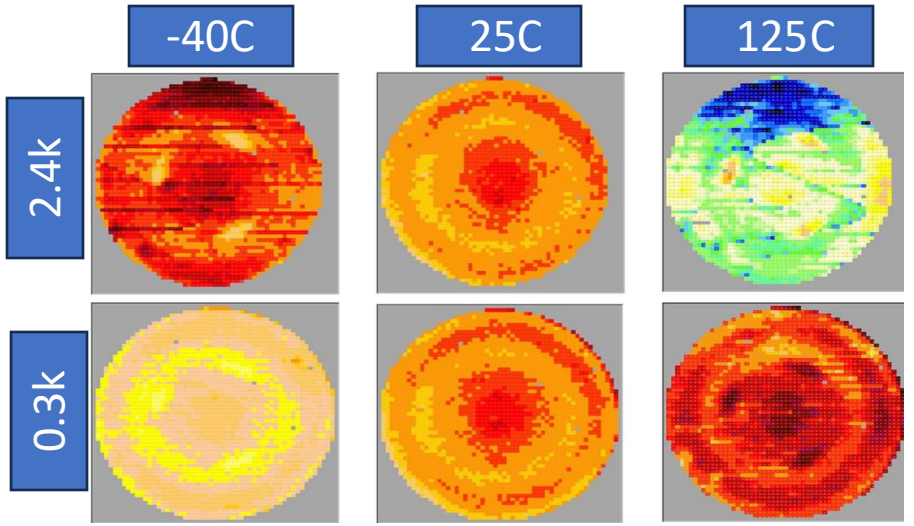
⑤Tester measurement accuracy
・Temp-sensor measurement

⑥Temp-sensor IP macro
・Trimming error
IP macro accuracy

variation error
fixed error

① ② ③ ④ ⑤ ⑥

Temp error due to the probe card



Probe card heatsink impact
(2.4k pins and 0.3k pins probe cards)

Especially in high/low temp environments, the larger the number of needle pins, the larger the temp variation effect.

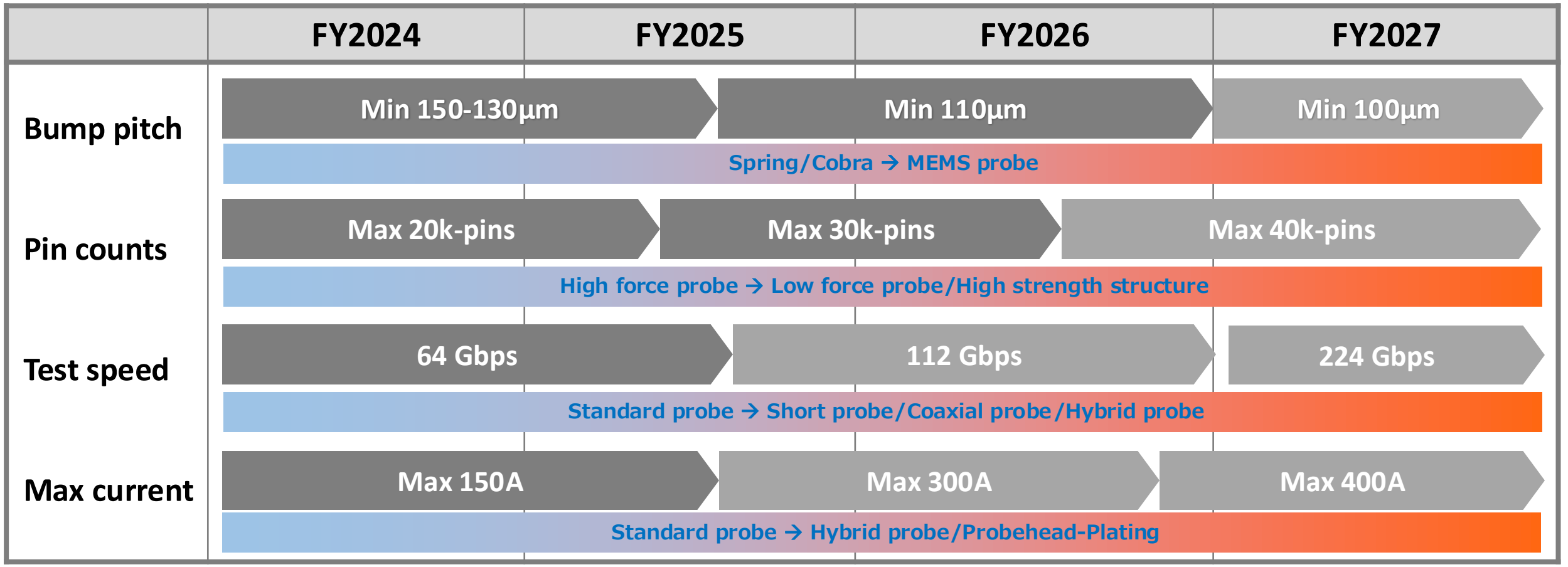
3. New wafer test technology challenges for leading-edge SoC products

■ High-speed wafer test

In leading-edge SoC, the manufacturing cost(Chip/PKG/HBM) and the quality improvement requirement (ADAS(high detection rate requirement), HPC (silent data corruption)) are big issues.

We need high-speed I/F wafer testing and better the characteristics of high-speed probe cards.

■ Probe card trends for advanced SoC (Our company survey)



socionext

3. New wafer test technology challenges for leading-edge SoC products

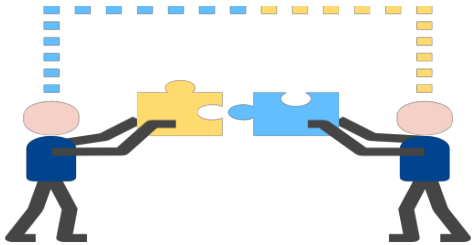
■ High-speed wafer test

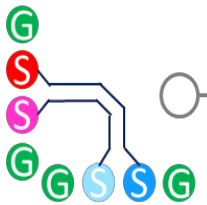
The leading-edge SoC require consideration of high-speed signal integrity, integration of high-power density and temp management as wafer testing.

To address these challenges, Socionext is currently collaboration with MPI to design and evaluate probe cards for new advanced chiplet products.

MPI is a reliable probe card partner with excellent support in Taiwan that can provide the high-speed, high-accuracy and customizability required for advanced SoC products.

socionext™ x MPI



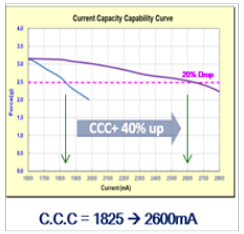


High-Speed Capabilities

- Well impedance control for high-speed test
- SerDes 112G in mass production stage
- SerDes 224G ready to release

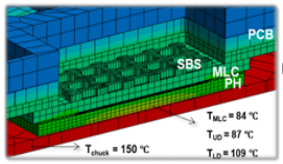
PAM4-56Gbps

PAM4-112Gbps



High Power Density

- Well contact stability in C4 and needle tip
- Current load balancing technology
- Higher CCC Performance / Higher MTBF

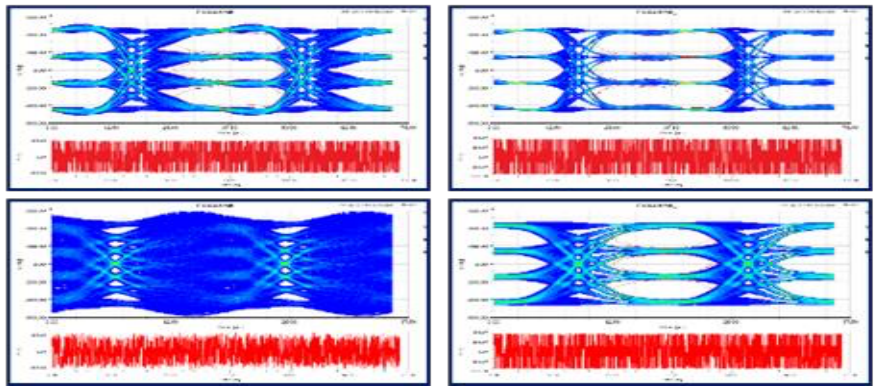


High Strength Mechanism

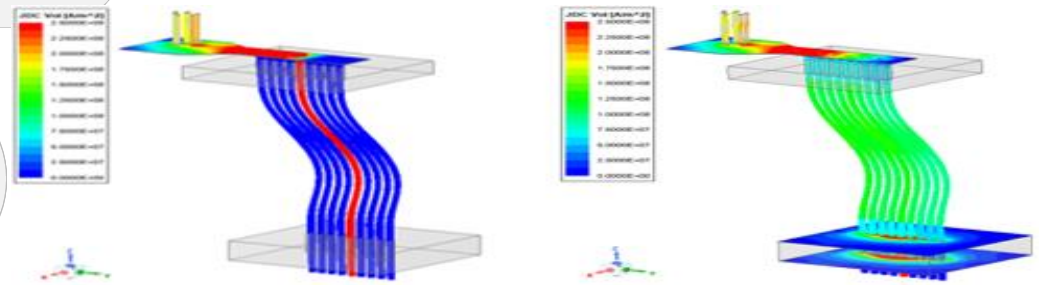
- Accommodate from -40° c to 150° c
- Over 12,000 pins for pitch 40um pad
- Over 50,000 pins MEMS probe card

MPI

Standard Design | **Z56/Z112 Solution**



Current Diverting Guide Plate
Patent no. US 9423424B2

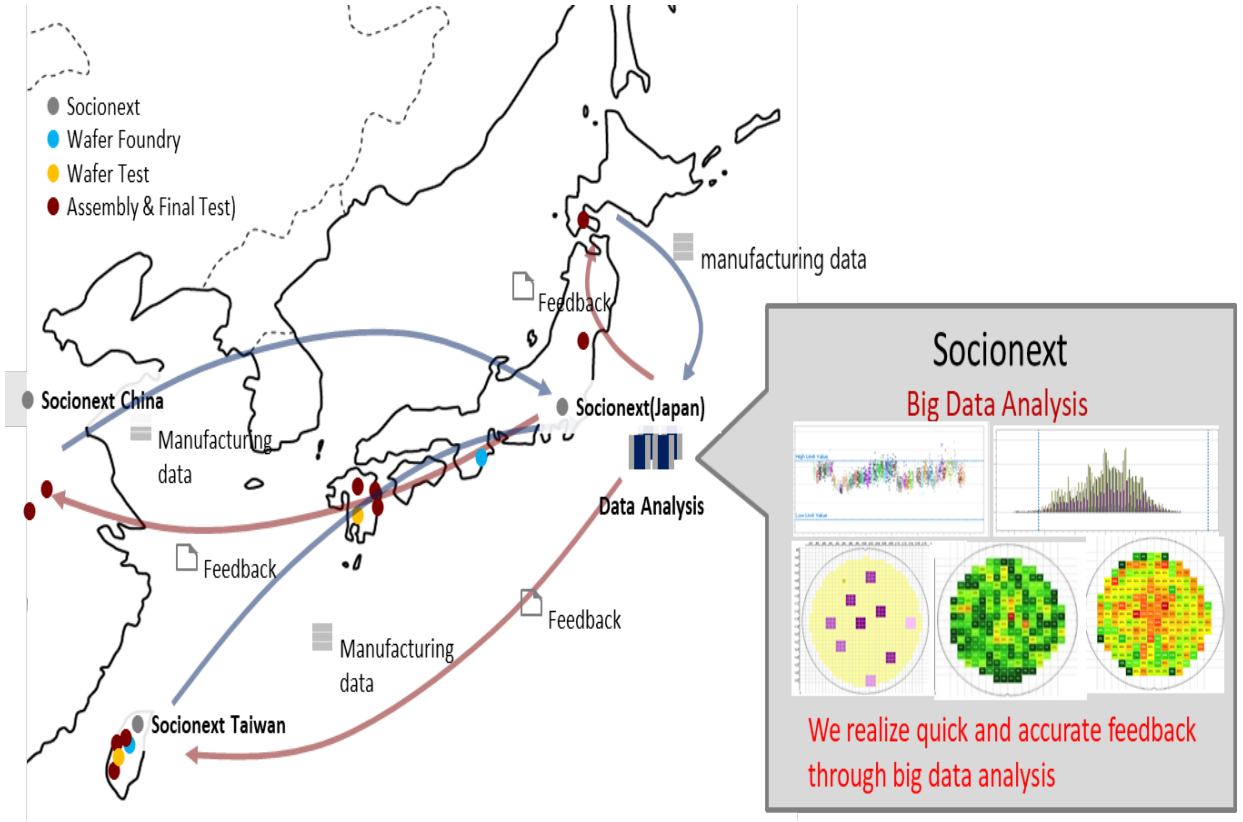


3. New wafer test technology challenges for leading-edge SoC products

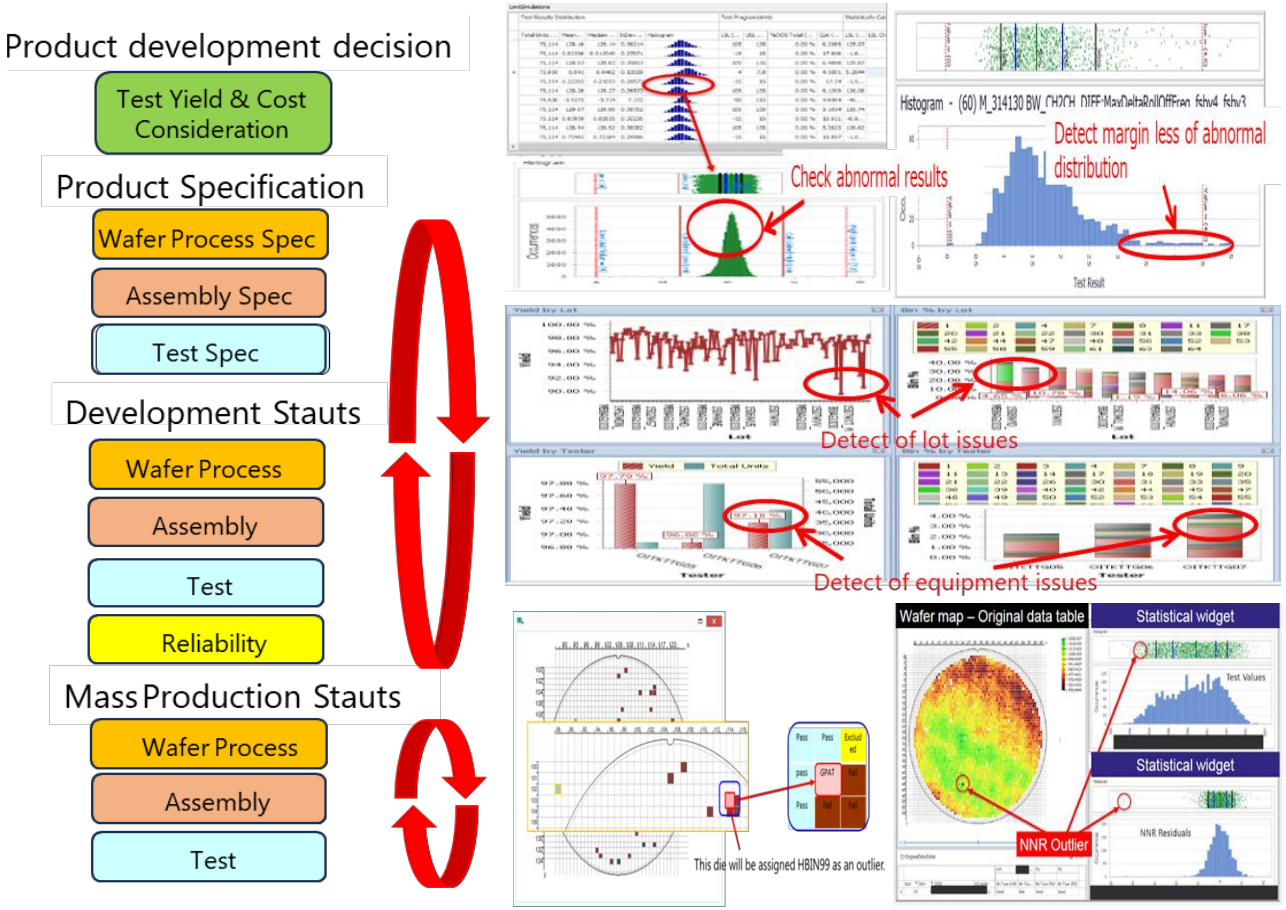
■ Linking and further utilizing big data

We can share the analysis results of manufacturing data of all products instantaneously from manufacturing bases in the world such as Taiwan. We have already established big data application flow from development to mass production.
We have established high-quality and stable product supply as a fabless enterprise by these data cooperation.

- Cooperation through an outsourcing management system
- Quickly collection, analysis, and monitoring of big data



- Utilization of big data from development to mass production



3. New wafer test technology challenges for leading-edge SoC products

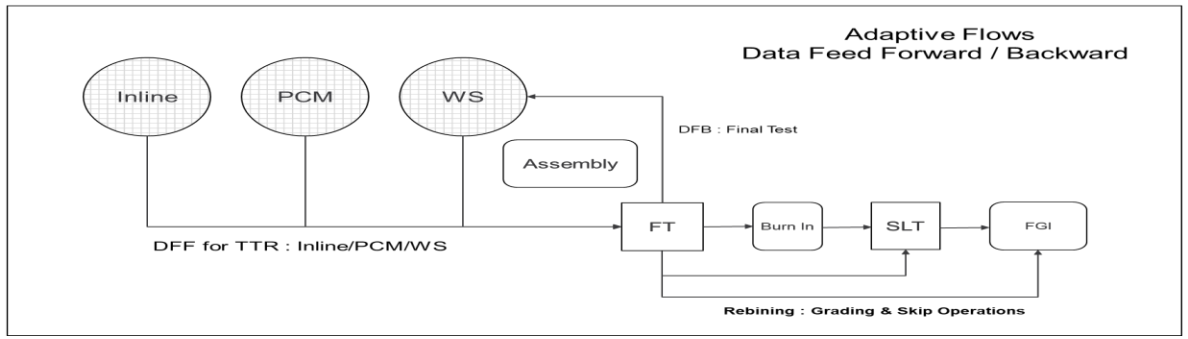
■ Yield control by real-time adaptive testing

- Consolidate and link existing big data and AI/ML for yield prediction and analysis to further improve yield and quality.
- Adaptive test technology which changes test condition from the analysis result in real time is necessary for the realization.
- Socionext collaboration with National Instruments(Optimal Plus), which has a lot of technology and experience in this field.
- We have already applied the adaptive test in several products, and the near real time adaptive test is also under final feasibility study.

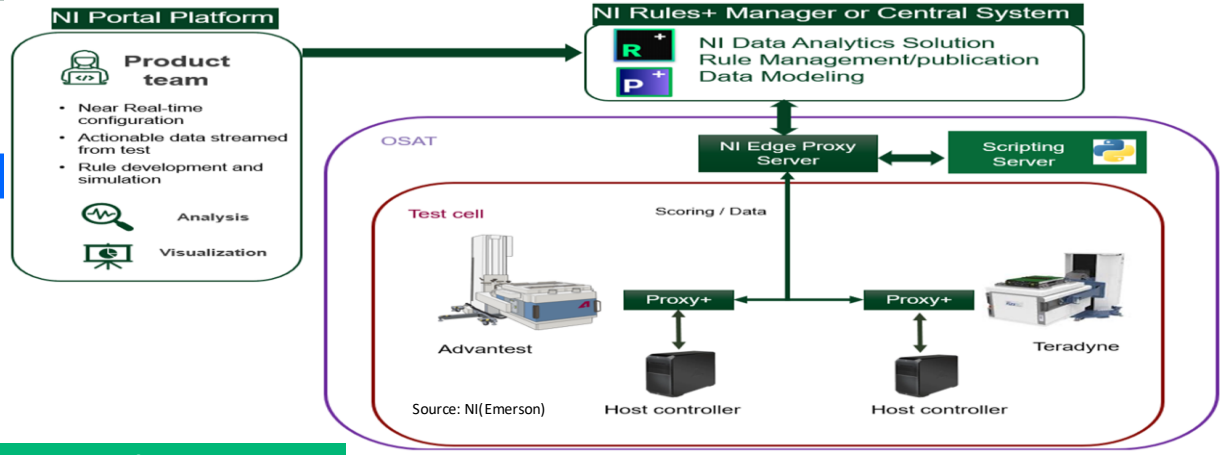
NI + Edge Solutions

Offering	Model Execution	Use Cases	Systems	Execution Timing
Near Real Time	Run Level	Offline Data Feed Forward (For Smart Operation Flow Re-binning)	NI	Cached @ Run start (offline)
Real Time	Device Level	Offline Data Feed Forward with Online Data (Advanced Binning)	NI NI + ACS NI + Archimedes	100's msec
Ultra Real Time	Test Level	Offline Data Feed Forward with Inline Data (Smart Test Flow)	NI + ACS/Teradyne	10's msec

Advanced Semi Test Flows



NI Near Real Time Solutions



In Deployment

Near Real Time Option:

- Customer or NI developed ML Models
- Model delivery and Data Feed Forward thru NI Edge Proxy Server
- Run level (lot to lot) or device level Model Execution thru Dockers and Test Program API

Use Case: Device binning for reduced post test operations (BI/SLT)

3. New wafer test technology challenges for leading-edge SoC products

■ Yield control by real-time adaptive testing

- We are considering the application of ultra real time solution as a future target. We will need collaboration with NI and ACS, who have a lot of technology and experience in this field.
- Chiplet products have variety of potential defects, and testing of these potential defects can result in significant losses.
- As a countermeasure, we are considering applying ultra real time test solution based on the history of big data and AI/ML results of each chip.

NI + Edge Solutions

Offering	Model Execution	Use Cases	Systems	Execution Timing
Near Real Time	Run Level	Offline Data Feed Forward (For Smart Operation Flow Re-binning)	NI	Cached @ Run start (offline)
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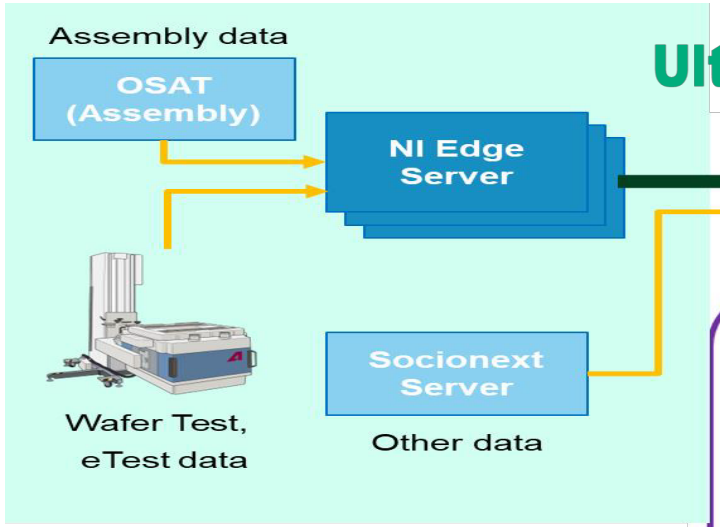
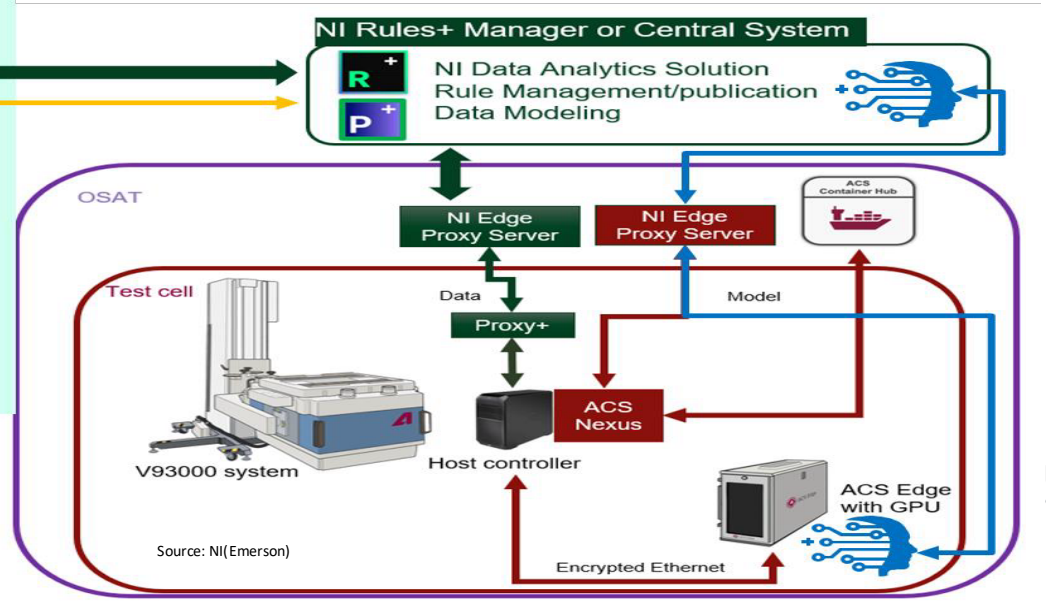


Ultra Real-Time Solution



Chiplet Products

- Advanced process
- some core chips + some HBM

Chiplet Test Fails on due to:

- Bad Unit
  - Lower Margin / Out of Spec Limits
  - Assembly Issue
  - Corrupted circuit
- Measuring System
  - Weak Contact
  - Site by Site difference
  - Repeatability
  - Accuracy
  - Temperature

Yield Loss that caused by technology limitations

Reduce Failure Judgement on Good units

- Recovery failed units by AI/ML technology if possible
  - Retest with spec change
  - Skip Tests
  - Grade Sorting

4. Conclusion

■ Conclusion of the presentation

Change in testing with leading-edge SoC

- Yield improvement is key
  demand for improved yield
- Importance of failure factor analysis by testing
- Importance of early feedback to design and manufacturing by testing
- Expectations for “Shift Left”
  Improved wafer test technology

Challenge for new test technology

- Temp control technology
  Test temp assurance issue
  Test temp accuracy issue
  Die level test solution
  Wafer level ATC solution
- High-speed wafer test
  Hybrid probe card technology
- Big data linkage
  Real-time testing using big data and AI/ML

Importance of collaboration with test partners

- Test partner support for new test challenges
- Let's great advanced test challenge together and grow together.

We will continue to provide high quality and stable supply of leading-edge SoC products of Socionext to various customers using advanced test technology. We need the support of our testing partners to take on new testing challenges.
We ask for your support and cooperation, and we would like to take on this great challenge and advance together.

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