



On PCB with 50Gbps for ATE board, Characteristic improvement Approach

OKI

Takahiro Yagi
OKI Circuit Technology Co., Ltd.

Overview

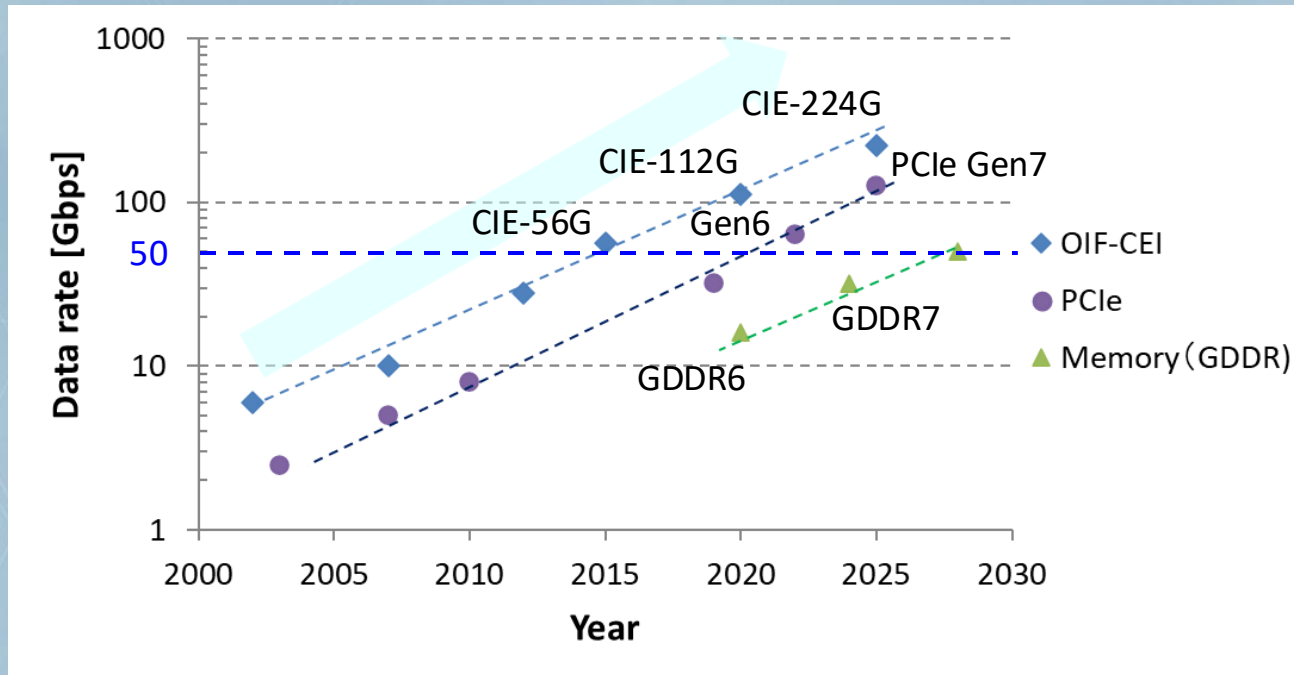
- **Background**
- **High-speed PCB trends**
- **Challenges for High-Speed PCB**
- **Flow for development of High-Speed PCB**
- **PCB characteristic improvement**
- **Development examples**
- **Correlation between Simulation and measurement**
- **Conclusion**

Background

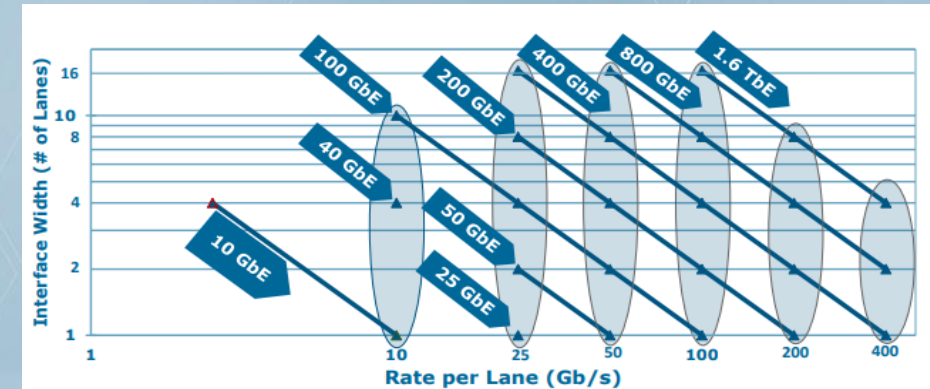
- Data Rate Doubled in 3 to 4 years : exceeding 56Gbps
- PCB are also required to perform at 50GHz or more

Ex:

- Nyquist frequency of 56G-PAM4 : 14GHz
- The 3rd harmonic : 42GHz



The Relationship Between Ethernet & Signaling Rates



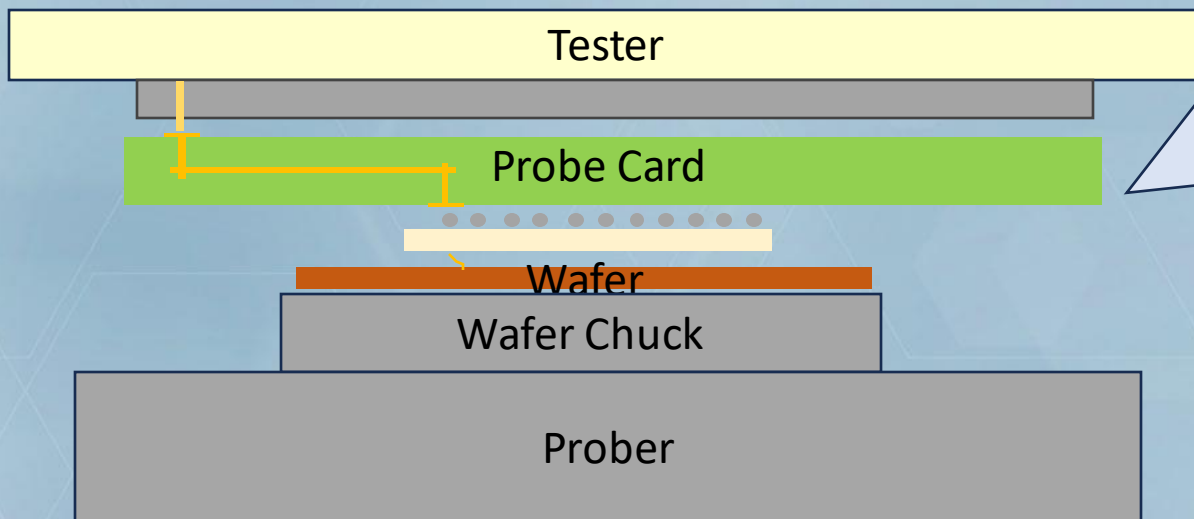
Source: [IEEE 802.3 Beyond 400 Gb/s Ethernet Study Group](#)

Data rate and Nyquist frequency

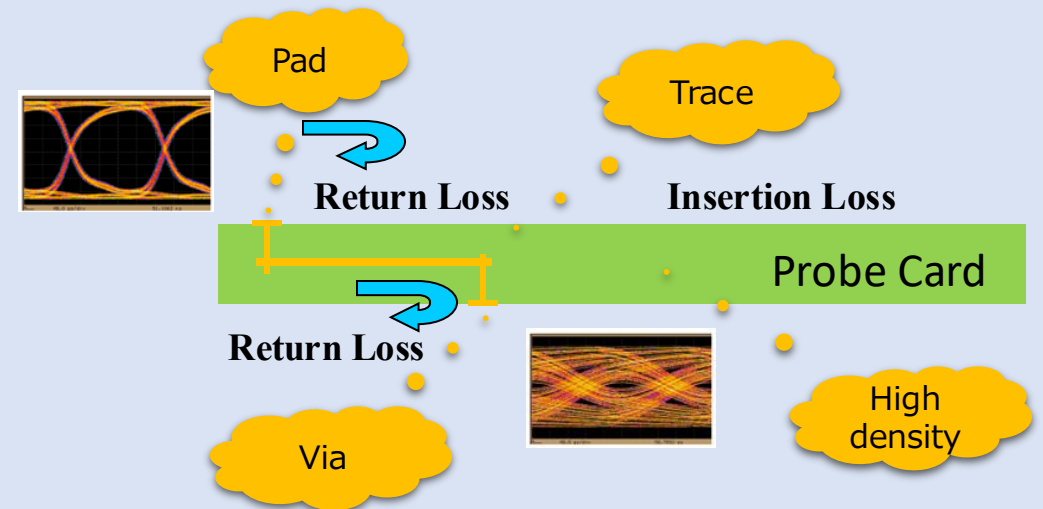
| Data Rate | Encoding | Nyquist Frequency |
|-----------|----------|-------------------|
| 56Gbps | PAM4 | 14GHz |
| 64Gbps | PAM4 | 16GHz |
| 56Gbps | NRZ | 28GHz |
| 112Gbps | PAM4 | 28GHz |
| 128Gbps | PAM4 | 32GHz |
| 224Gbps | PAM4 | 56GHz |

Background

- Signal speed in wafer testing is increasing
Probe Card also required to support high-speed signal
→ Reducing loss and reflection of pads and vias



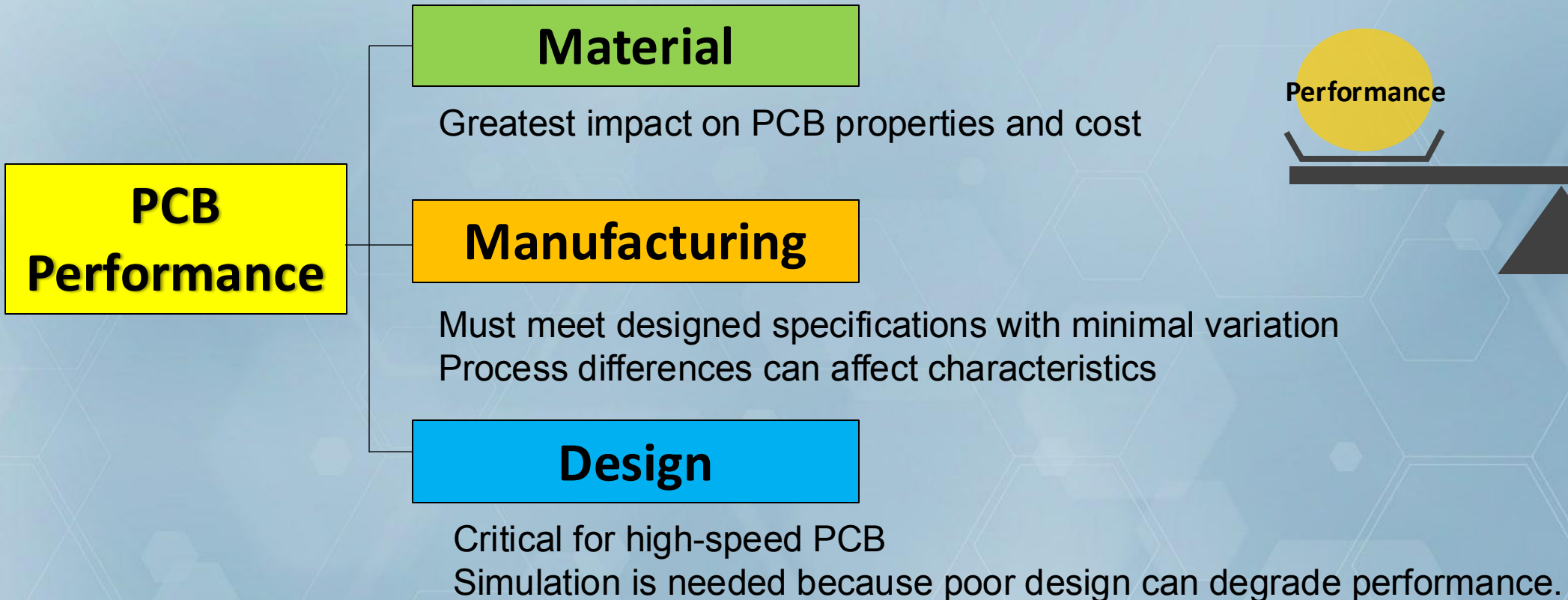
Challenges of high-speed PCB



- Increased loss and reflection
- Eye pattern does not open

Background

- Three factors of PCB Performance : Material, Manufacturing, and Design
→ These factors must be balanced with performance and cost

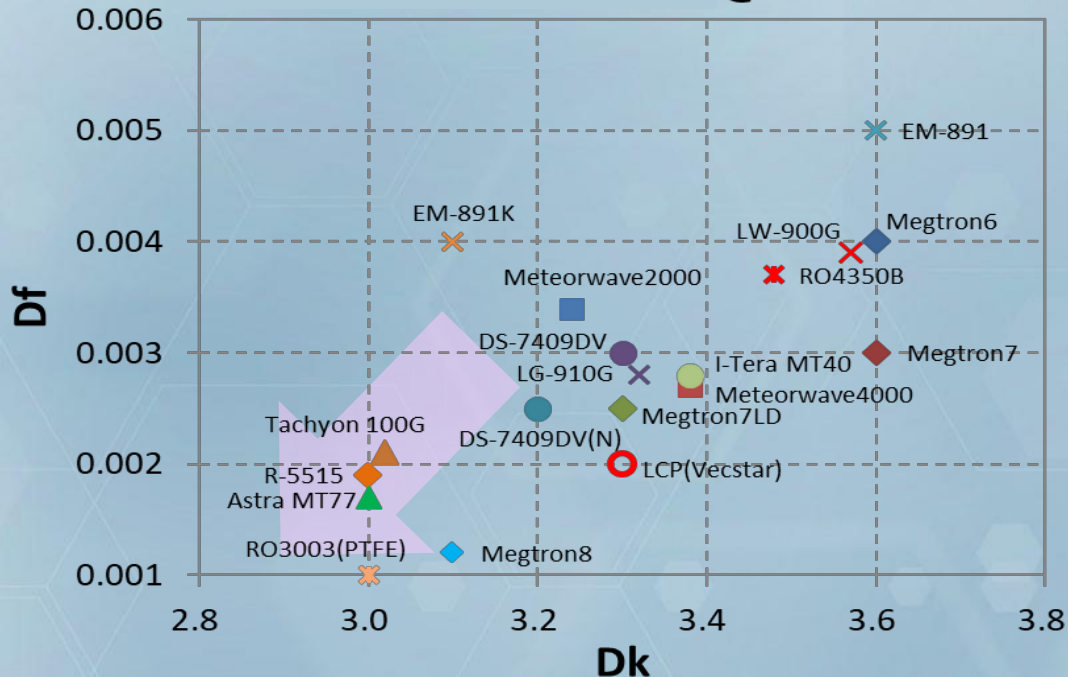


High-speed PCB trends

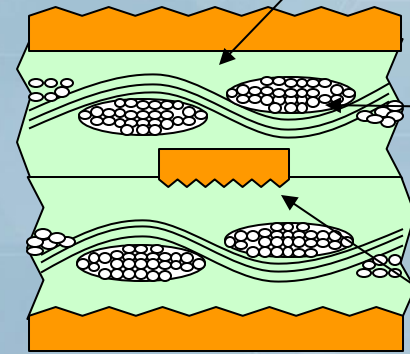
- Approach by materials

Evolution to Low-Dk/Df (Dk : 3.0, Df : 0.001 and less)

Low loss materials @10GHz



✘ Nominal value of material suppliers
Using values measured by our TEG in simulation



Resin

Base resin, Filler
Dielectric Loss $\propto \tan \delta \times \sqrt{\epsilon r} \times f$

⇒ Low-loss

Glass cloth

Glass Fiber (Low-Dk glass) ,
Cloth style (Filament diameter, bundle pitch)

- Thinner
- Low-Dk
- Cloth less

⇒ Low-Dk glass

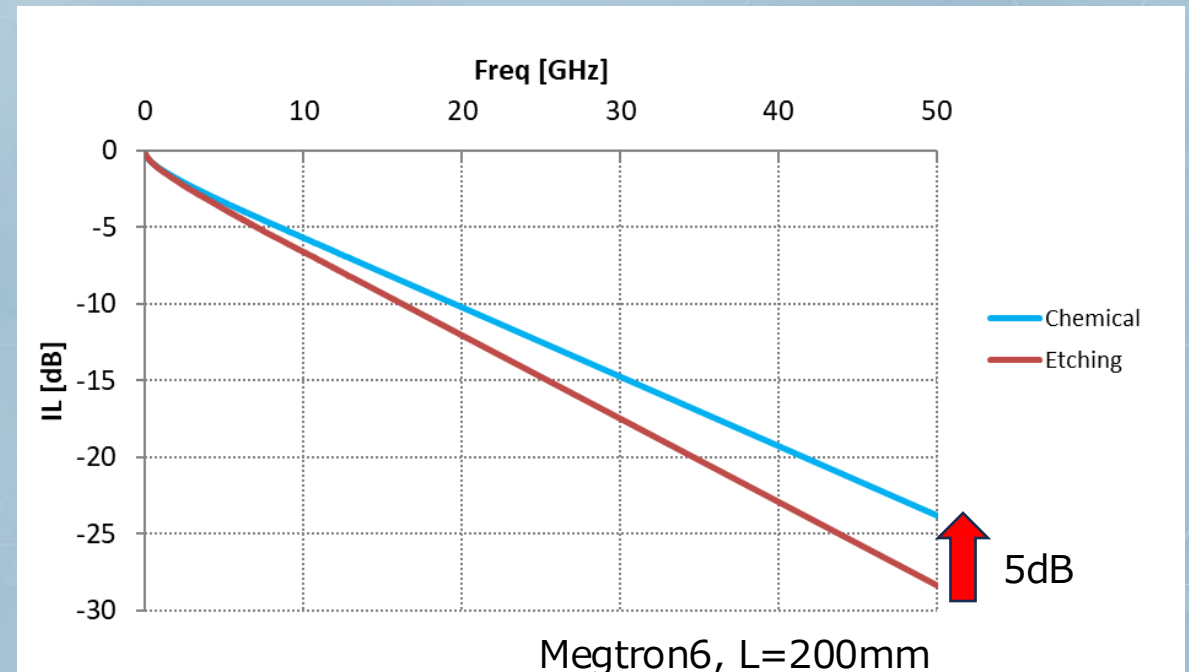
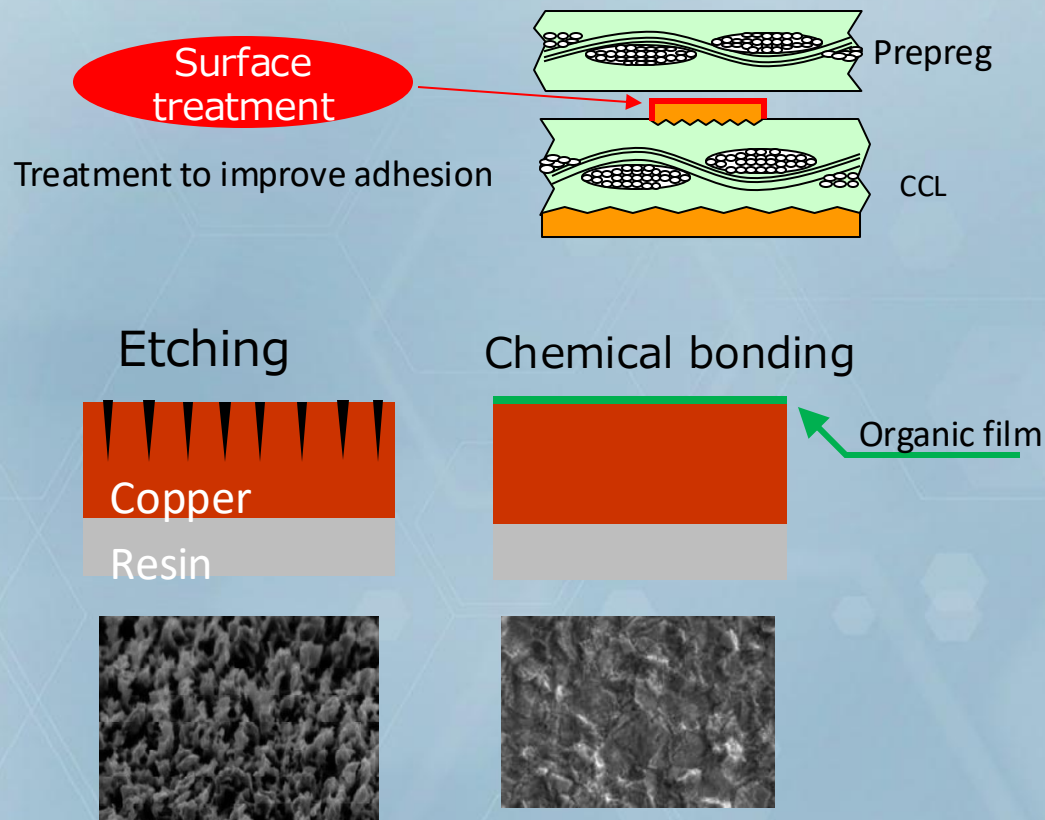
Copper foil

Roughness reduction

⇒ Flat copper foil

High-speed PCB trends

- Approach by manufacturing process -1
High speed PCB require flat surfaces → Chemical bonding



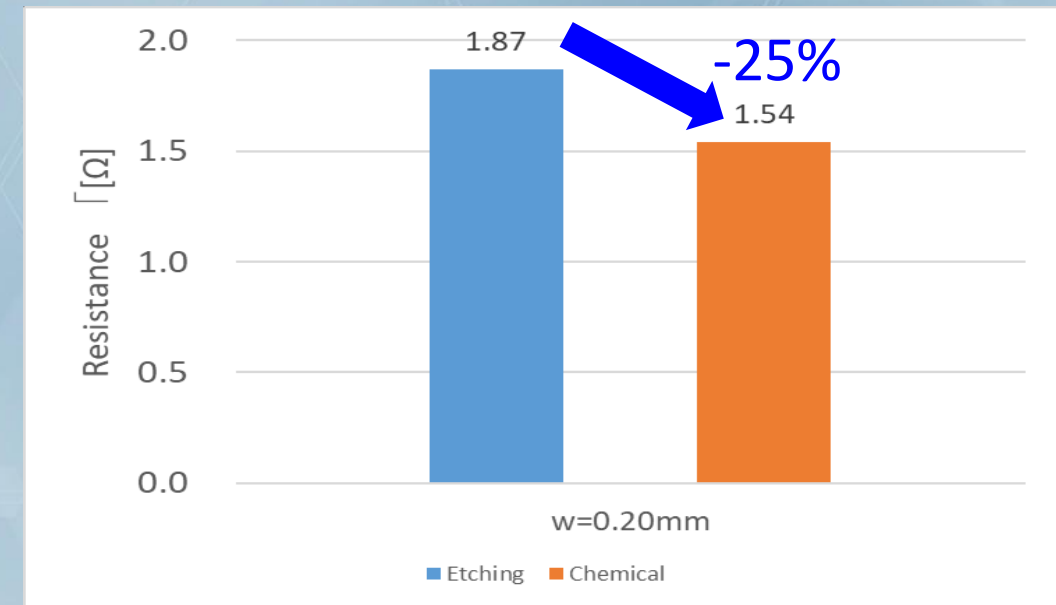
Etching process increases roughness impact due to skin effect

High-speed PCB trends

- Approach by manufacturing process -2
Chemical bonding is also effective in DC resistance
Resistance is reduced by 25%, especially effective for power wiring



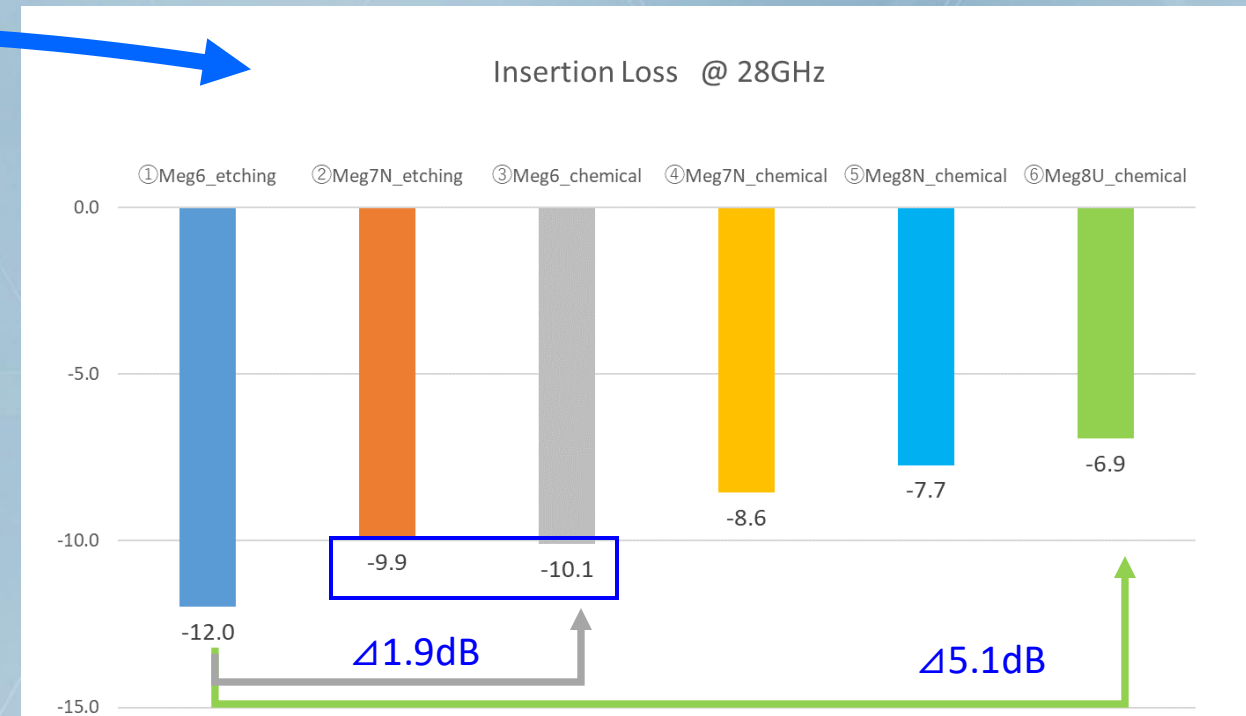
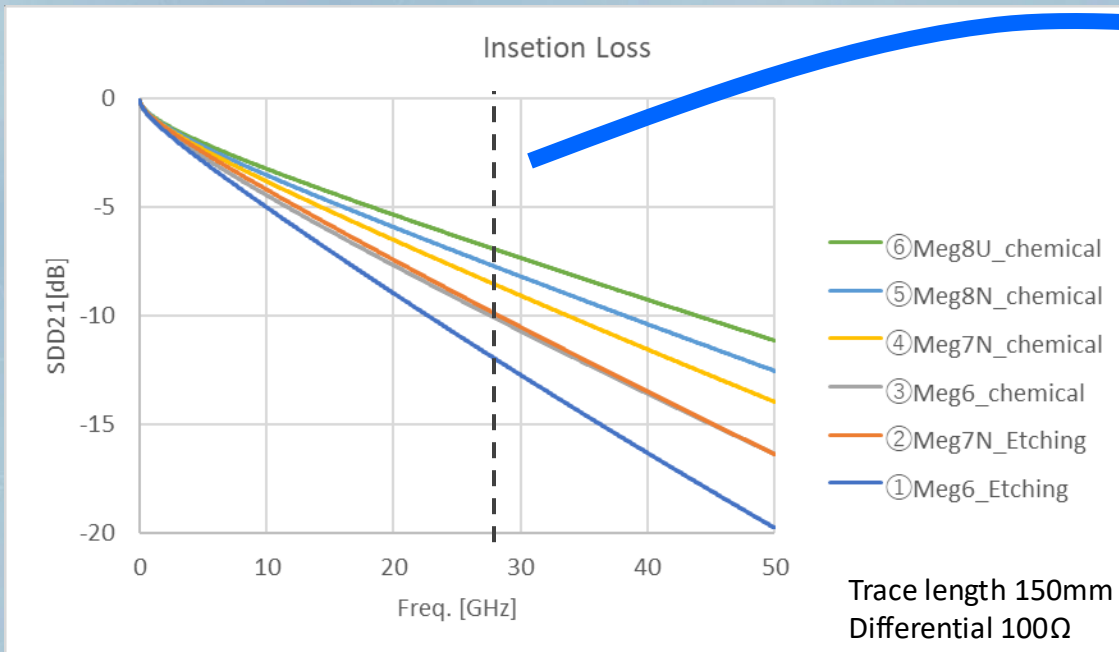
<Probe Card>



0.5oz
L=250mm

High-speed PCB trends

- Effect of material & surface treatment
- ③ improves 1.9dB by the effect of chemical bonding
- ③ and ② are similar → Chemical bond improves loss and cost
- Most Effective is ⑥ : Megtron8U and Chemical bonding: 5.1dB improvement



High-speed PCB trends

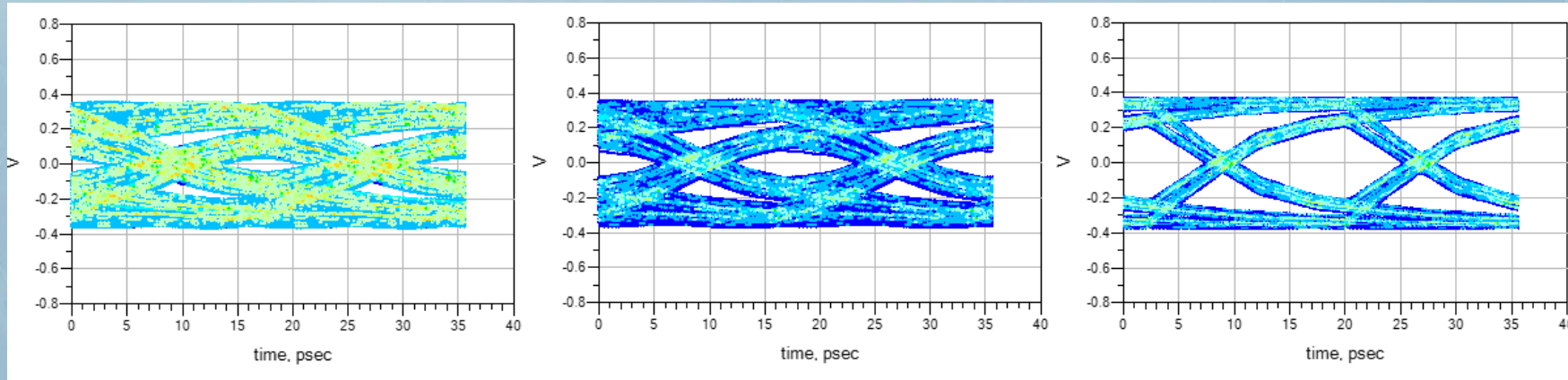
- Eye pattern comparison : ① < ③ < < ⑥
→ High-speed materials and processing show great effects

①Meg6_etching

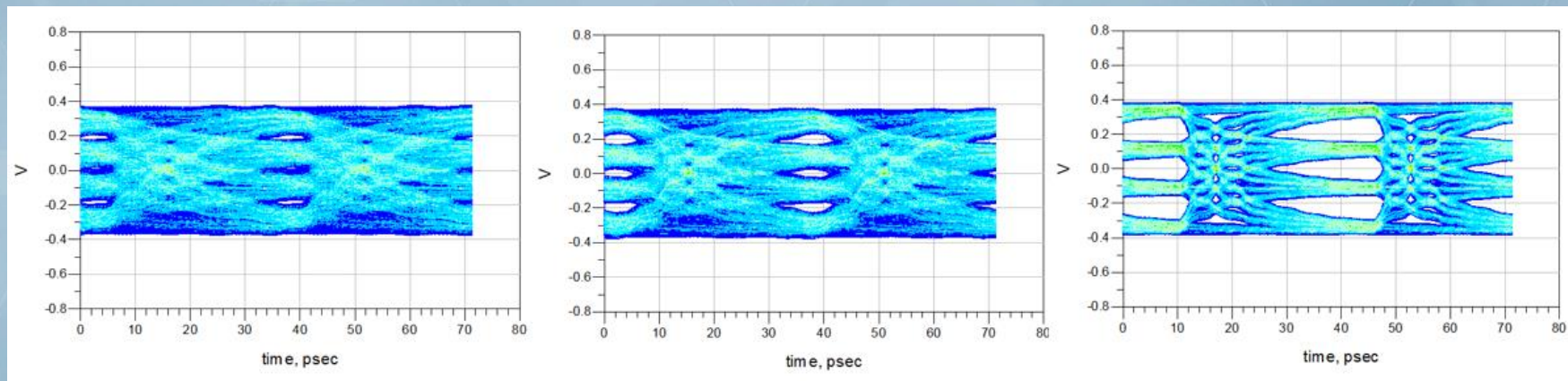
③Meg6_chemical

⑥Meg8U_chemical

56Gbps
(NRZ)

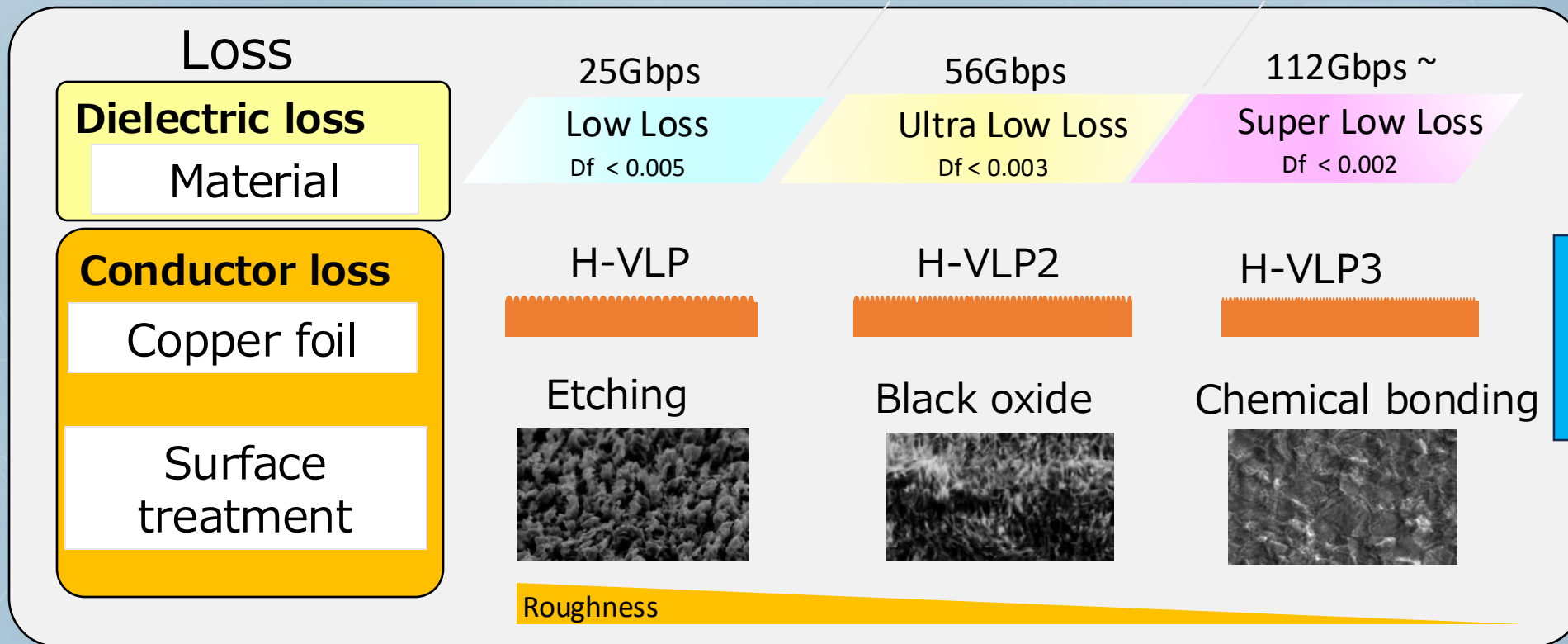


56Gbps
(PAM4)

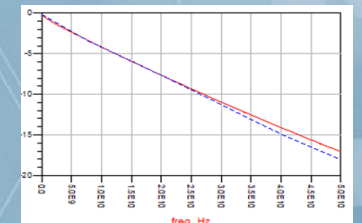
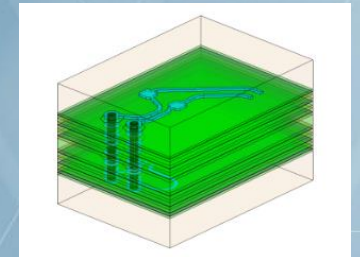


High-speed PCB trends

- Dielectric loss is the dominant factor
 - At High frequency, the effect of conductor loss has increased
 - Realize required characteristic by combinations



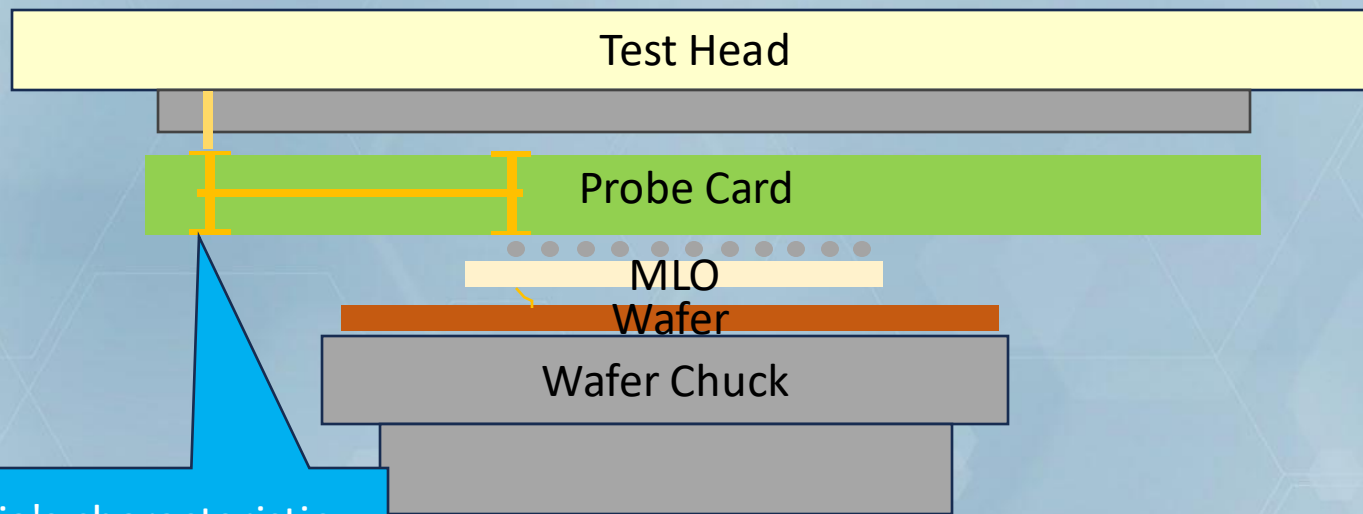
Our own parameters for simulations (Dk, Df, Roughness)



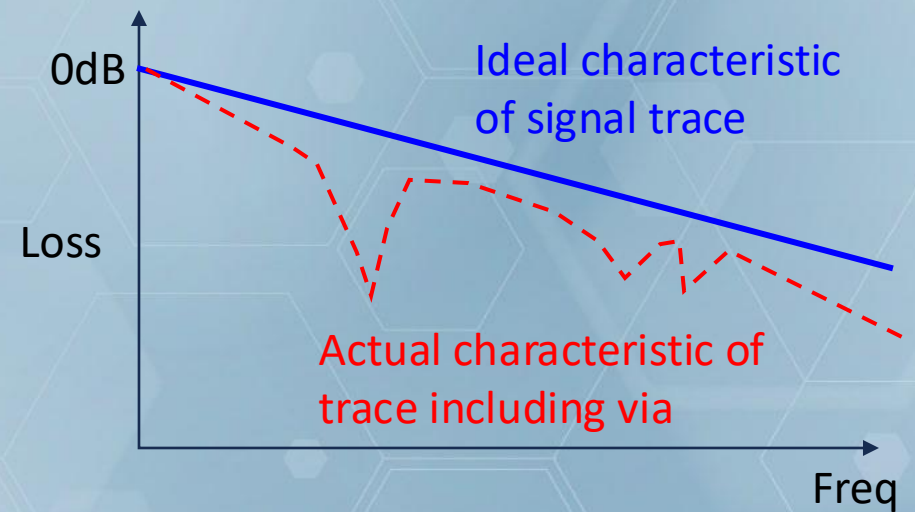
High-speed PCB trends

Structural challenges

- In Probe card, via is necessary for connection from top to bottom
- That via becomes the cause of loss of PCB performance
- Controlling via characteristics at high frequencies is so challenging



Via's characteristic should be "Non-existent" as possible



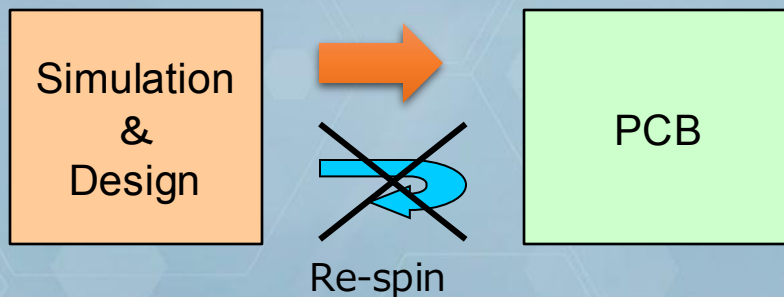
Challenges for High-Speed PCB

■ Goal

- Achieve well-balanced cost and characteristics
- "Via characteristic control" to achieve the targeting characteristics

■ Challenges

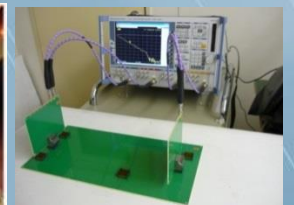
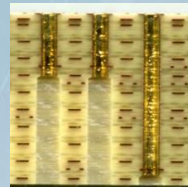
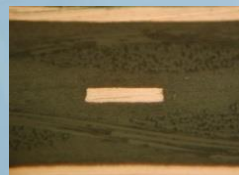
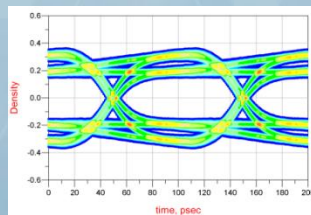
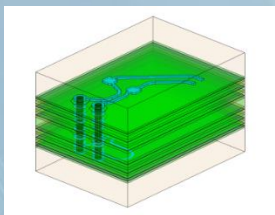
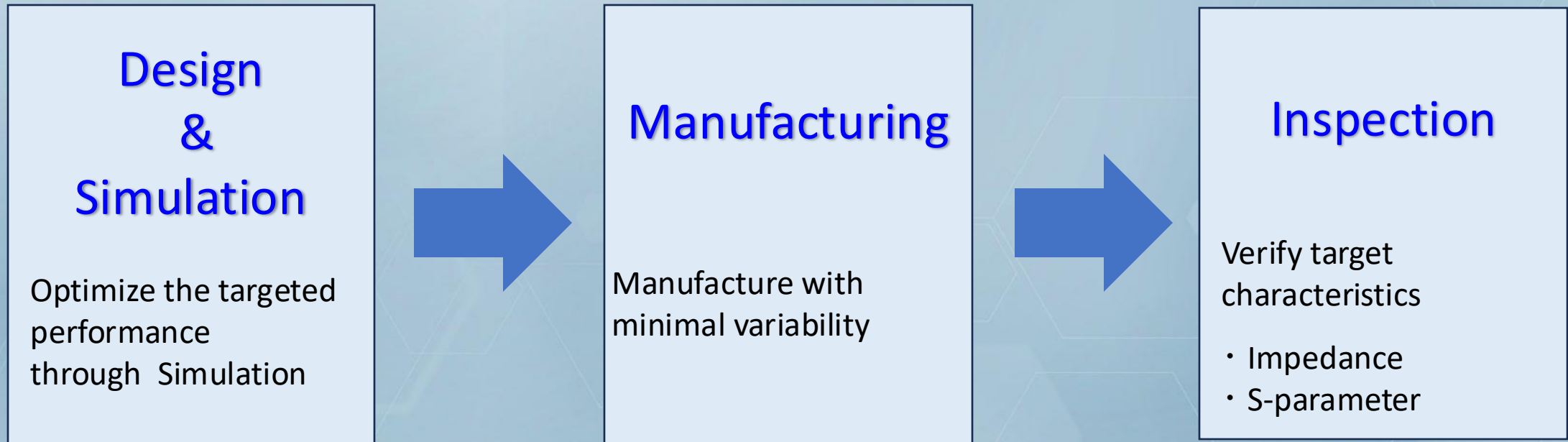
Providing PCBs that meet required characteristics without re-spin
→ Design & Simulation with link to “MONOZUKURI” technology



- Simulation technology that reflecting manufacturability
- Correlation b/w simulation and measurement

Development flow of High-Speed PCB

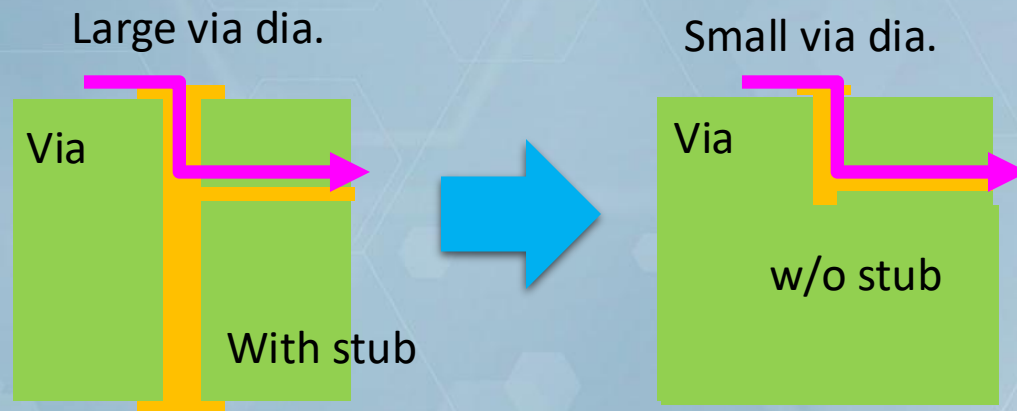
Manage design, manufacturing, and inspection consistently



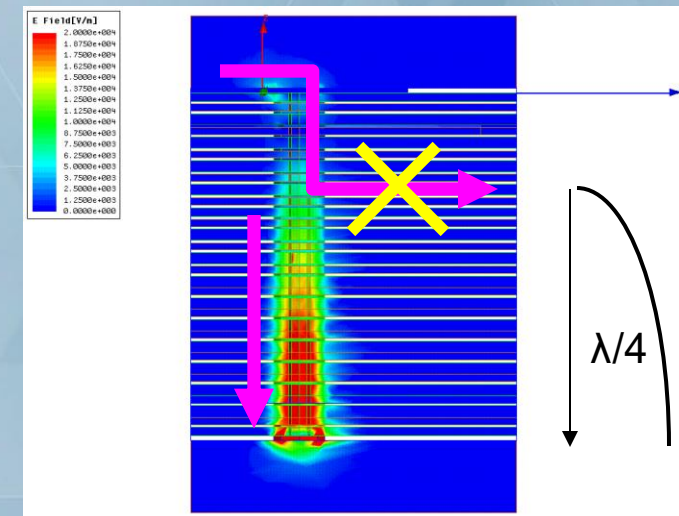
PCB characteristic improvement by design

Improved via's characteristic

- 1) Apply smaller hole and via diameter as possible
⇒ Reduce parasitic capacitance
- 2) Not exist stub
⇒ Not cause resonance



Stub resonance

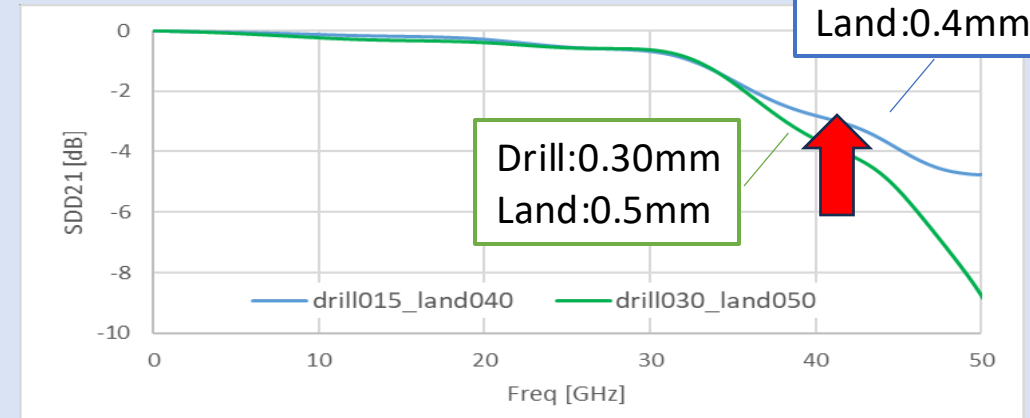


PCB characteristic improvement by design

Effects of dimensional changes

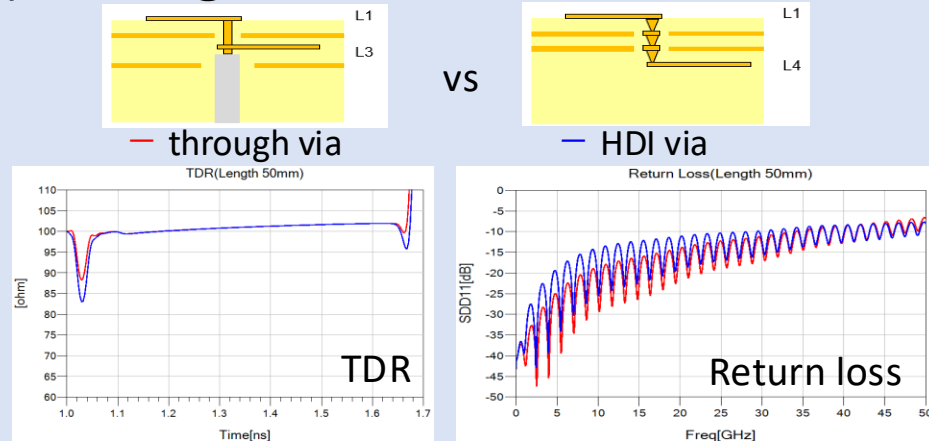
- 1) Hole and land diameters
- 2) Via structure
- 3) Stub length

1) Hole/land diameter



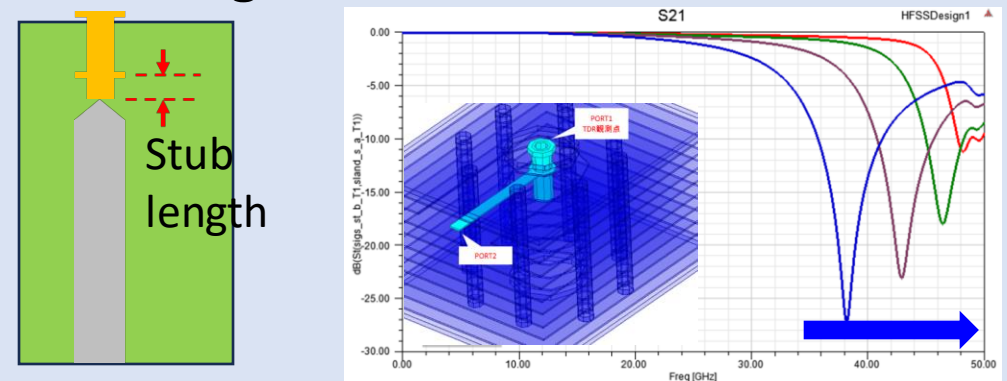
Smaller hole sizes improve insertion loss

2) Through vias vs HDI vias



HDI via lands increases reflection

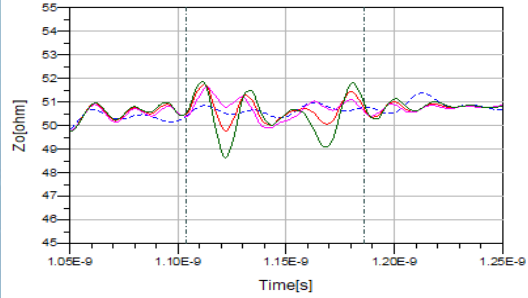
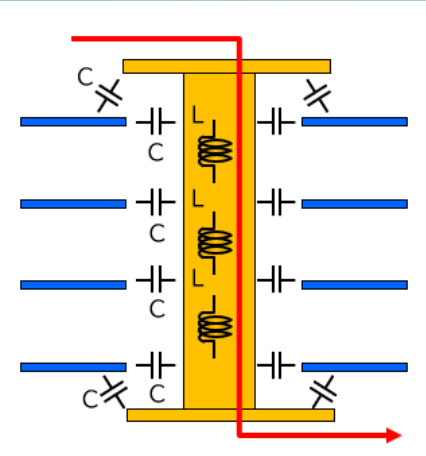
3) Stub length



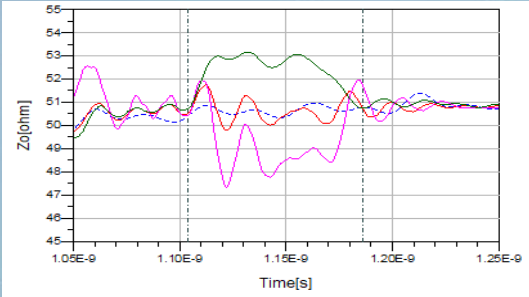
Long stubs cause low-frequency resonance

PCB characteristic improvement by process

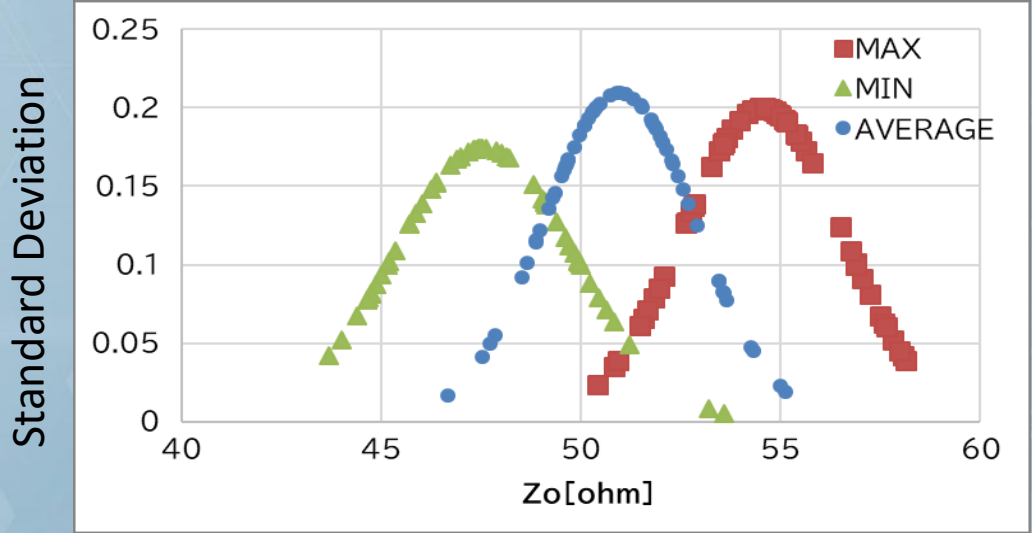
Manufacturing variations impact
So many variable factors in PCB manufacturing
→ which is key factor ?
→ Definition of manufacturing tolerances
The impact of random changes must be considered



Land dia variation



Anti-pad variation

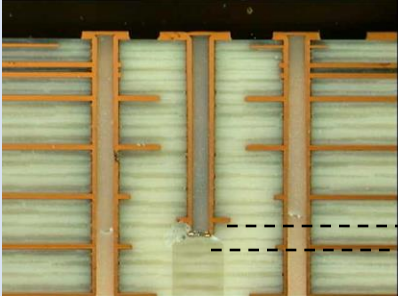


- Variable factors
 - Board thickness
 - Hole Dia
 - Land Dia
 - Anti-pad Dia
 - Hole alignment
 - Layer alignment
 - Dk
 - Stub length

PCB characteristic improvement by process

- Stub accuracy control and inspection
 - High-speed PCB achieve a stub accuracy in 0.15mm or less
 - TDR inspection detects remaining stubs

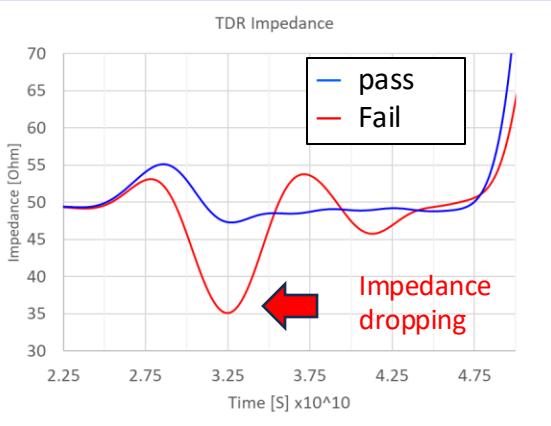
Back Drilling accuracy



Stub length
Available 0.15mm and less

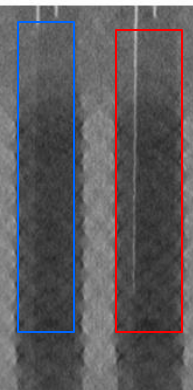
Stub inspection

TDR (Impedance)



| Time [S] x10 ¹⁰ | Impedance [Ohm] (Pass) | Impedance [Ohm] (Fail) |
|----------------------------|------------------------|------------------------|
| 2.25 | 50 | 50 |
| 2.75 | 55 | 53 |
| 3.25 | 48 | 35 |
| 3.75 | 49 | 54 |
| 4.25 | 49 | 47 |
| 4.75 | 70 | 65 |

X-ray image



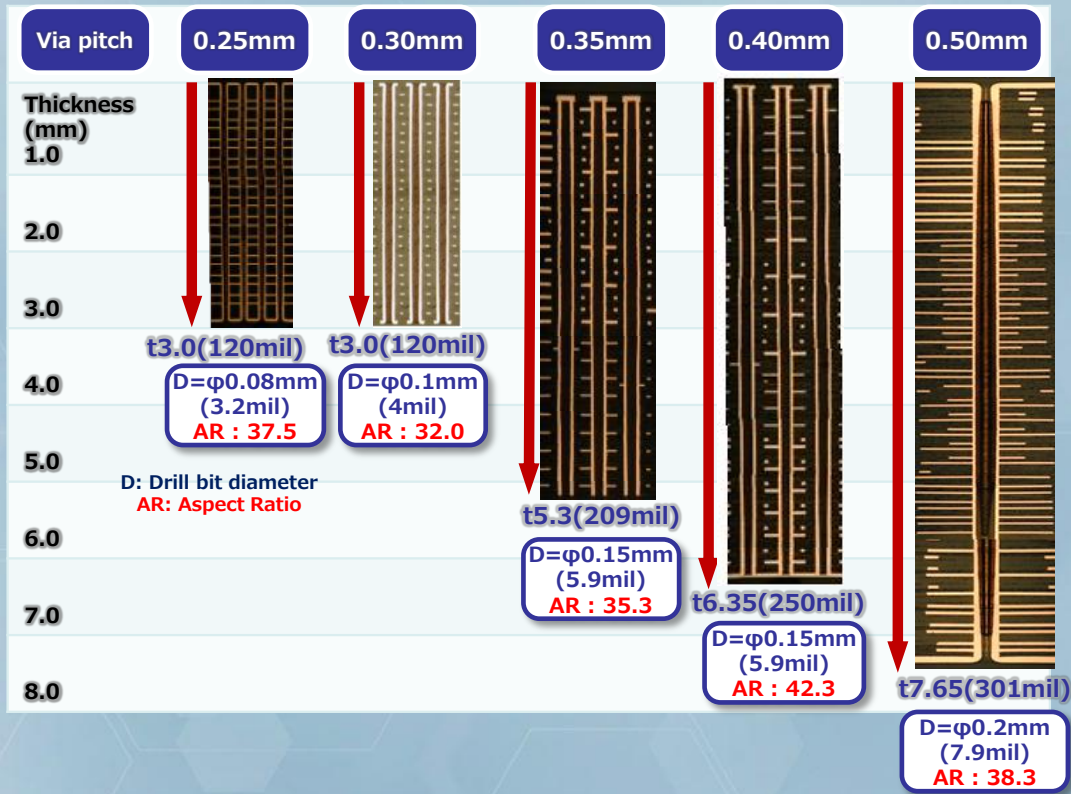
pass Fail

Development examples

- "Fine pitch Through via Technology" reduces crosstalk for 56G-PAM4
 ⇒ Smaller 0.15mm drill is used to reduce coupling in the Z direction

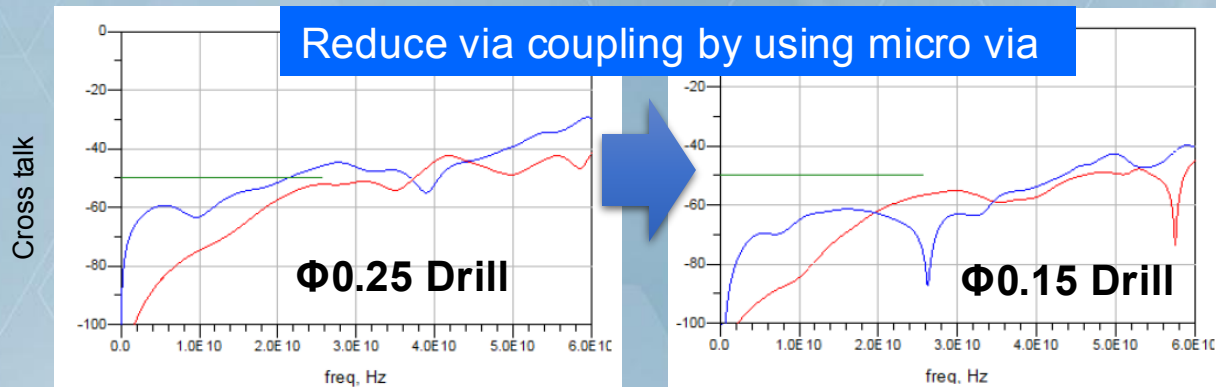
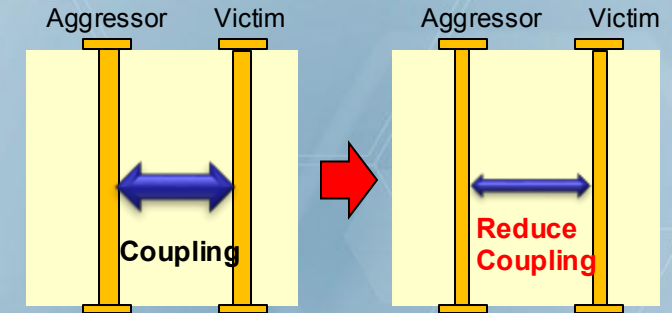
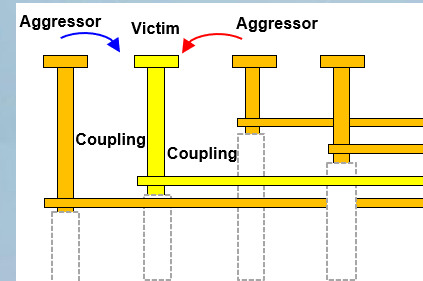
Fine pitch Through via Technology

X-section pictures



PCB thickness : 6.3t
 0.8mm pitch/56G-PAM4
 Crosstalk issues

Drill dia.: φ0.25(9.8mil) → φ0.15(5.9mil)

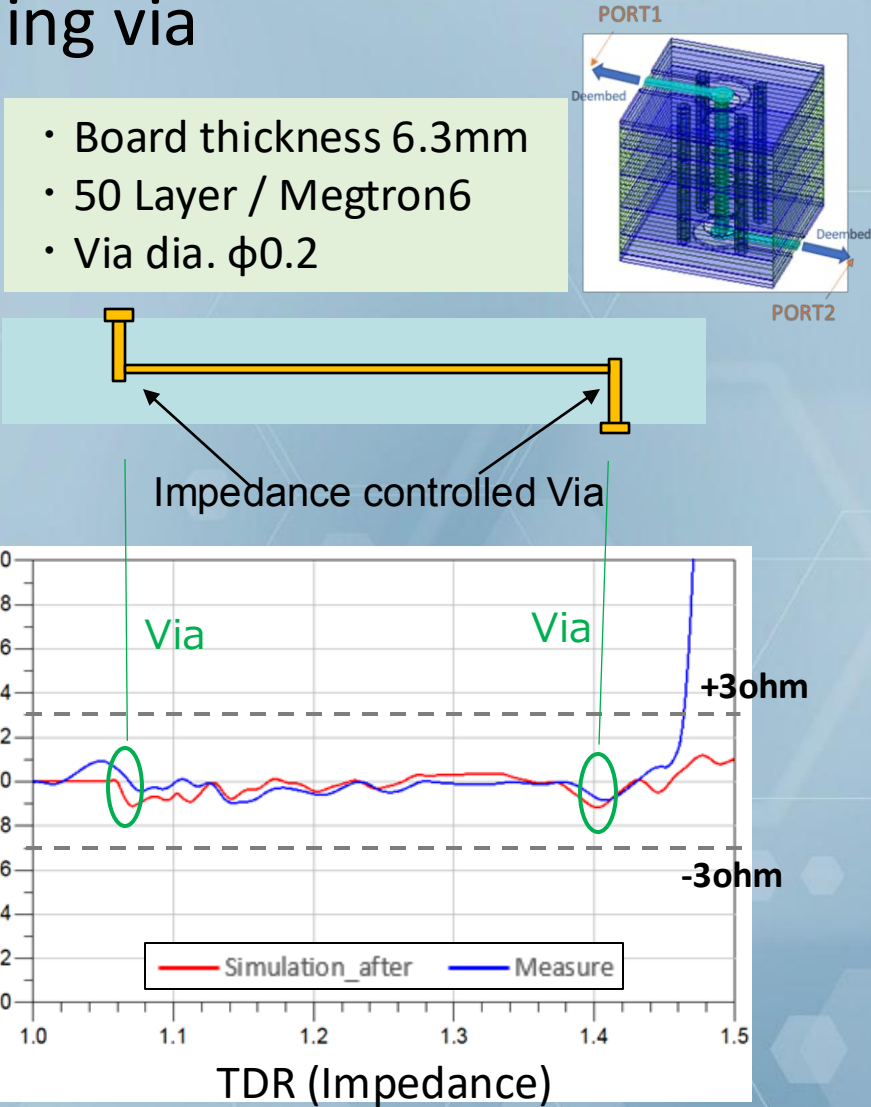
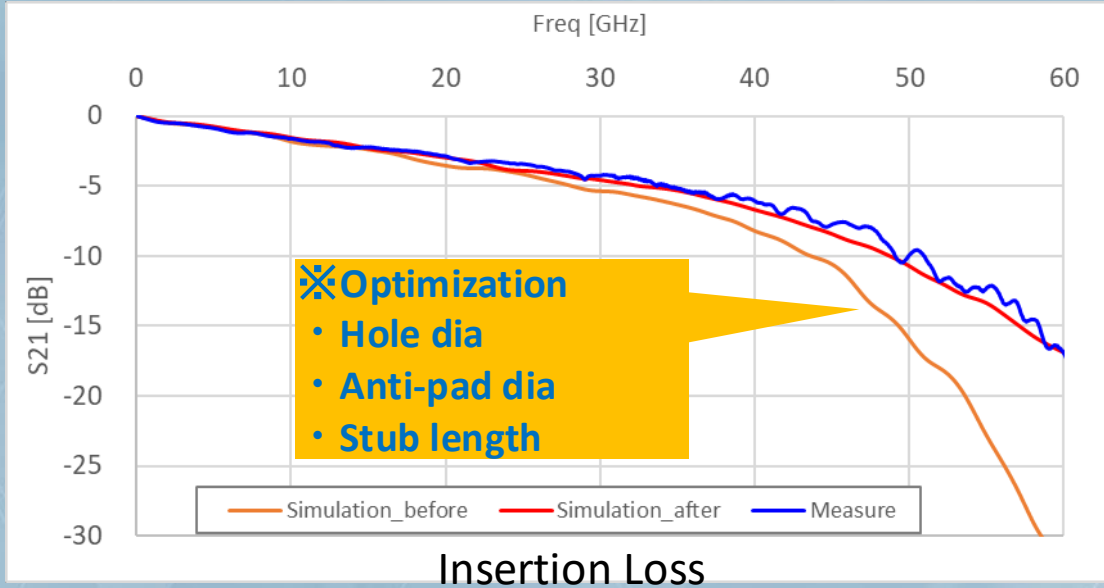


Correlation between measurement and simulation

- Characteristics control of high-speed trace including via

Target spec : Insertion loss : -3dB@20GHz
 Impedance : $50\Omega \pm 3\Omega$ (Tr=25ps)

Good correlation between via TDR (impedance) and Insertion loss up to 60GHz



Conclusion

- **Achieve the development of high-speed PCB efficiently by controlling materials, processes, and design**
- **Via's characteristic control is the effective technology for high-speed transmission**
- **Through the simulation with high correlation up to 50GHz, realize the required characteristic with proper cost**
- **Aim correlation on 100 GHz as next step**



Thank You