SWTEST ASIA
PROBE TODAY, FOR TOMORROW

Space Transformer Organic Technologies for Next-Generation Probe Card Substrates

FICT

Yo Nozaka
FICT LIMITED

5th Annual SWTest Asia | Fukuoka, Japan, October 24 - 25, 2024

Outline

- **Introduction**
  - Background
  - Demand for Probe Card
  - Manufacturing Structure Selection
  - Goals/Challenges
- **Latest Development Status of Space Transformer Organic**
  - TOPIC 1 : Pin Count Increase (Multi-DUTs)
  - TOPIC 2 : Fine Pitch Development
  - Future Challenges
- **Breakthrough Technology : G-ALCS (Multi Layer Glass Substrate)**
  - What is G-ALCS?
  - Characteristics of G-ALCS
  - Our Technology Roadmap
- **Conclusion**

FICT History

1967
FUJITSU LIMITED (PCB Division)

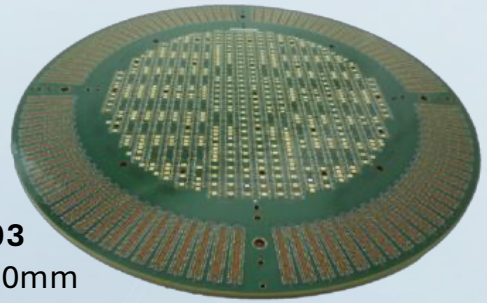
2002
FUJITSU INTERCONNECT TECHNOLOGIES LIMITED

2022
FICT LIMITED

Evolution of FICT Probe Card Substrates

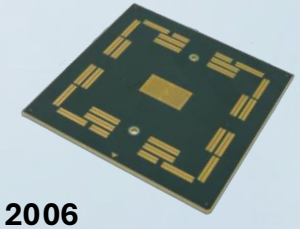
PROBE CARD SUBSTRATE

Probe Card PCB

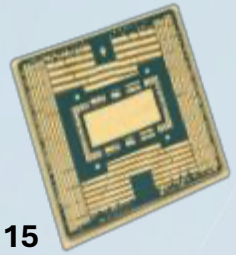


Since 2003
Size : ϕ520mm
Layers: 108L

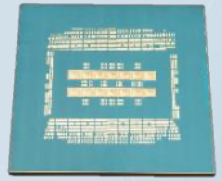
Space Transformer Organic
(Multi Layer Organic)



2006
Size : □60-□80 mm
Build-up : max 6-2-6

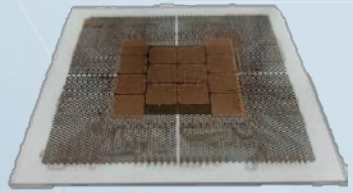


2015
Size : □100mm
Build-up : max 7-24-7



2024
Size **: □100-□150 mm**
Build-up : **max 20-18-20**

Inorganic ST
(Multi Layer Glass)



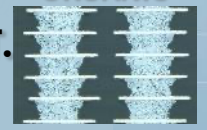
Under Development

OUR TECHNOLOGIES

1990
FLIP CHIP TECHNOLOGY ON CERAMIC

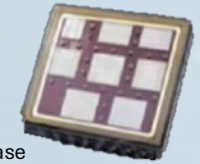
2001
FLIP CHIP TECHNOLOGY ON ORGANIC SUBSTRATE

2011
ANY LAYER VIA STRUCT. F-ALCS TECHNOLOGY

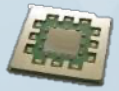


2017
ANY LAYER VIA STRUCT. G-ALCS TECHNOLOGY

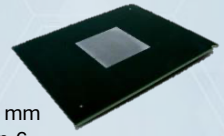
PKG SUBSTRATE



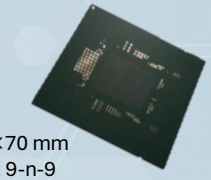
1993
CERAMIC base
Multi Chip Module



2003
ORGANIC base
FC-BGA substrate



2014
Size : 72×60 mm
Build-up : 6-n-6



2022
Size : 87×70 mm
Build-up : 9-n-9

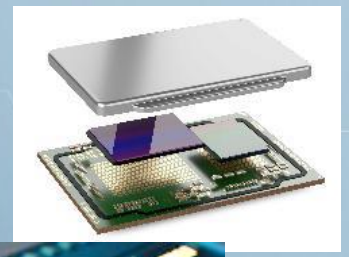
Under Development

1990 1995 2000 2005 2010 2015 2020 2025 FUTURE

Demand for Probe Card

Pin Count Increase (Multi-DUTs)

for Test efficiency



Fine Pitch

for Chiplet,

2.xD/3D assembly

Demand

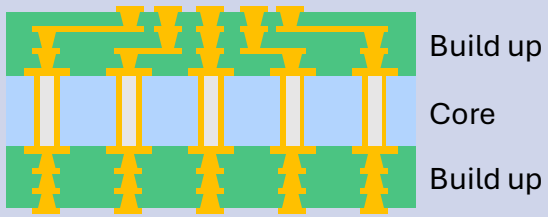
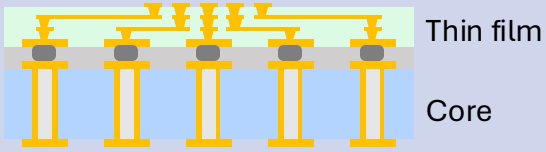
High Power

- Power control, High current

High Speed

- 5G/6G, Big data transmission

Manufacturing Structure Selection

Specifications	Build up		Thin film	
High density	Good	Core + Build up 	Excellent	Core + Thin film 
Layer #	Good		Poor	
Electrical properties (SI, PI)	Good		Poor	
Power delivery structure	Good		Poor	
Productivity	Good		Poor	
Cost (NRE, Material, Yield)	Good		Poor	
Lead time	Fair		Fair	
Comments	Generally superior properties (No critical disadvantages)		Superior on high density routing	

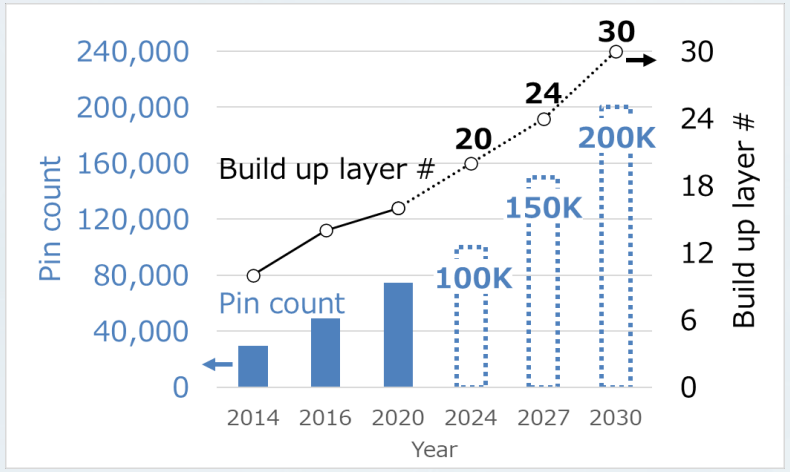
Build up structure can be applied to a wide range of existing products.
By unleashing its potential, we aim to offer higher-performance products.

Goals/Challenges

TOPIC 1
Pin Count Increase (Multi-DUTs)

Goal : 100K pins by 2024
200K pins by 2030

Pin count evolution estimation



Source: FICT LIMITED

Challenge :

Increasing build up layers up to 20 and more

TOPIC 2
Fine Pitch Development

Goal : 45μm pitch by 2024
30μm pitch by 2026

Min. Bump pitch scale roadmap for chiplet interposer

(unit : μm)

Material	2019	2022	2025	2028	2031
Organic interposer	50	45	40	40	30
Silicon interposer	40	35	30	20	20

Source: Heterogeneous Integration Roadmap. IEEE

Challenges :

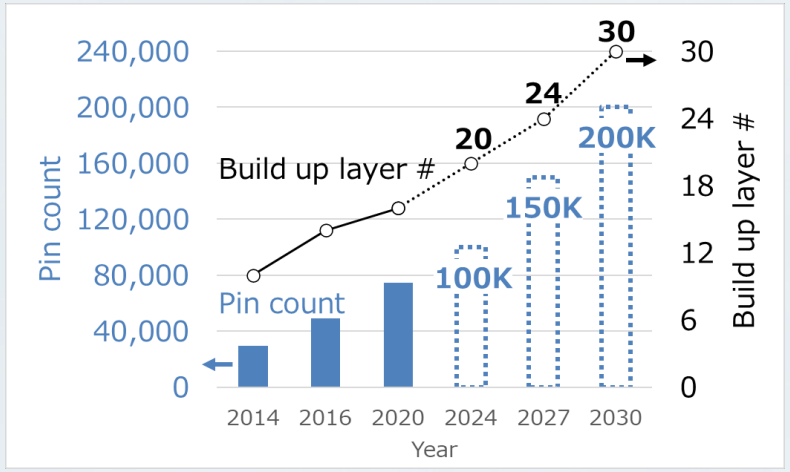
1. Fine via pitch by using thin build up structure
2. Pad position control by lowering substrate CTE

Goals/Challenges

TOPIC 1
Pin Count Increase (Multi-DUTs)

Goal : 100K pins by 2024
200K pins by 2030

Pin count evolution estimation



Source: FICT LIMITED

Challenge :

Increasing build up layers up to 20 and more

TOPIC 2
Fine Pitch Development

Goal : 45μm pitch by 2024
30μm pitch by 2026

Min. Bump pitch scale roadmap for chiplet interposer

(unit : μm)

Material	2019	2022	2025	2028	2031
Organic interposer	50	45	40	40	30
Silicon interposer	40	35	30	20	20

Source: Heterogeneous Integration Roadmap. IEEE

Challenges :

1. Fine via pitch by using thin build up structure
2. Pad position control by lowering substrate CTE

Approach to Keep up with Pin Count Increasing Trend

Pin count increasing

I/O nets increasing

Routing area increasing

High build up layers

Large size
⚠ ASSEMBLY PROCESS

Fine L/S
⚠ SI PERFORMANCE

Essential technologies to increase build up layers

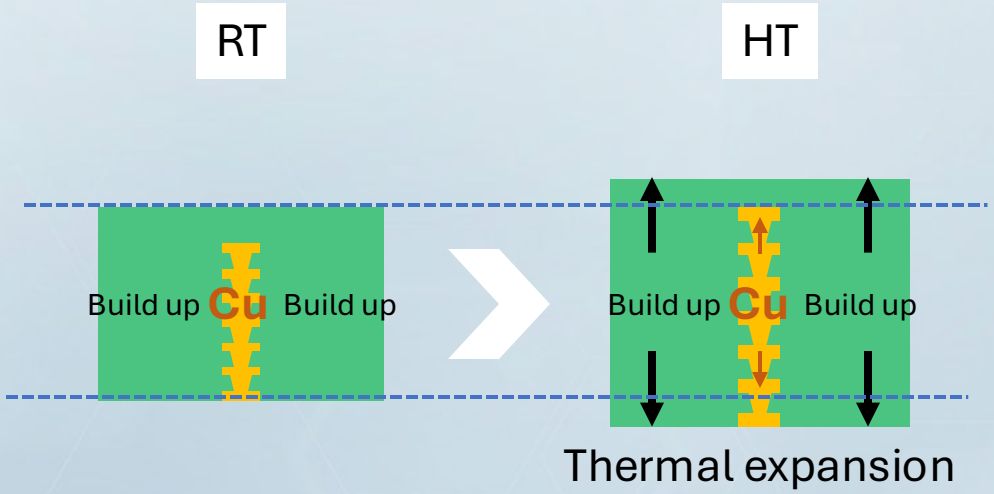
Technology 1	Technology 2	Technology 3	Technology 4
Laser via stress reduction by small CTE mismatch	Laser via shape imp. by process tuning (Laser via drilling, Desmear)	Flat dielectric/Cu plating surface	Layer to layer position accuracy improvement

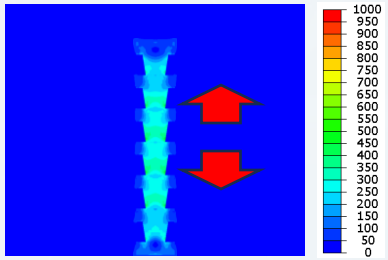
Main focus in this presentation

Thermal stress due to CTE mismatch

Mechanism 1

(Build up 39ppm/Cu 16.5ppm)

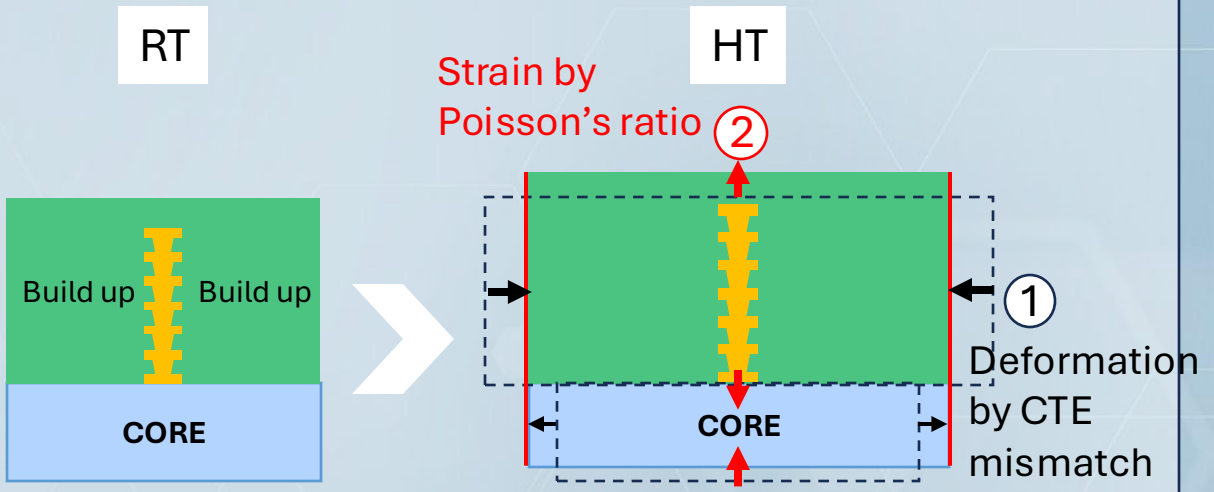


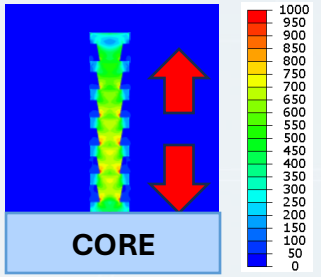


Stress due to thermal expansion mismatch

Mechanism 2

(Build up 39ppm/**CORE** 14ppm)





Stress caused by combination with Mech. 1

Test Vehicle Specification (Increasing Build up Layers)

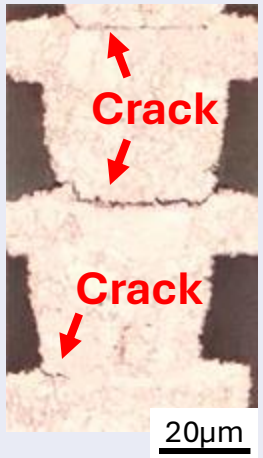
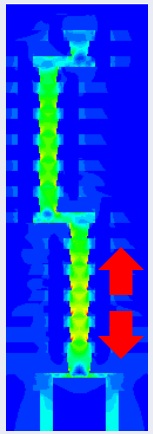
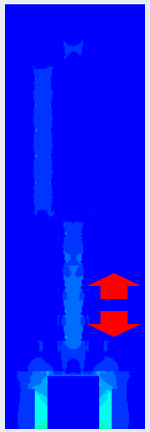
Specifications		Conventional		(New) Low CTE material	
Substrate size		100mm*100mm*3mmt		100mm*100mm*3mmt	
Layers		20-8-20		20-8-20	
CTE [ppm]	Core	14	-57%	**6**	⊿14
	Build up film	39	-49%	**20**	
	Copper	16.5		16.5	⊿3.5
Modulus [GPa]	Core	26.5	+28%	**34**	
	Build up film	5	+160%	**13**	
	Copper	130		130	
Build up film thickness		30μm		30μm	
Laser via diameter		40μm		40μm	
DUT pad diameter		60μm		60μm	
DUT pitch		80μm		80μm	

⊿25 (Core, Build up film)

⊿22.5 (Build up film, Copper)

Results (Thermal Cycle Test)

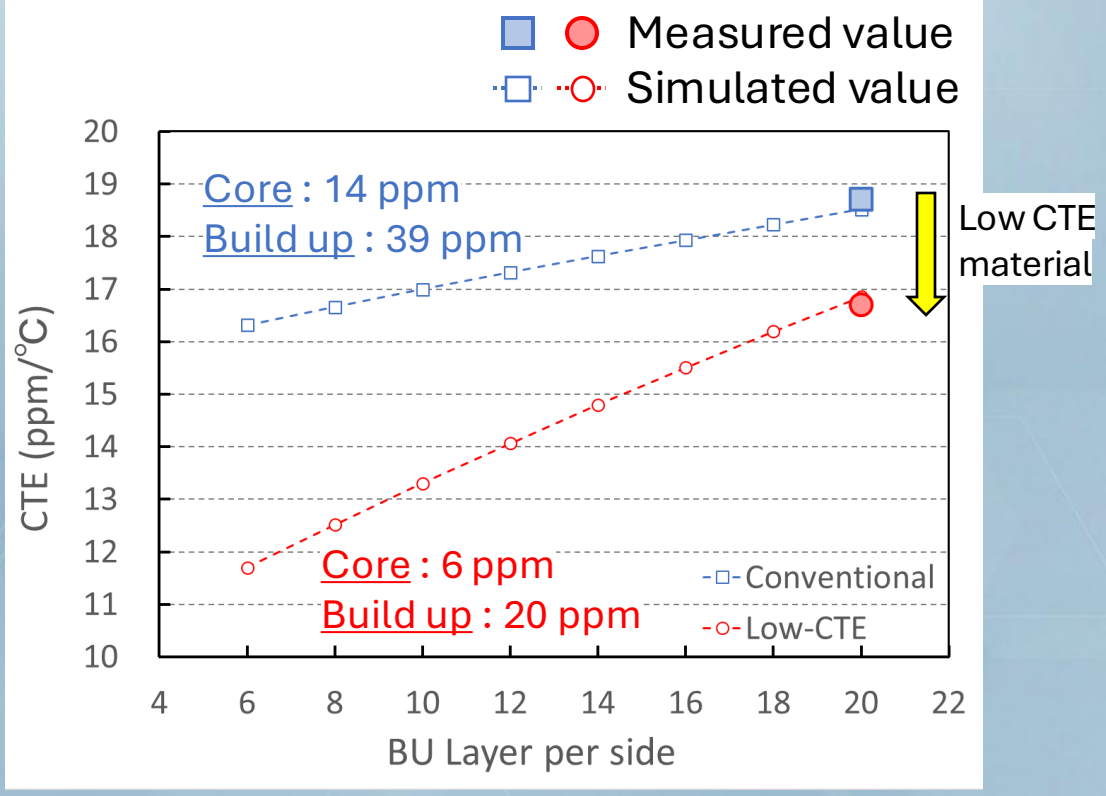
Test condition : Reflow 235deg.C x 6times + TC 50, 100, 200, 300cycles

	Conventional				(New) Low CTE material			
Thermal cycle	**50cyc**	**100cyc**	**200cyc**	**300cyc**	**50cyc**	**100cyc**	**200cyc**	**300cyc**
Result	PASS	PASS	FAIL	FAIL	PASS	PASS	PASS	PASS
Cross section after TC 300cyc Laser via dia. : ϕ40		 Higher stress				 Lower stress by limiting CTE mismatch		

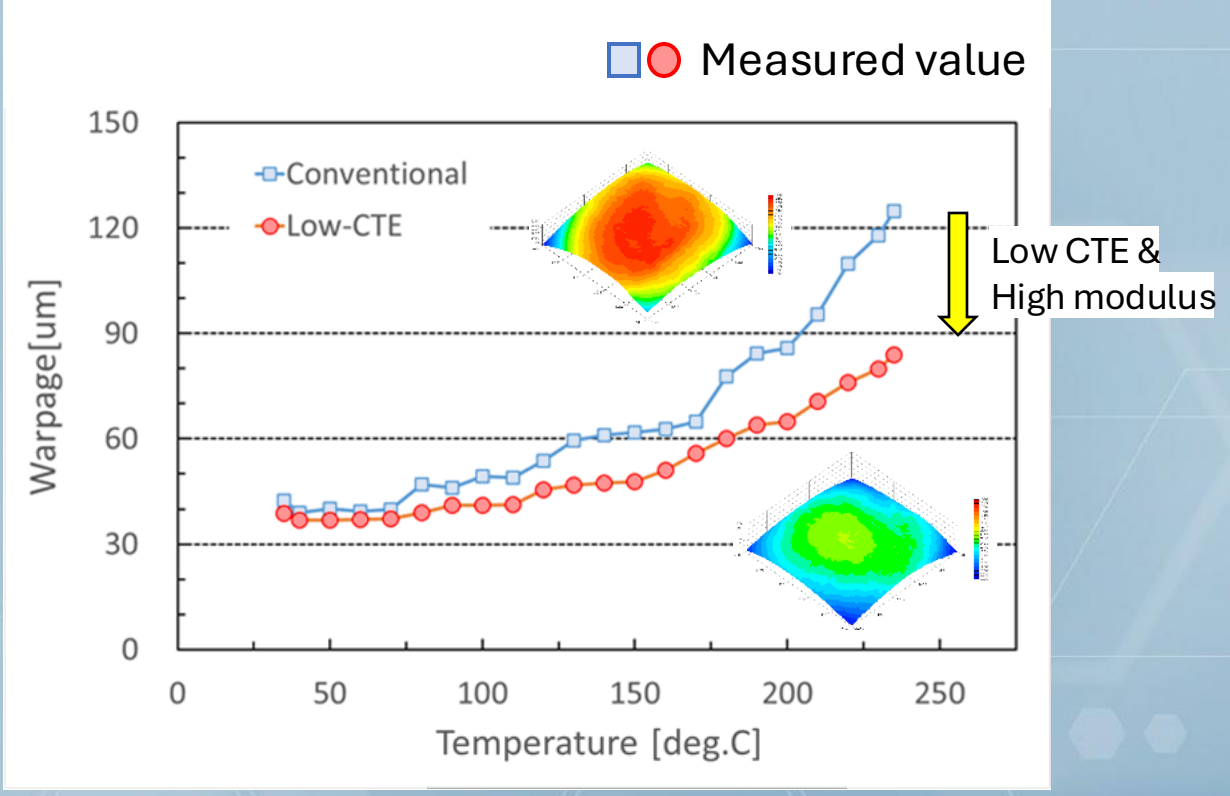
Reliability was improved by controlling CTE mismatch among Cu/Build up/Core.
100K pins structure with 20 build up layers is in mass production.

Results (CTE and Warpage)

CTE measurement and simulation



Warpage measurement



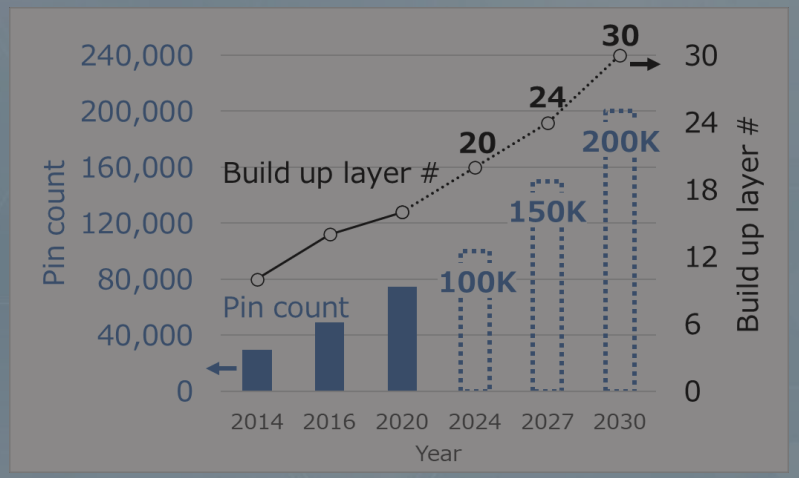
CTE and warpage was improved by applying low CTE material set.

Goals/Challenges

TOPIC 1
Pin Count Increase (Multi-DUTs)

Goal : 100K pins by 2024
200K pins by 2030

Pin count evolution estimation



Source: FICT LIMITED

Challenge :
Increasing build up layers up to 20 and more

TOPIC 2
Fine Pitch Development

Goal : 45μm pitch by 2024
30μm pitch by 2026

Min. Bump pitch scale roadmap for chiplet interposer

(unit : μm)

Material	2019	2022	2025	2028	2031
Organic interposer	50	45	40	40	30
Silicon interposer	40	35	30	20	20

Source: Heterogeneous Integration Roadmap. IEEE

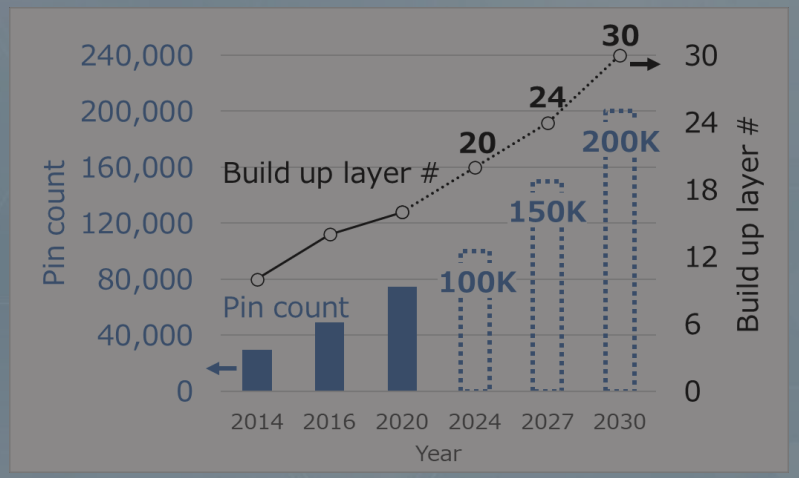
Challenges :
1. Fine via pitch by using thin build up structure
2. Pad position control by lowering substrate CTE

Goals/Challenges

TOPIC 1
Pin Count Increase (Multi-DUTs)

Goal : 100K pins by 2024
200K pins by 2030

Pin count evolution estimation



Source: FICT LIMITED

Challenge :
Increasing build up layers up to 20 and more

TOPIC 2
Fine Pitch Development

Goal : 45µm pitch by 2024
30µm pitch by 2026

Min. Bump pitch scale roadmap for chiplet interposer

(unit : µm)

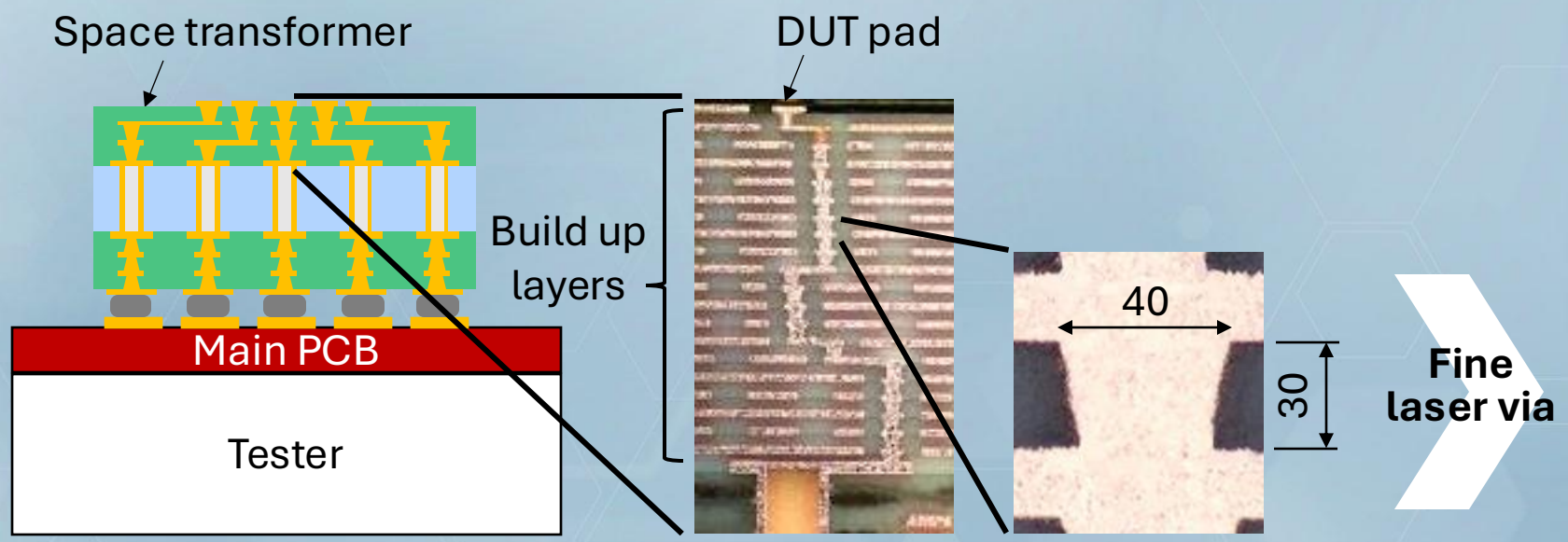
Material	2019	2022	2025	2028	2031
Organic interposer	50	45	40	40	30
Silicon interposer	40	35	30	20	20

Source: Heterogeneous Integration Roadmap. IEEE

Challenges :
1. **Fine via pitch by using thin build up structure**
2. Pad position control by lowering substrate CTE

Challenge 1 : Fine Via Pitch by Using Thin Build up Structure

- **Concept of fine pitch development**

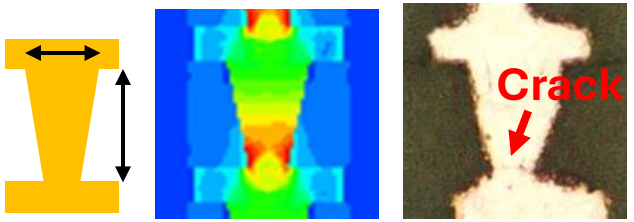


Fine laser via

Bad shape

High aspect ratio

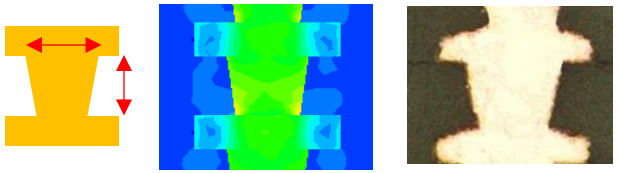
(**Fine** laser via / **Thick** build up)



Good shape

Low aspect ratio

(**Fine** laser via / **Thin** build up)



For fine pitch laser, control of aspect ratio (laser via/build up thickness) is important.

Test Vehicle Specification (Challenge 1 : Fine Via Pitch)

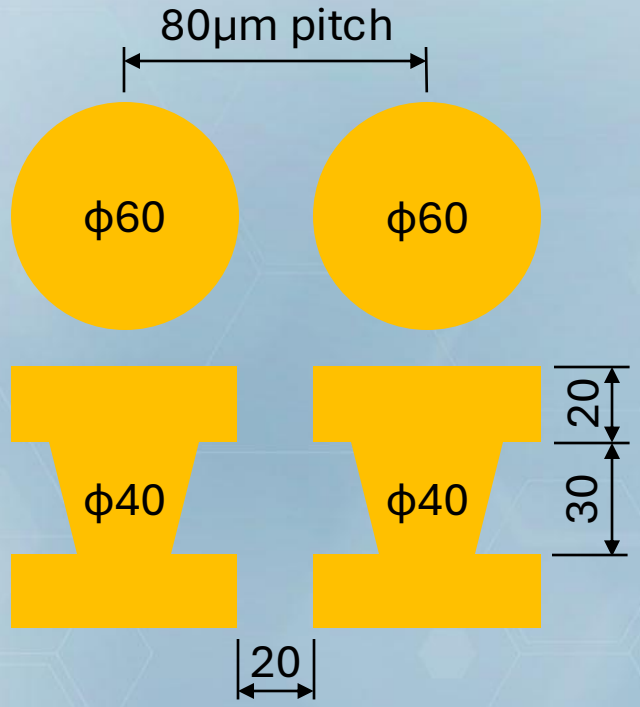
Specifications		Conventional build up & Low CTE material	(New) Thin build up & Low CTE material
Substrate size		72mm*72mm*3mmt	72mm*72mm*3mmt
Layers		16-8-16	16-8-16
CTE [ppm]	Core	6	6
	Build up film	20	20
	Copper	16.5	16.5
Modulus [GPa]	Core	34	34
	Build up film	13	13
	Copper	130	130
Build up film thickness		30µm	**15µm**
Laser via diameter		40µm	**20µm**
DUT pad diameter		60µm	**30µm**
DUT pitch		80µm	**45µm**

-50%

-44%

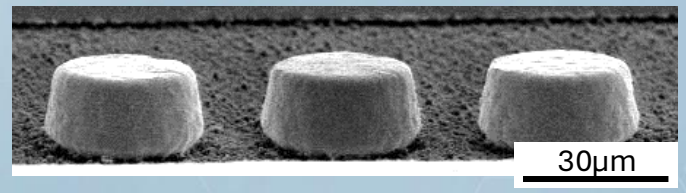
Results (Challenge 1 : Fine Via Pitch)

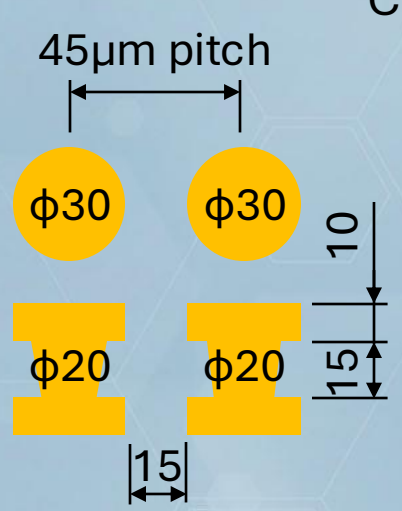
80μm pitch (Conventional)



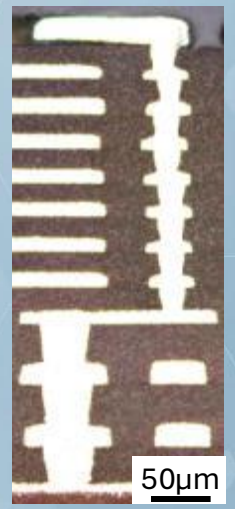
Cross section

45μm pitch (New)



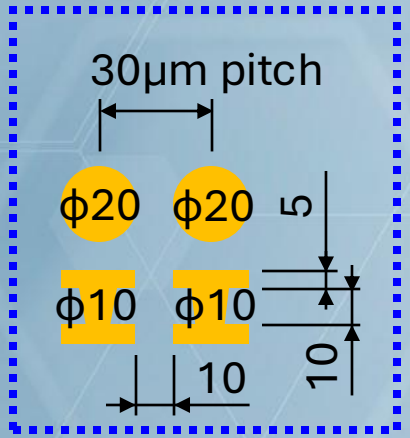


Cross section



30μm pitch

Under development



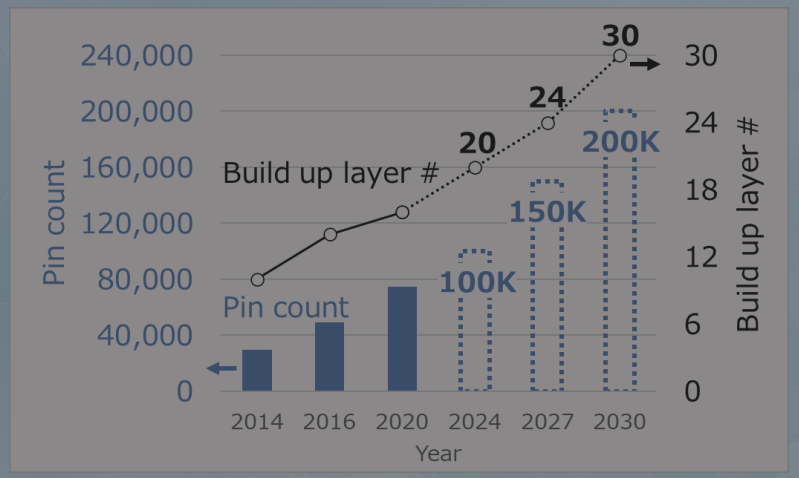
45μm pitch with ϕ20μm laser via was developed by using thin build up structure.

Goals/Challenges

TOPIC 1
Pin Count Increase (Multi-DUTs)

Goal : 100K pins by 2024
200K pins by 2030

Pin count evolution estimation



Source: FICT LIMITED

Challenge :
Increasing build up layers up to 20 and more

TOPIC 2
Fine Pitch Development

Goal : 45µm pitch by 2024
30µm pitch by 2026

Min. Bump pitch scale roadmap for chiplet interposer

(unit : µm)

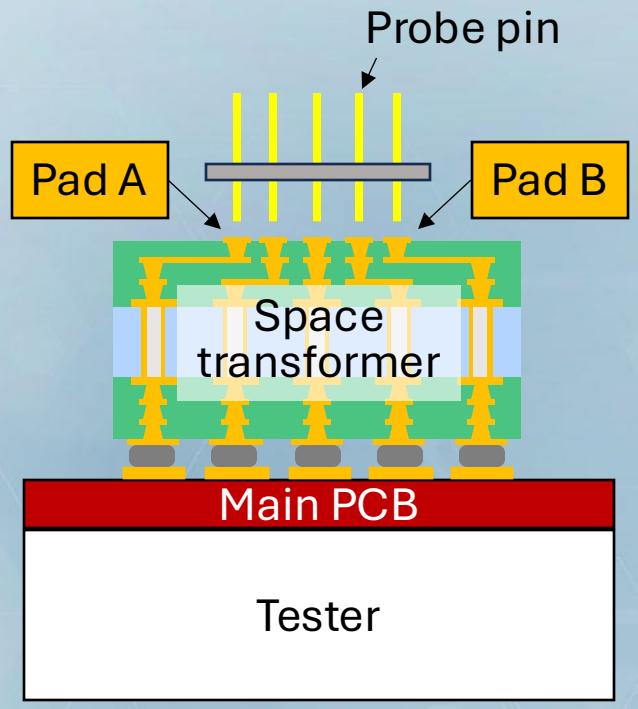
Material	2019	2022	2025	2028	2031
Organic interposer	50	45	40	40	30
Silicon interposer	40	35	30	20	20

Source: Heterogeneous Integration Roadmap. IEEE

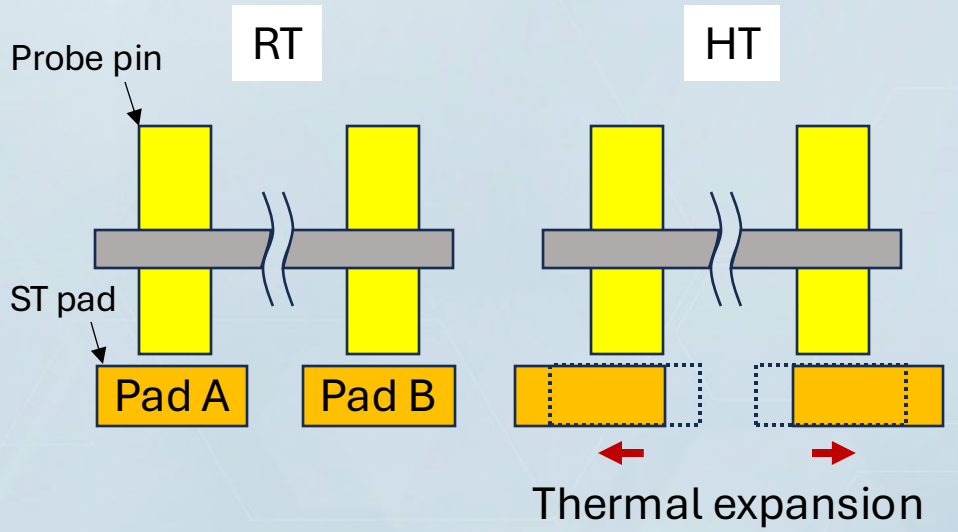
Challenges :
1. Fine via pitch by using thin build up structure
2. **Pad position control by lowering substrate CTE**

Challenge 2 : Pad Position Control by Lowering Substrate CTE

- **Pad position shift by thermal expansion**

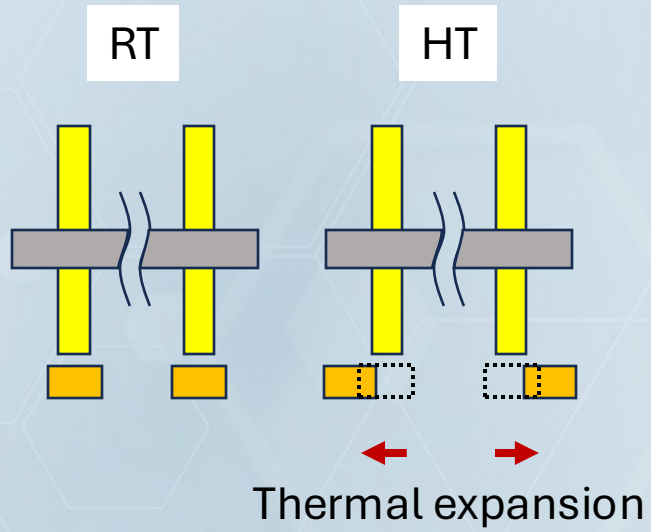


Large pitch with large pads



Relatively small impact

Fine pitch with small pads

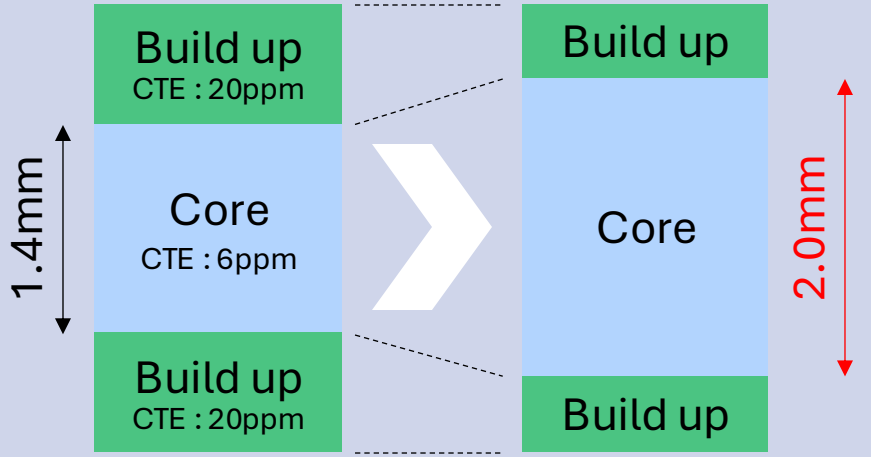
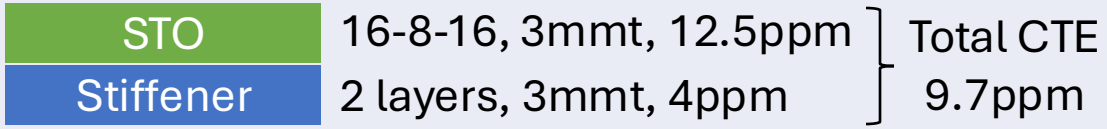


Larger impact on pin alignment

Influence of thermal expansion becomes larger as DUT pads become smaller. CTE has to be lowered at the same time as fine pitch development.

Challenge 2 : Pad Position Control by Lowering Substrate CTE

- **Methods for lowering substrate CTE**

	Methods	Status
1	Core thickness increase by applying thin build up structure Main focus in this presentation	Available 
2	Low CTE organic stiffener	Available 
3	Further low CTE material	Under development
4	Scaling control by estimating thermal expansion	Available

Test Vehicle Specification (Challenge 2 : Pad Position Control)

Specifications		Conventional build up & Low CTE material	(New) Thin build up & Low CTE material
Substrate size		72mm*72mm*3mmt (Core : 1.4mmt)	72mm*72mm*3mmt **(Core : 2.0mmt)**
Layers		16-8-16	16-8-16
CTE [ppm]	Core	6	6
	Build up film	20	20
	Copper	16.5	16.5
Modulus [GPa]	Core	34	34
	Build up film	13	13
	Copper	130	130
Build up film thickness		30µm	**15µm**
Laser via diameter		40µm	**20µm**
DUT pad diameter		60µm	**30µm**
DUT pitch		80µm	**45µm**

+43%

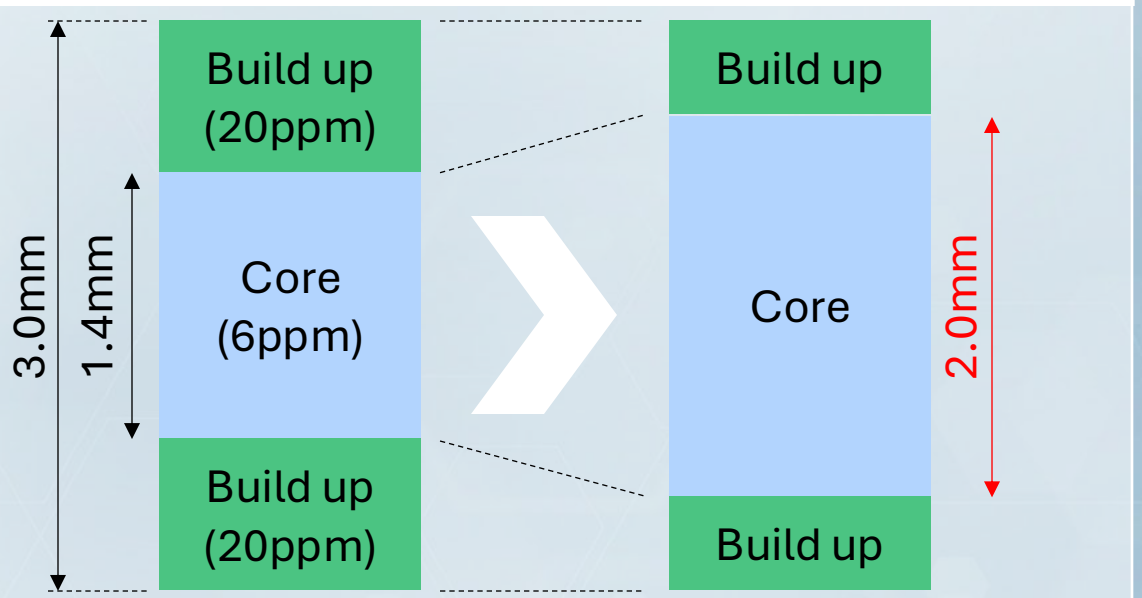
-50%

-44%

Results (Challenge 2 : Pad Position Control)

Substrate structure and CTE

Conventional build up & Low CTE material	(New) Thin build up & Low CTE material

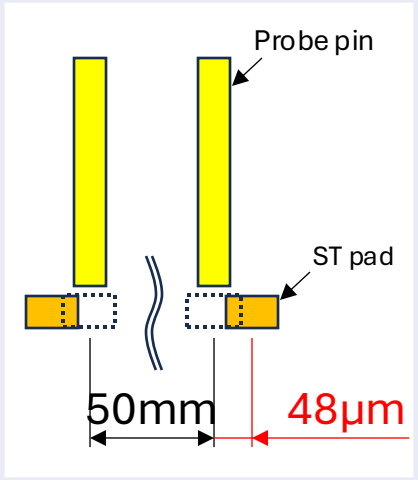


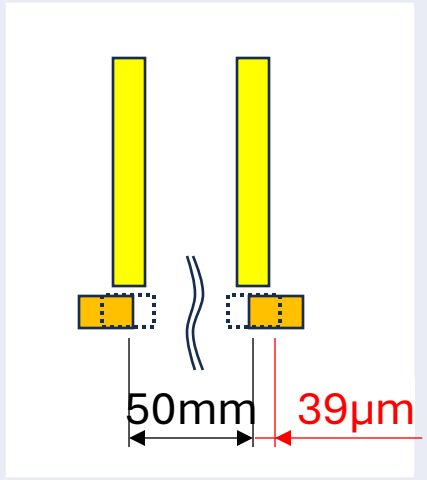
Total CTE 15.5ppm **-19%** **Total CTE 12.5ppm**

Thermal expansion (25 to 150deg.C)

Temp.	Conventional build up & Low CTE material	(New) Thin build up & Low CTE material
RT	0μm	0μm
HT	+48μm	+39μm

-19%



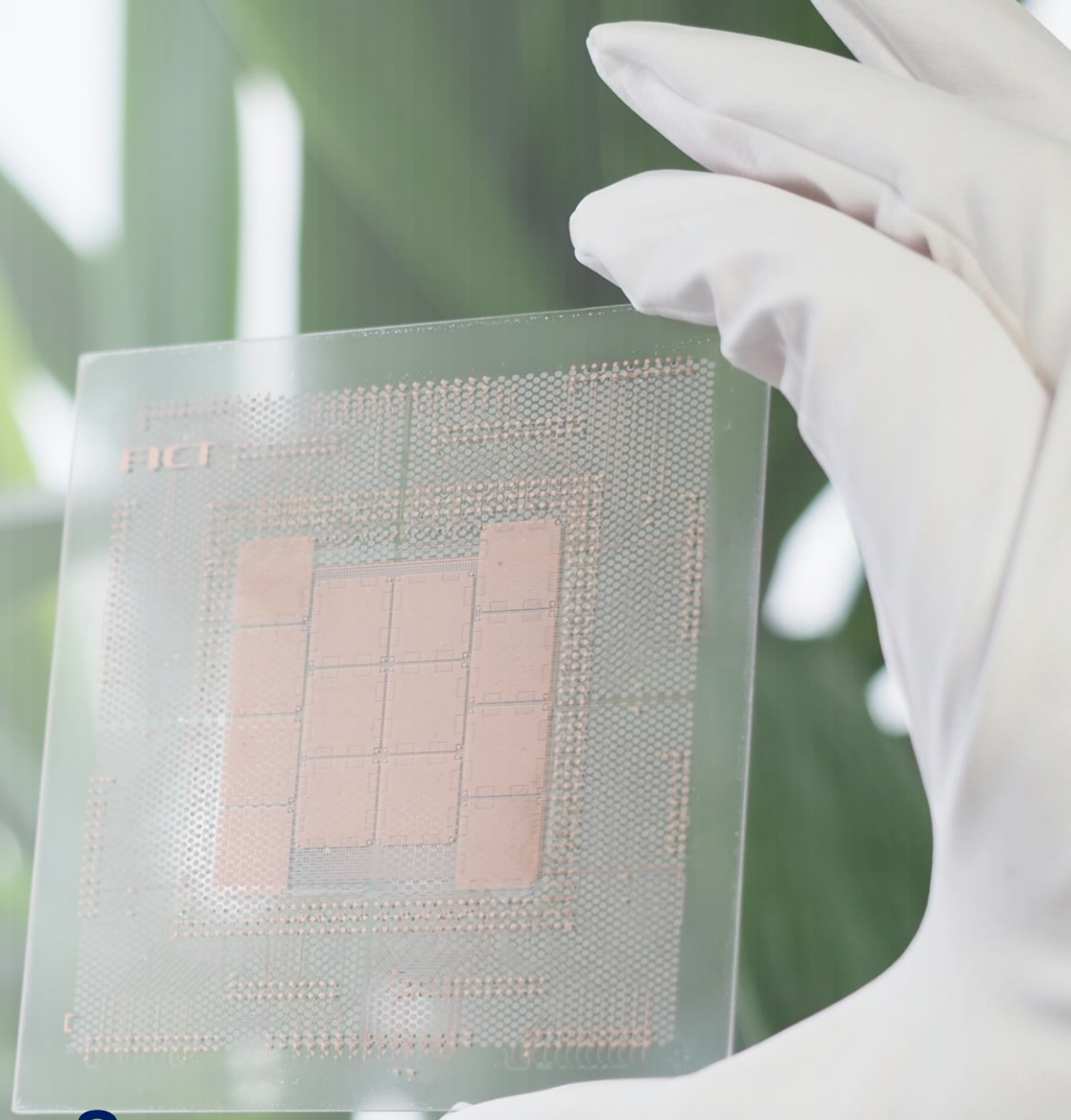


Pad position accuracy was improved by lowering substrate CTE.

Future Challenges

		TOPIC 1 : Pin Count Increase	TOPIC 2 : Fine Pitch Development
Goal		100K pins by 2024 200K pins by 2030	45μm pitch by 2024 30μm pitch by 2026
Challenges		Increasing build up layers up to 20 and more	1. Fine via pitch by using thin build up structure 2. Pad position control by lowering substrate CTE
Results		100K pins structure with 20 build up layers was realized by controlling CTE mismatch.	1. 45μm pitch structure was developed by using thin build up structure. 2. Pad position accuracy was improved by lowering substrate CTE.
Future Challenges	Near future	200K pins structure development by 2030 ⇨ Increasing build up layers up to 30	Development of fine pitch of 30μm by 2026 ⇨ Further thin build up structure
	Beyond 2030	Lowering CTE and warpage of substrate with higher build up layers ⇨ G-ALCS Technology (Glass Substrate)	Development of fine pitch of 20μm ⇨ G-ALCS Technology (Glass Substrate)

G-ALCS Technology (Glass Substrate)

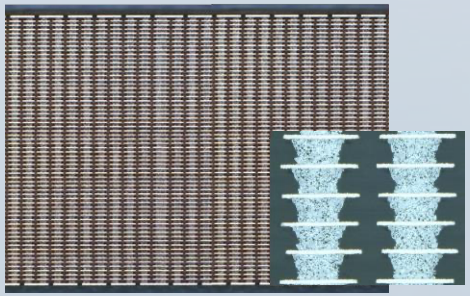


Glass **A**ll-**L**ayer Z-**C**onnection **S**tructure Technology

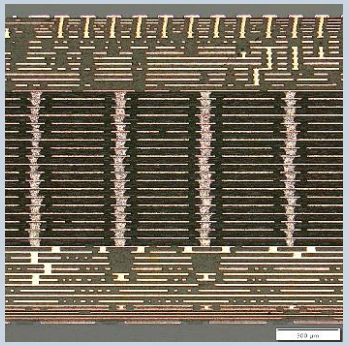
What is G-ALCS?

Current technology

F-ALCS



High layer PCB



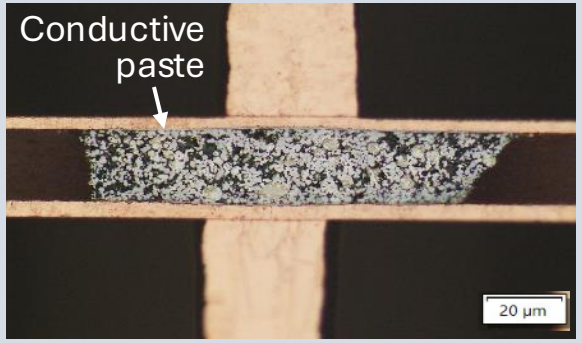
STO with F-ALCS core

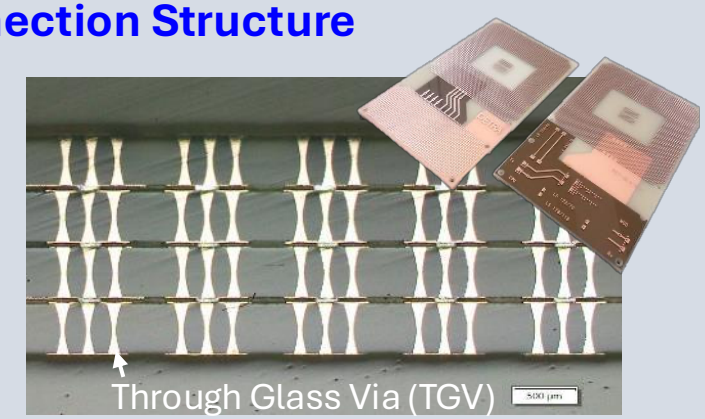
PATENTED FICT LIMITED TECHNOLOGY

New technology

G-ALCS

Glass All Layer Z-Connection Structure



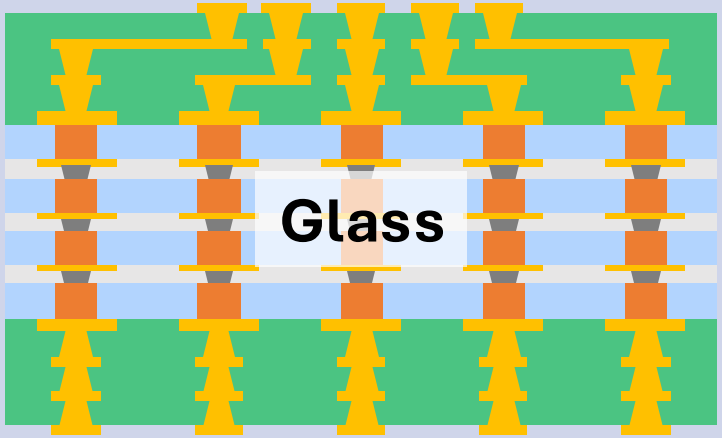
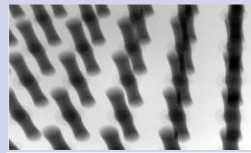


Features and benefits of our glass lamination

Feature	Benefit
Stack of thinner TGV	Yield and lead time imp. for high aspect ratio
Resistance to bending	Higher tolerability
Stack of glass	Components embedding
Any layer routing	Design flexibility
Low warpage	Fine pitch routing

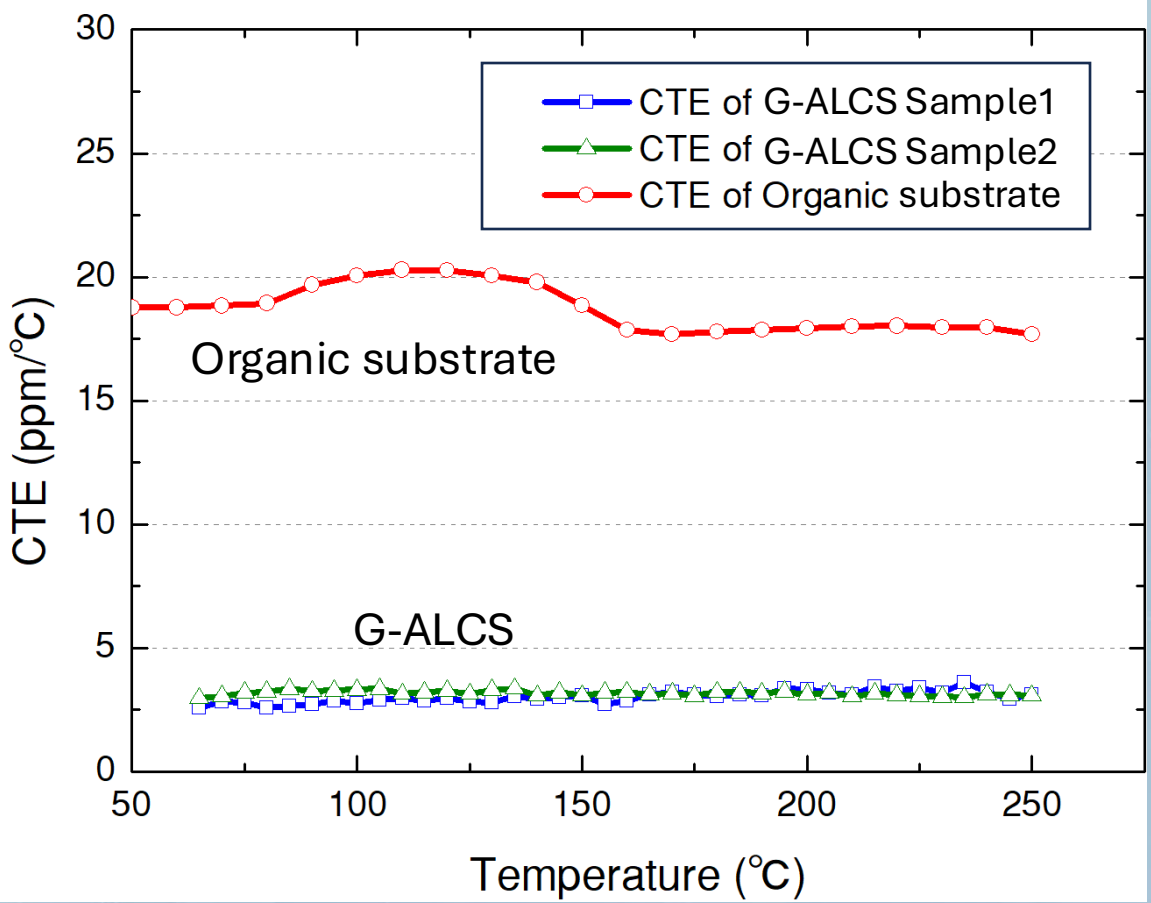
PATENTED FICT LIMITED TECHNOLOGY

Glass Core Space Transformer

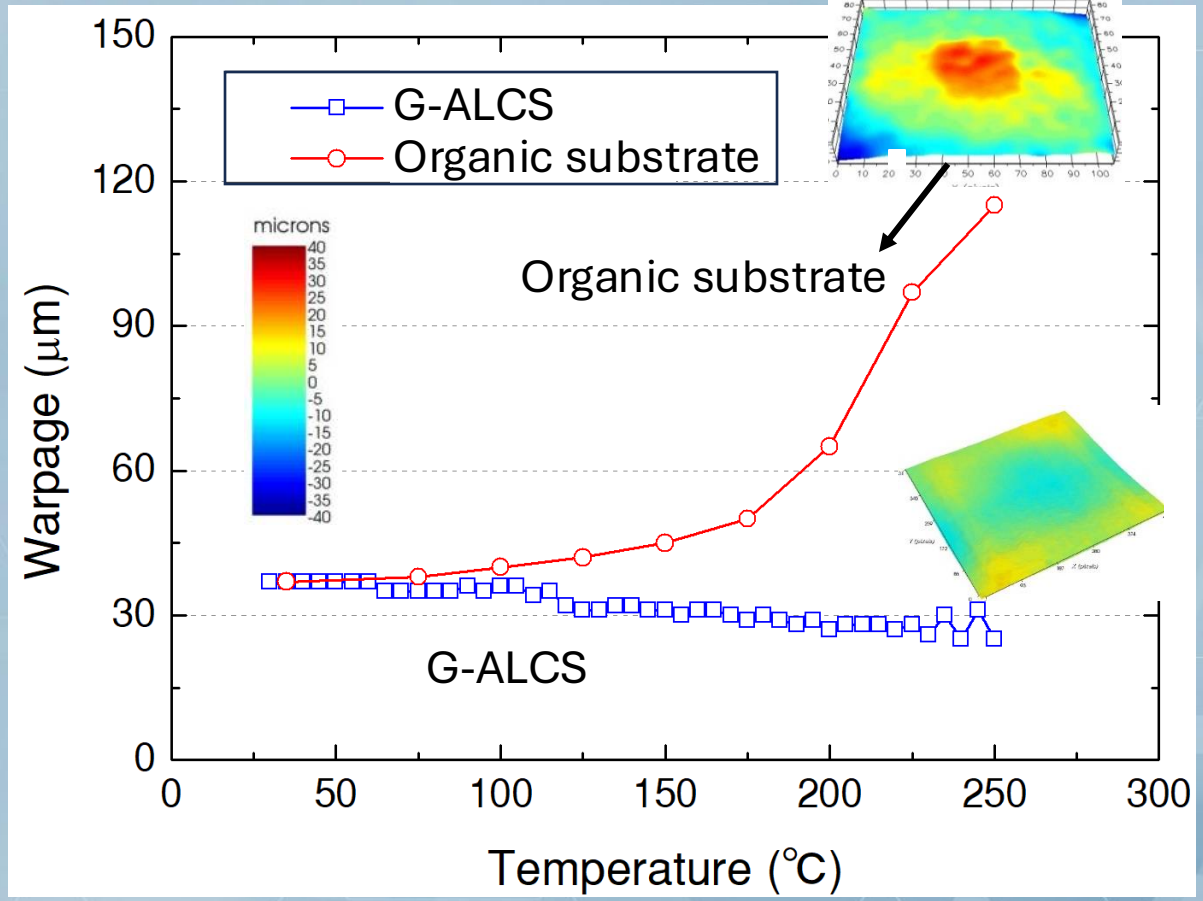
	Organic core	Glass core
Structure		  Ex：4L Core  Ex： 2L Core
CTE	6-16ppm/°C	3-7ppm/°C
Modulus	10-40GPa	50-90GPa
Tg	150-300°C	>600°C
tanδ	0.003-0.01	0.001
Roughness	0.1-1.0	<0.05

Characteristics of G-ALCS

CTE measurement

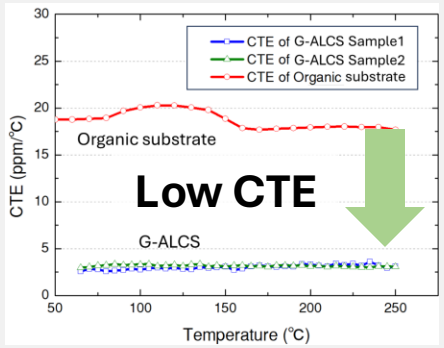


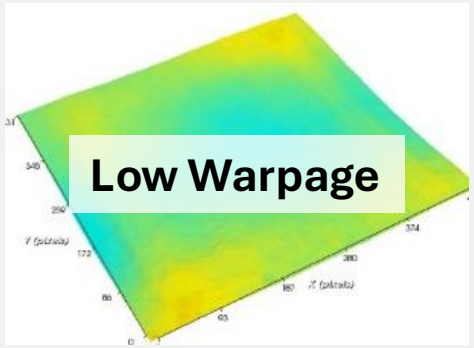
Warpage measurement

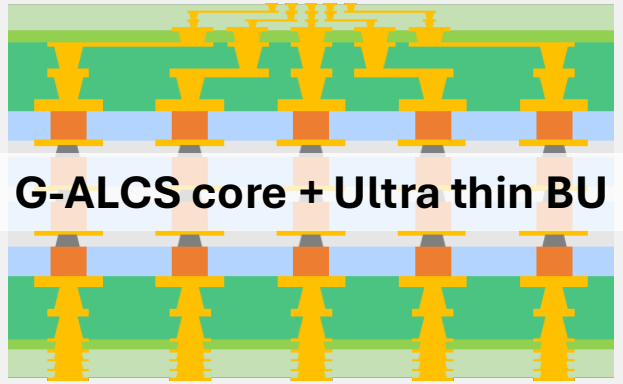


Future Challenges with G-ALCS

		TOPIC 1 : Pin Count Increase	TOPIC 2 : Fine Pitch Development
Goal		100K pins by 2024 200K pins by 2030	45μm pitch by 2024 30μm pitch by 2026
Future Challenges	Beyond 2030	Lowering CTE and warpage of substrate with higher build up layers ⇨ G-ALCS Technology (Glass Substrate)	Development of fine pitch of 20μm ⇨ G-ALCS Technology (Glass Substrate)
G-ALCS Technology		**Material properties allowing Low CTE and Warpage**	**20μm pin pitch by G-ALCS core with ultra thin build up structure**







Our Technology Roadmap

Large Size

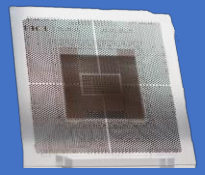
Low Warpage
Low CTE

Fine Pitch

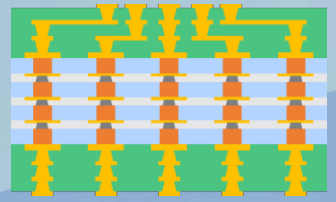
High Pin Count

Performance

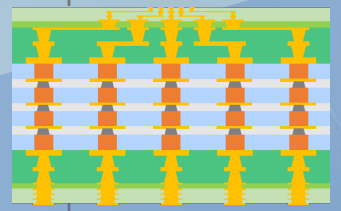
Space
Transformer
with GLASS



G-ALCS core + BU

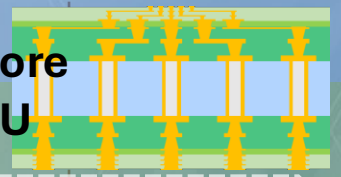


G-ALCS core
+ Ultra thin BU

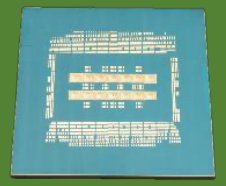


20μm pitch

Organic core
+ Thin BU



Space
Transformer
ORGANIC



45 μm pitch

30μm pitch

20μm pitch

Build up 20

Build up 24

Build up 30

BASE TECHNOLOGY

PKG Substrate, F-ALCS (Any Layer & Fine Pitch), High Layer PCB

2024

2027

2030

Conclusion

- **Latest Development Status of Space Transformer Organic**
  - Achievements
    - 100K pins structure with 20 build up layers
    - 45μm pin pitch using thin build up structure
    - Higher pad position accuracy by lowering substrate CTE
  - Future Challenges
    - 200K pins structure with build up layers up to 30 by 2030
    - 30μm pin pitch using further thin build up structure by 2026
- **Breakthrough Technology : G-ALCS (Future challenges beyond 2030)**
  - Lowering CTE and warpage of substrate with higher build up layers
  - 20μm pin pitch by G-ALCS core with ultra thin build up structure

THANK YOU !

If you have any questions, feel free to visit our Booth (No.307)
Or send an e-mail : fict-exhibition@fict-g.com

Latest Information Available on:

fict-g.com/en/

@fict9961

FICT LIMITED