



Enhancing Reliability and Accuracy in High-Speed KGD Testing through Comprehensive System Improvements



Giulia Rottoli - Product Owner - Technoprobe
Dario Villa - RF Product Marketing - Technoprobe

Agenda

- **The Need for Speed**
- **Device Overview**
- **Wafer Sort High Speed KGD Testing**
- **KGD Test Hardware configuration** – the importance to address all the marginalities for an accurate KGD high-speed testing:
 - Solved issues/ Unsolved issues
 - Resolutions and results
 - Probe card optimizations
 - Probe card and Prober interaction
 - Probe card and Tester interaction

The Need for Speed

Over the past several years, data center networks have faced a **dramatic increase in demand of optical modules**, driven by the advent of **hyperscale cloud data centers** and the rise of **machine learning**.

Hyper-connectivity within data centers has become crucial:

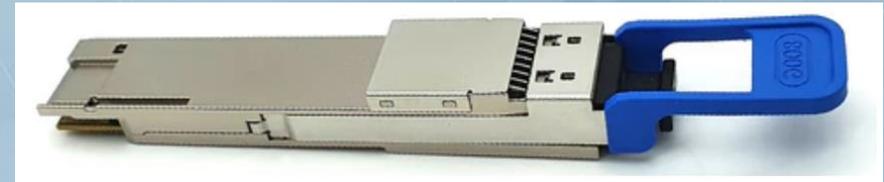
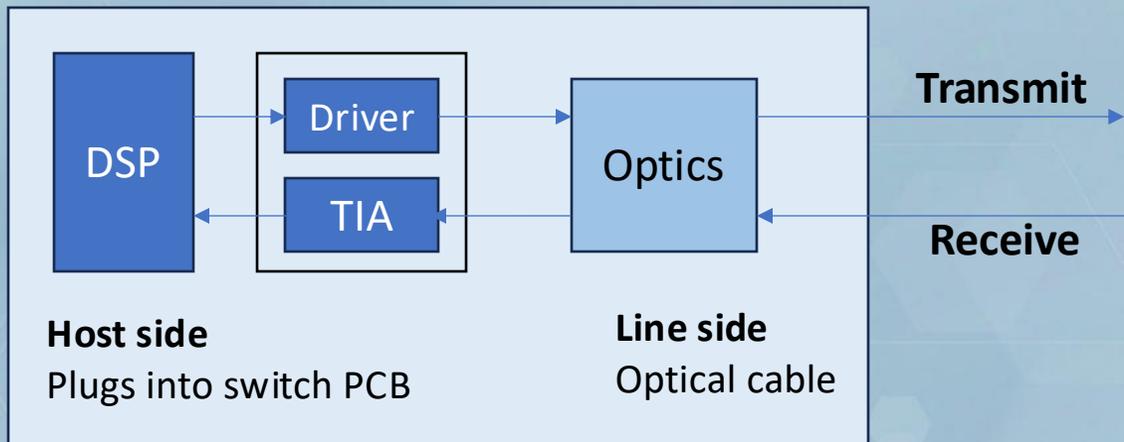
- High Bandwidth
- Low latency
- High reliability
- Low power consumption

These features necessarily lead to the adoption of more efficient modulation techniques, replacing NRZ with **PAM4**.

The convergence of these forces in the network have resulted in a **massive ramp of PAM4 based systems and modules**, with demand for multi-millions of ports per year.

Device Overview – PAM4 Optical DSP

PAM4 Optical DSP is a device which enables the optical interconnection inside the cloud and AI data centers.



Device Overview

For this work, a device with following features has been used:

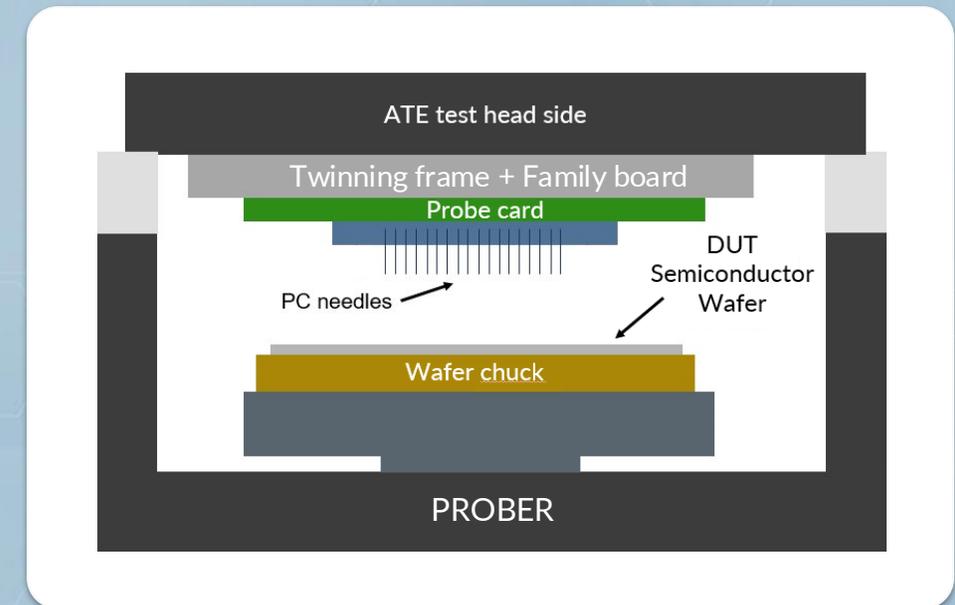
- PAM4 Optical DSP with integrated TIAs and laser drivers
- 4 x 50G (56 Gbps) TX and RX both Host side and Line side.
- 70 μm pitch

Probe Card has been designed both in x2 and x4 parallelism

Wafer Sort High Speed KGD Testing

Introduction

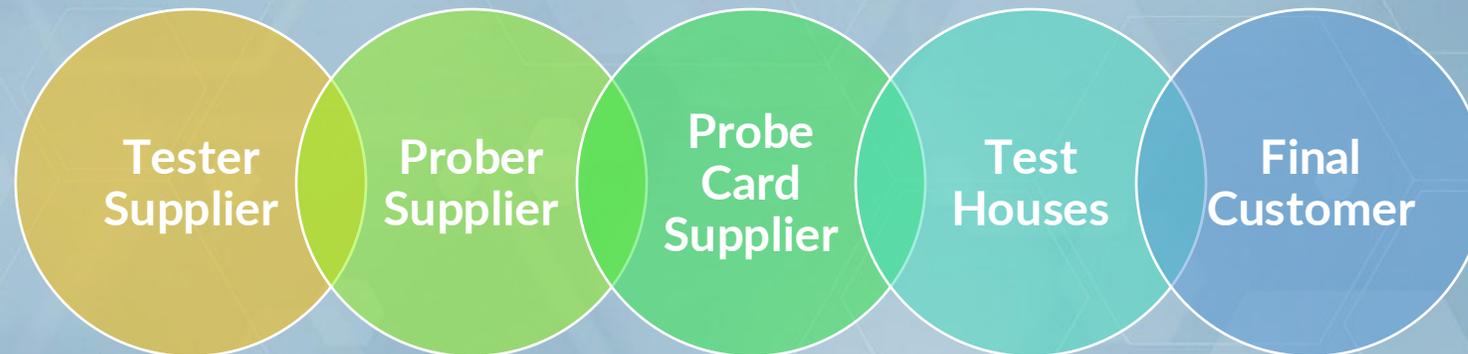
- **Wafer Sort:** Functional testing of a chip while it is still on the wafer.
- **KGD (Known Good Die):** Die that has passed the functional test and is ready for packaging.
- **High-speed testing:** Functional tests are conducted at high speed and frequency to simulate the actual usage conditions of the devices under test.
- The **twinning solution** was introduced to enable high speed testing in wafer sort with limited external loopback testing capability.



KGD Test Hardware configuration

Overview

- The **mechanical** and **electrical interaction** between the prober, probe card, and tester is crucial during high-speed testing to minimize signal loss and ensure signal integrity.
- An optimal KGD hardware configuration requires strong **collaboration** and **coordination** among all contributors within the wafer testing supply chain.

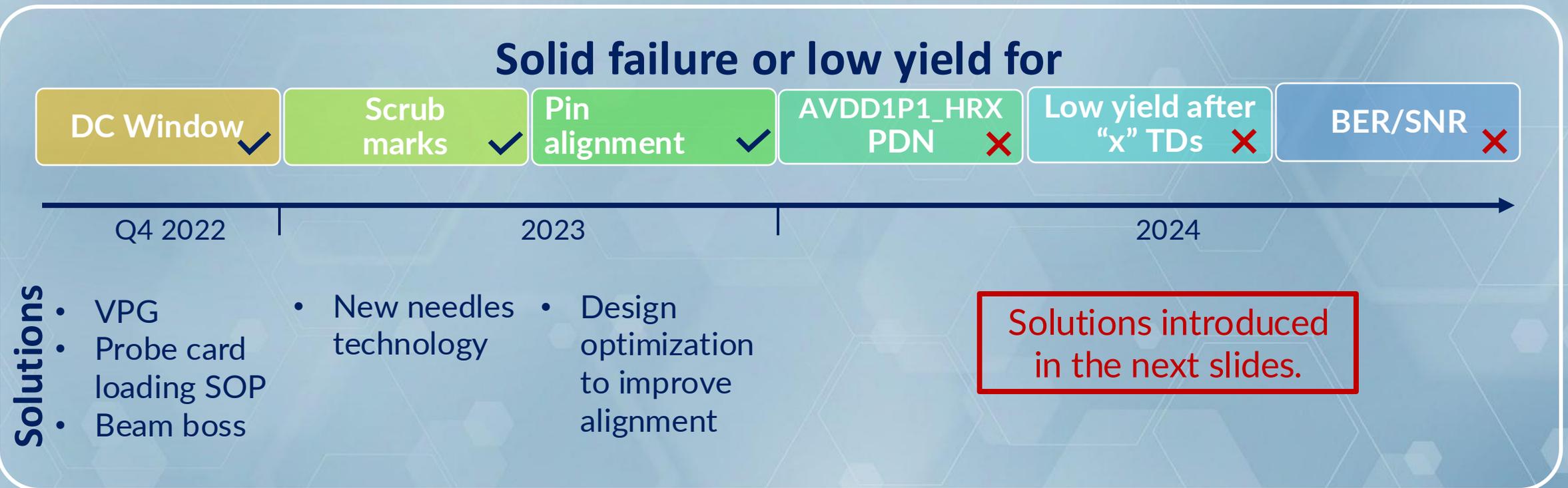


KGD Test Hardware configuration

Solved/Unsolved issues

- If the mechanical and electrical interaction between the prober, probe card, and tester is inefficient, the final yield will not accurately reflect the true yield of the wafer, as it will be compromised.

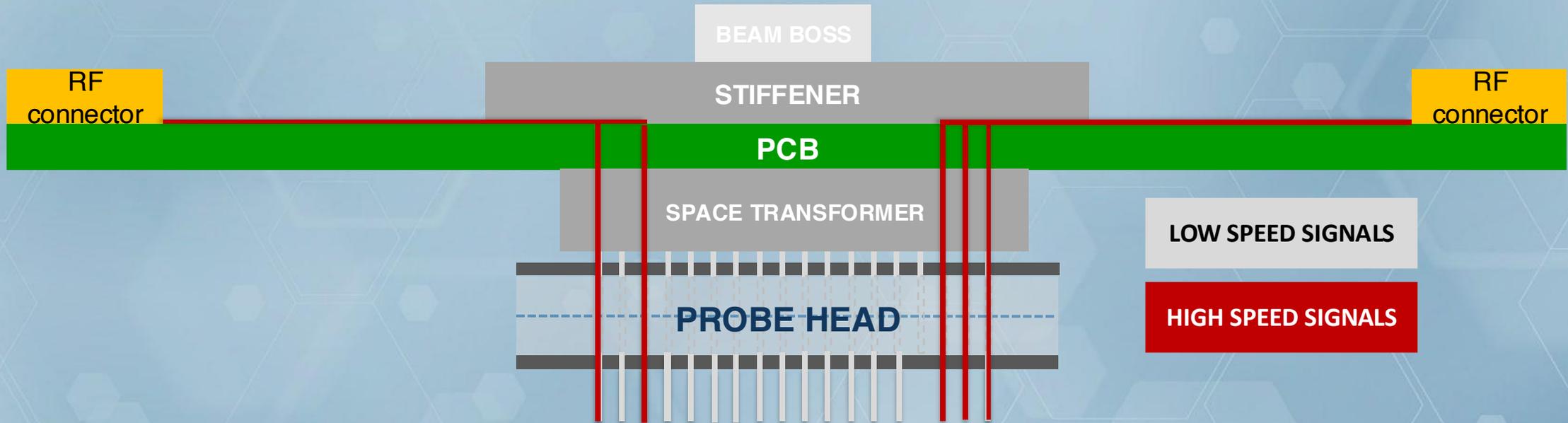
Solid failure or low yield for



Probe card

Phantom Technology

- Phantom probe head technology is a hybrid
 - Low speed signals, power and GND with TPEG™ vertical MEMS needles
 - High speed signals and GND with RF needles



Probe card

Design Improvements

Old design



Modification

Shorter RF traces

RF cabling optimization

From coaxial to SMD 50 Ohm termination

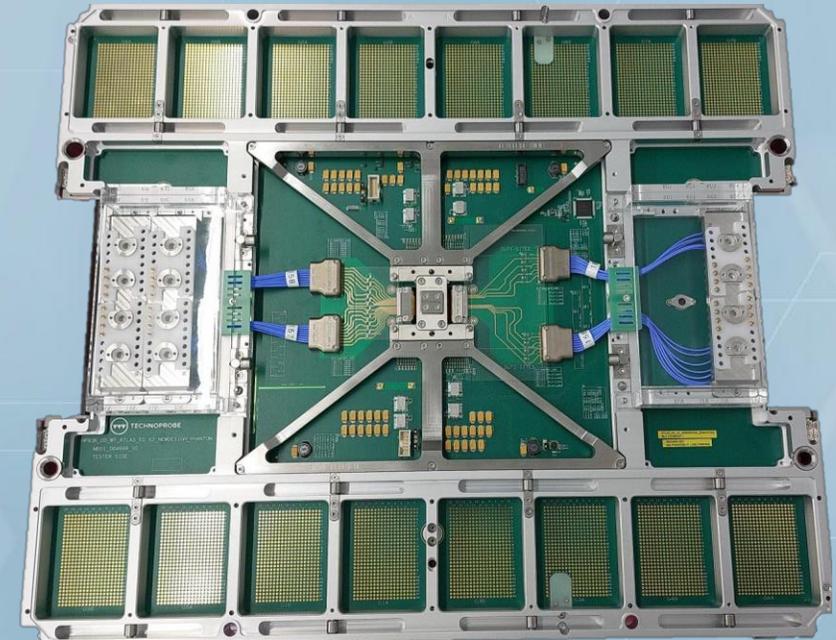
Improvement

Lower IL

RF performance

Less RF cables

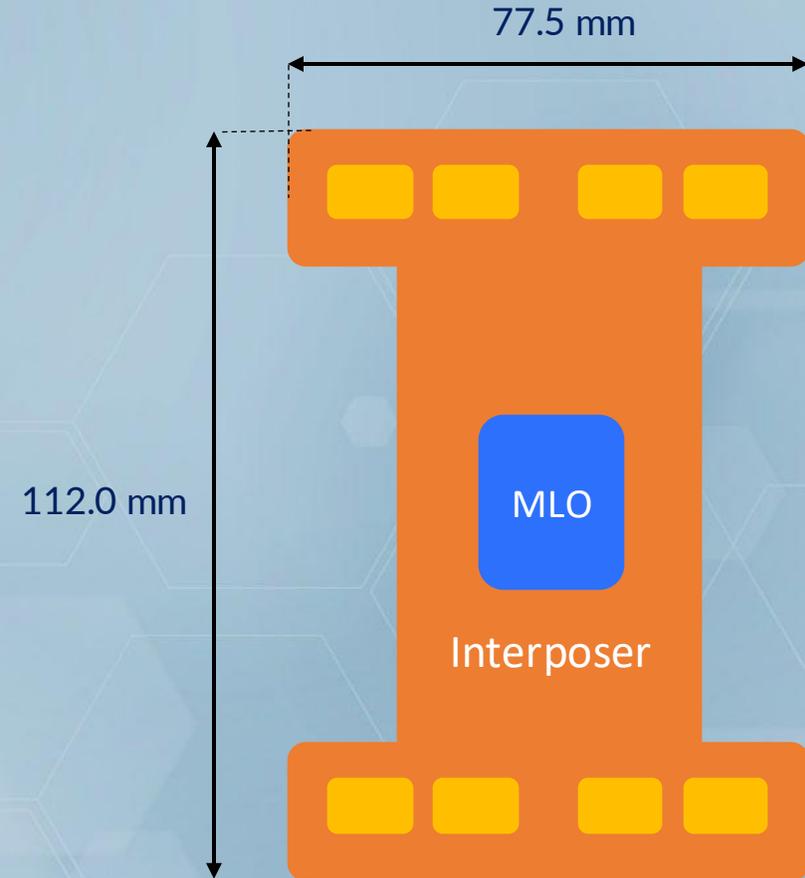
New design



Probe card

Design Improvements

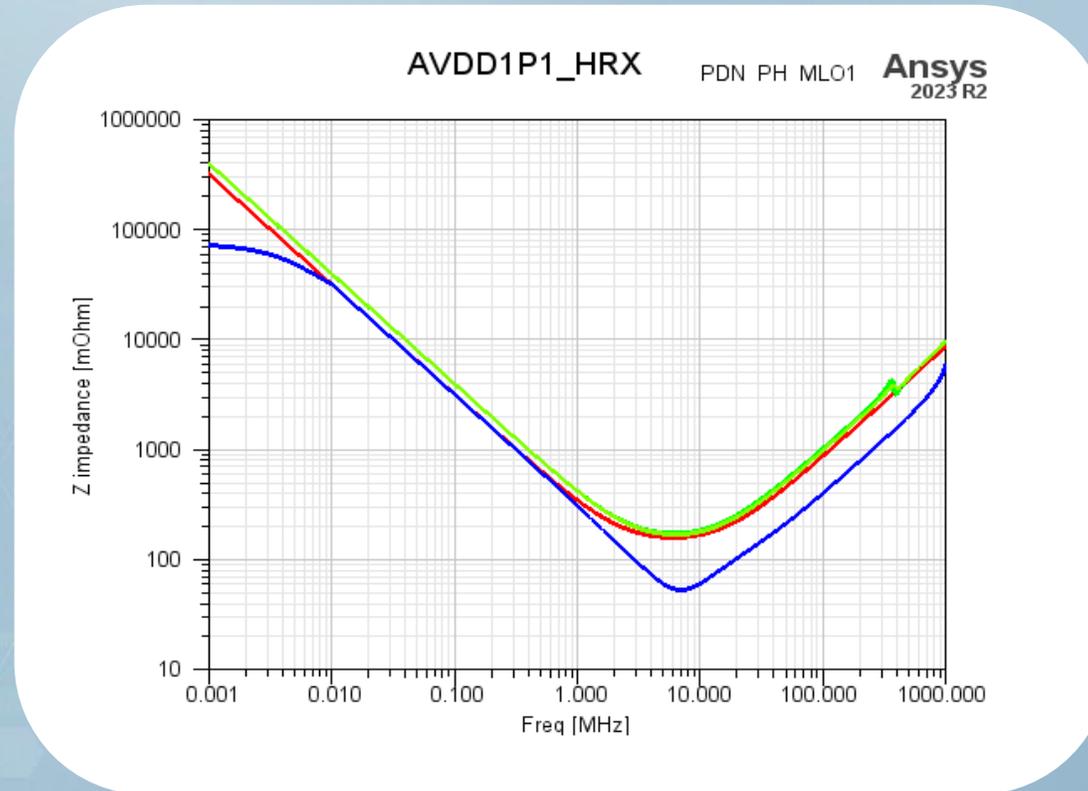
- **Modification**
 - From Interposer to MLO interconnection
- **Improvements**
 - Compact solution: more room for RF routing
 - Better PDN (closer decoupling caps)
 - Thinner interconnection
 - Reflow interconnection: no contact oxidation issues



Probe card

PDN performances

- **Modification**
 - AVDD1P1_HRX probed with RF needles
- **Improvements**
 - Power and sense closer to the DUT



DC Needles - Interposer

Freq [MHz]	Z [mOhm]
25	301.83
50	541.31
100	1040.75

DC Needles - MLO

Freq [MHz]	Z [mOhm]
25	301.83
50	541.31
100	1040.75

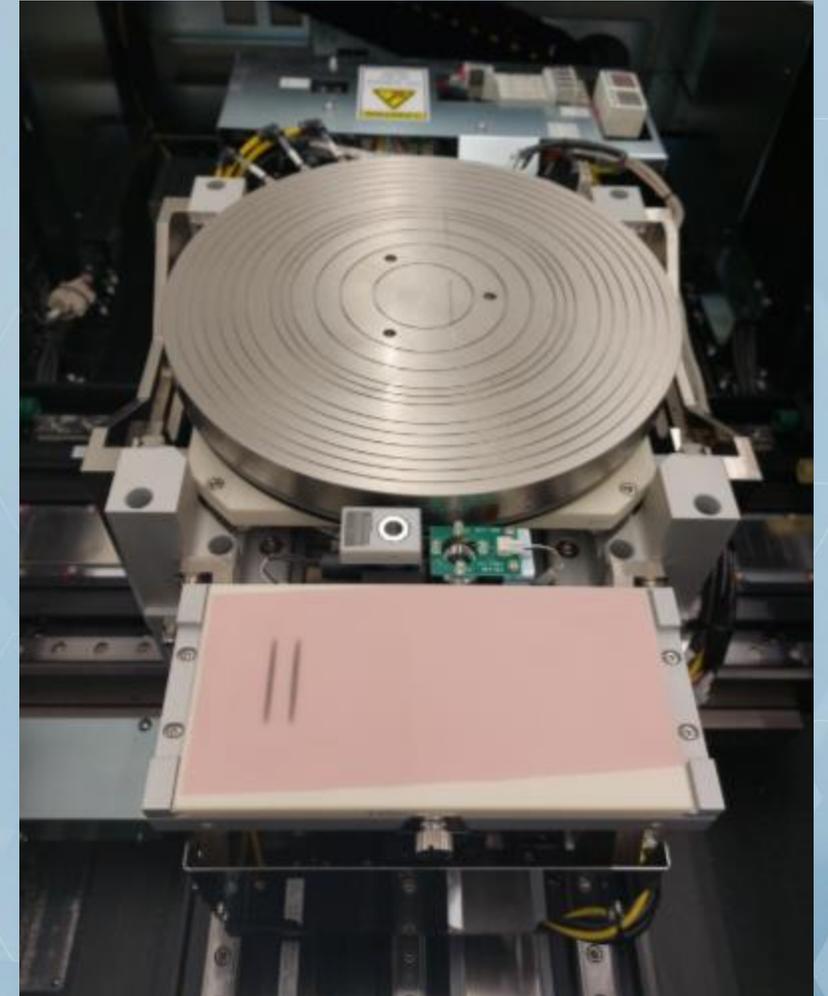
RF Needles

Freq [MHz]	Z [mOhm]
25	115.21
50	205.28
100	387.31

Probe card and Prober interaction

Cleaning Unit setup

- At high frequencies, KGD testing become more sensitive to small residues or oxidation on the probes
- It is therefore important depending on prober type:
 - to devise a suitable **cleaning recipe** to maintain a stable yield over time
 - Check **Cleaning unit** level with respect to **Wafer chuck** (maximum mismatch 10 μ m)

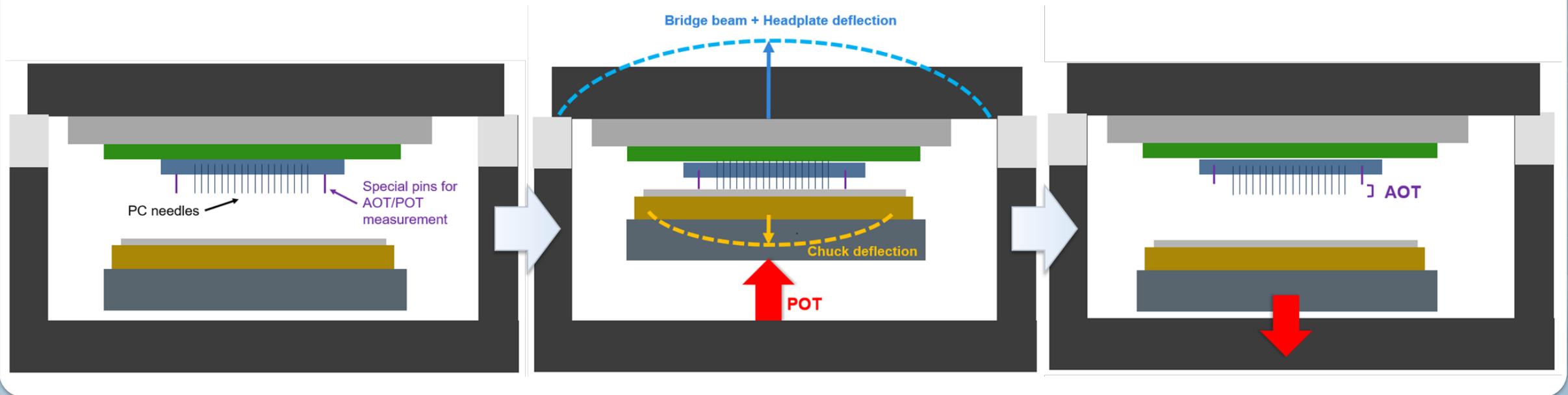


Probe card and Prober interaction

POT/AOT

- Analysis of the **compliance/flexibility** of the PC and prober system is essential for the probes to undergo the OT probing for which they have been characterized

POT/AOT measurement method

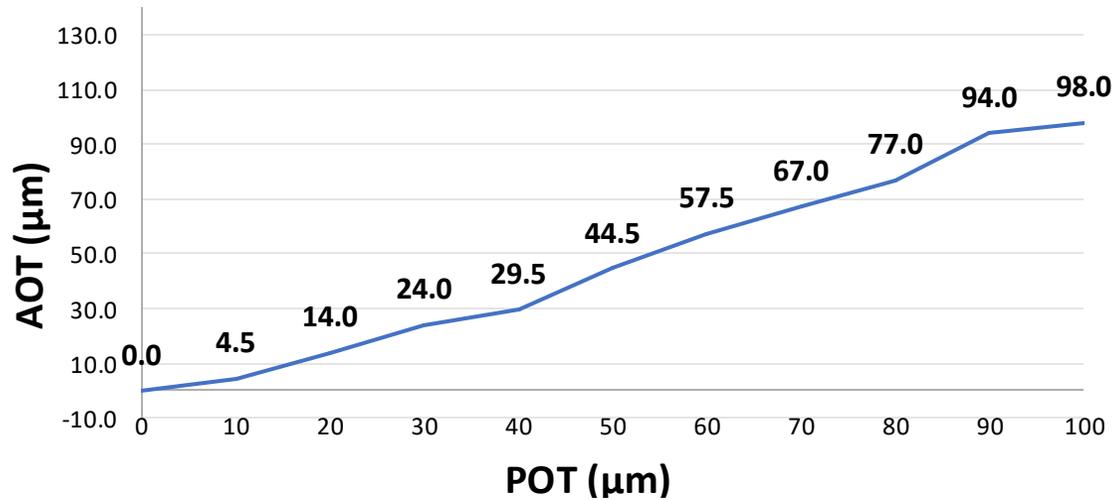


Probe card and Prober interaction

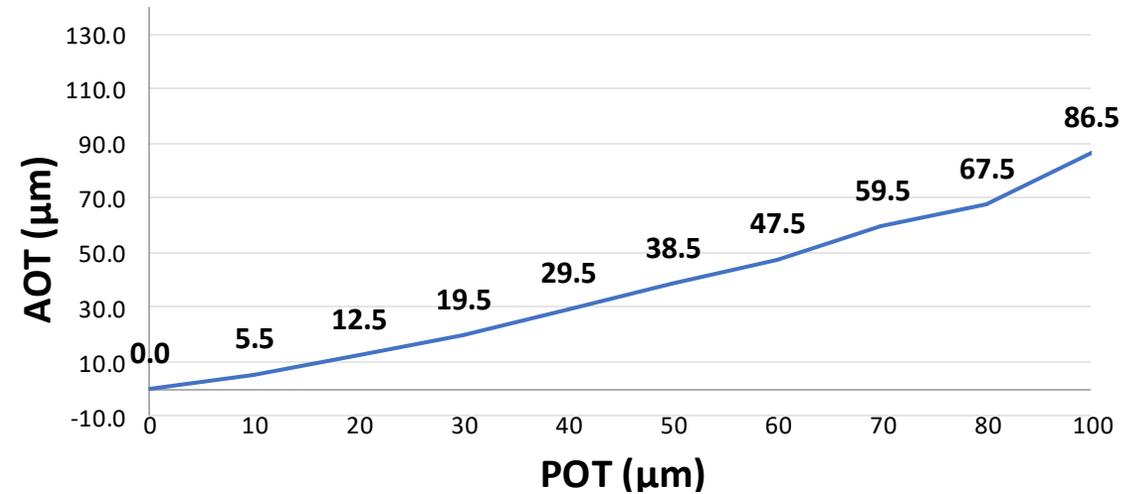
POT/AOT

- POT/AOT study depends on the type of prober of the Test Houses.

AOT vs POT type 1



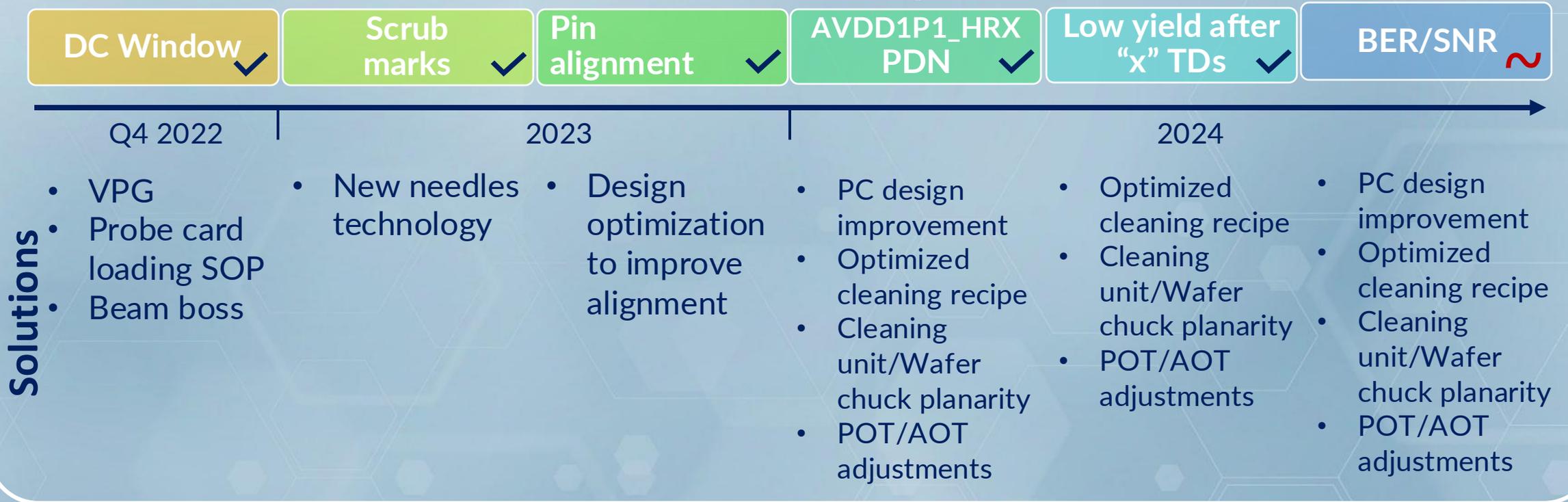
AOT vs POT type 2



KGD Test Hardware configuration

Solved/Unsolved issues

Solid failure or low yield for



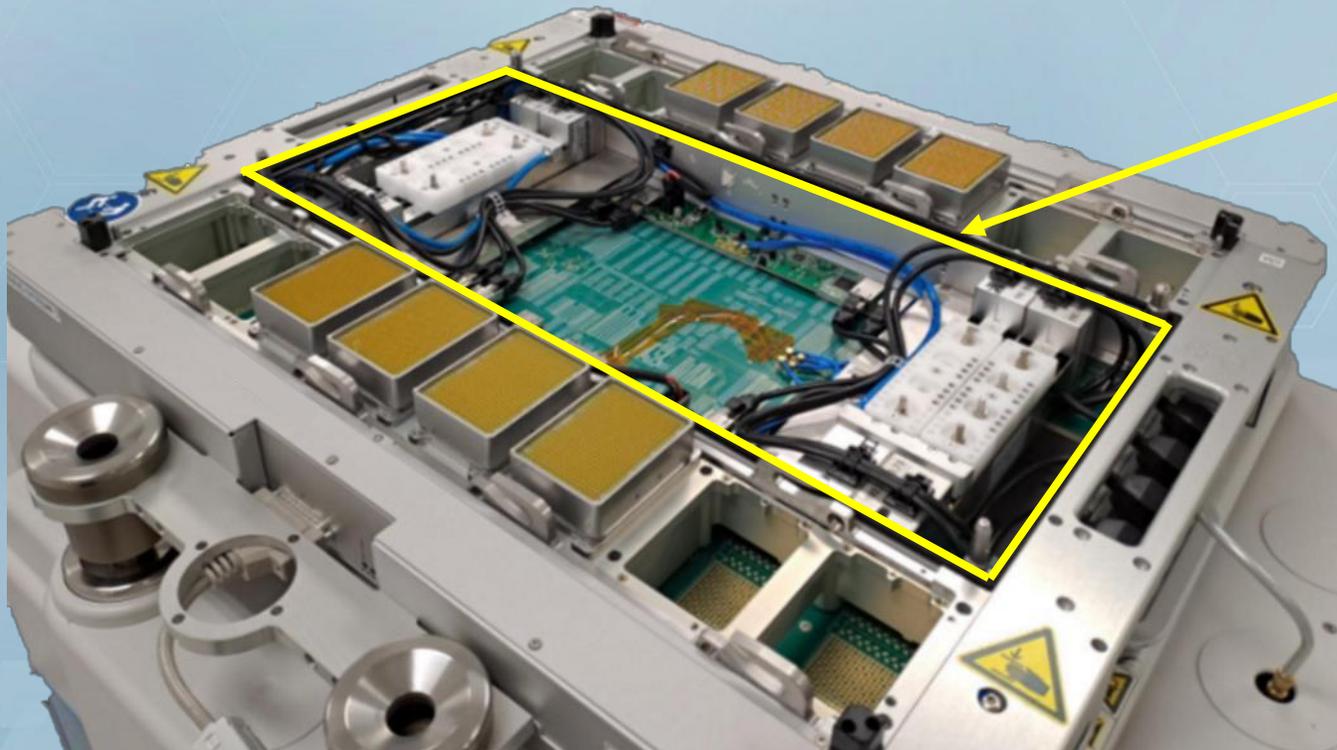
Low-yield BER/SNR – probe card vs Prober/Tester dependence

Root cause hypothesis: no proper mechanical interaction between Probe card and Tester

Probe card and Tester interaction

Twinning solution

- The structure, on the probe side of the tester head, that enables **high speed testing**, ensuring signal integrity and improving the overall efficiency of the wafer sort process is the **twinning solution**



Twinning frame

Probe card and Tester interaction

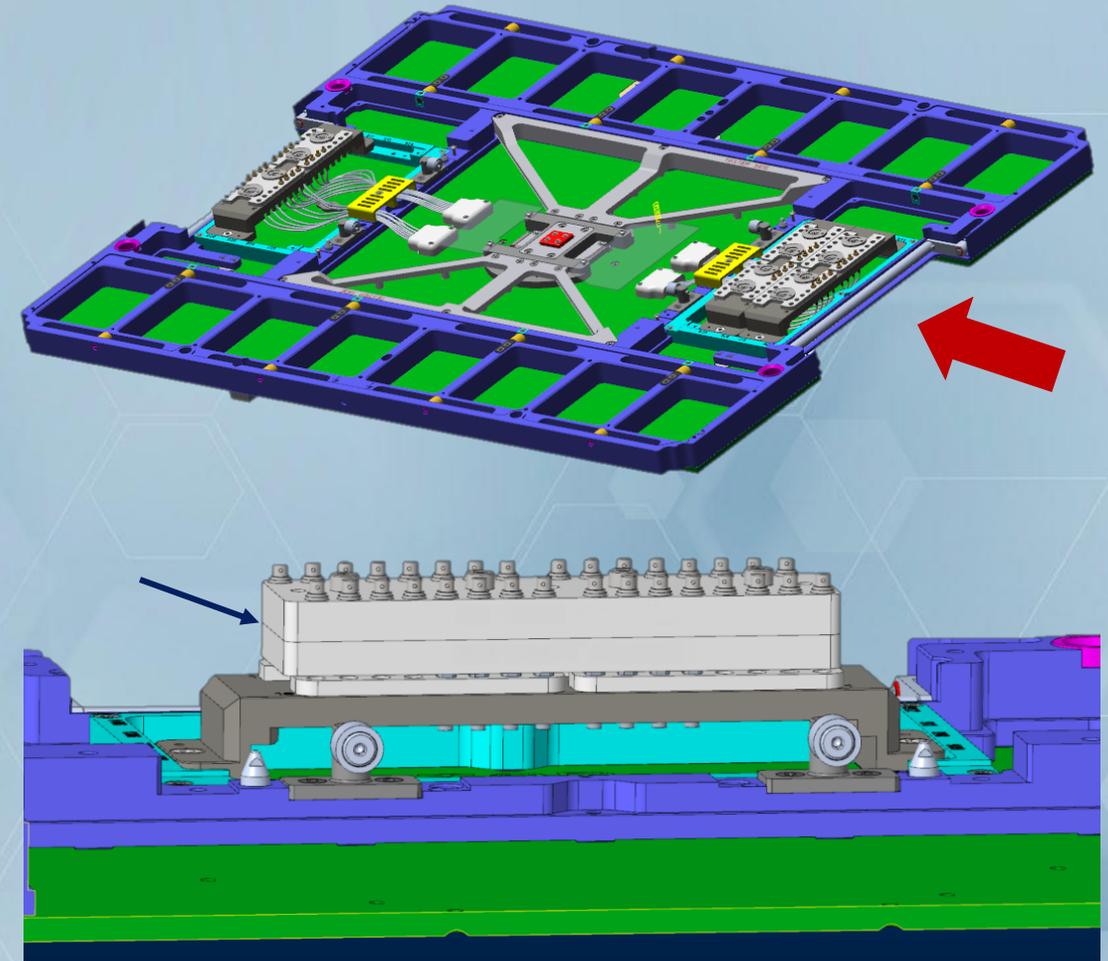
Tester Head

Proper management of **mechanical transitions** between the probe card and tester is essential to ensure that high-speed tests are reliable, accurate, and repeatable.

A stable **mechanical contact** helps reduce signal loss.

- **Mechanical instability** can cause intermittent errors or false negatives, decreasing test accuracy.
- Excessive **vibrations** compromise signal quality, especially at high frequencies, leading to potential test malfunctions.
- Mechanical transitions between the probe card and tester are subject to **wear over time**, affecting contact quality.

The convergence of the last three factors results in an overall reduction in test yield.



Conclusion

Collaboration in Wafer Sort High-Speed KGD Testing

- The **Wafer Sort** process is essential for filtering out malfunctioning dice, significantly reducing production costs and improving overall yield.
- The complexity and precision required for wafer sort demand strong **collaboration** and **coordination** between all contributors in the wafer testing supply chain, from probe card manufacturers to prober and tester suppliers.
- This approach is applicable to all types of semiconductor devices. Effective collaboration and clear communication between customers and suppliers are not only critical for **technological development** but also for the **introduction of new technologies** and the **optimization of existing ones**.
- This was the approach used by Marvell, Technoprobe, and all parties involved in this development that has led to significant improvements in **RF performance**, **power delivery network (PDN)**, and the **mechanical behavior** of the entire system.

Thank you!

Acknowledgement

The authors express their gratitude to **Marvell** as well as **Nicolò Renna, Kanjully Sumesh, Fabiola Graziani, Andrea Delfino** and **Luca Carella** from Technoprobe for their valuable contribution to this paper.

Giulia Rottoli
Product Owner
Technoprobe Italy
giulia.rottoli@technoprobe.com

Dario Villa
RF Product Marketing
Technoprobe Italy
dario.villa@technoprobe.com