SWTEST ASIA
PROBE TODAY, FOR TOMORROW

“Challenges and Solutions in Wafer Testing” from Viewpoint of Back-end Process of Power Semiconductors

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Overview

1. What is Power Device?
2. Market and Trend
3. Challenges in Wafer Testing from Viewpoint of Back-end Process
4. Solution (Prober side)
5. Solution (Tester side)
6. Conclusion

Power Device

- **Where are they used?**

Electric Vehicles (EVs): cars, trains, ships…

Renewable Energies: solar, wind…

Efficient power supplies: chargers, mobile…

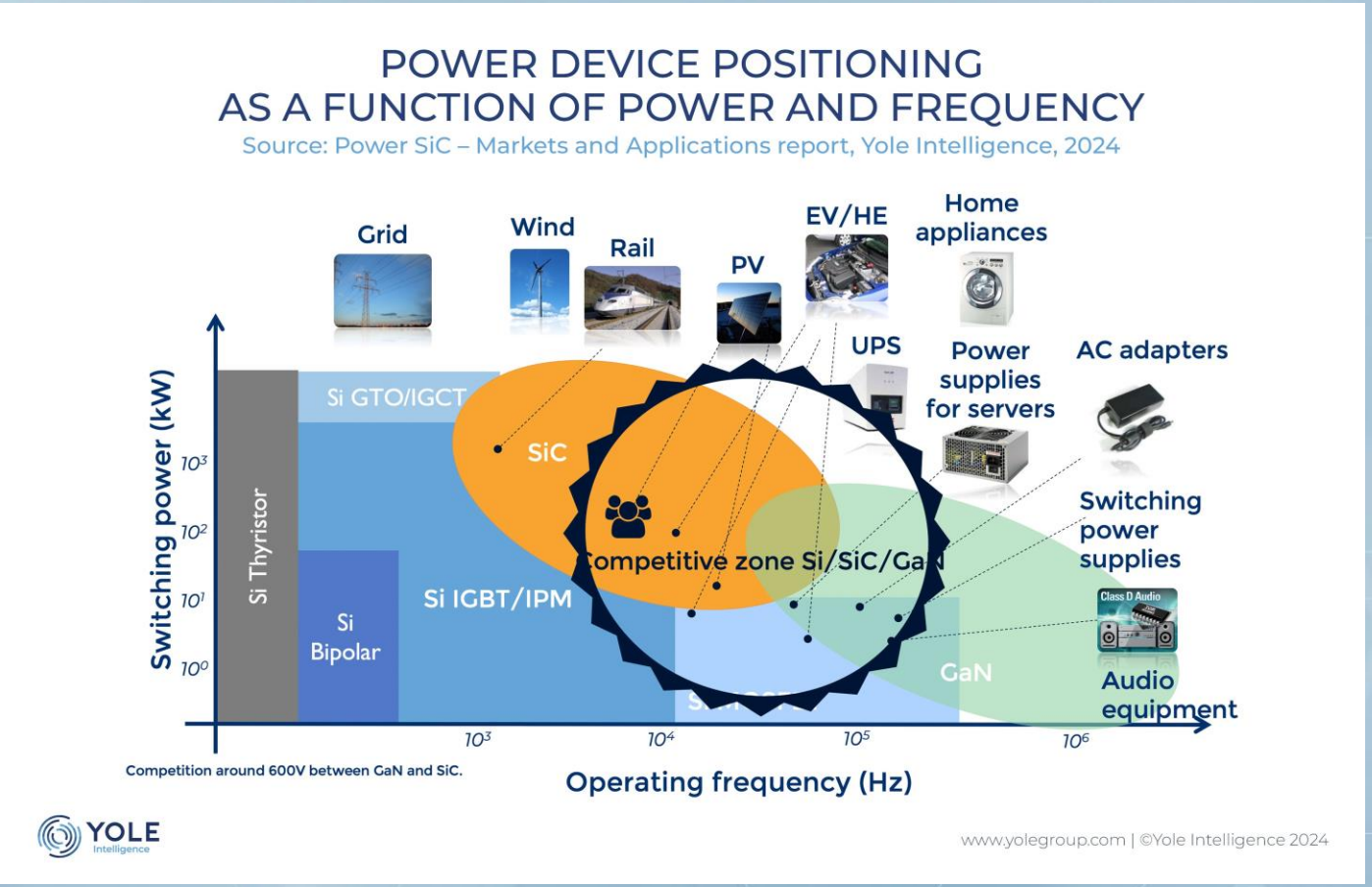
- **Types**

Discreates: MOSFET, IGBT, Diode…

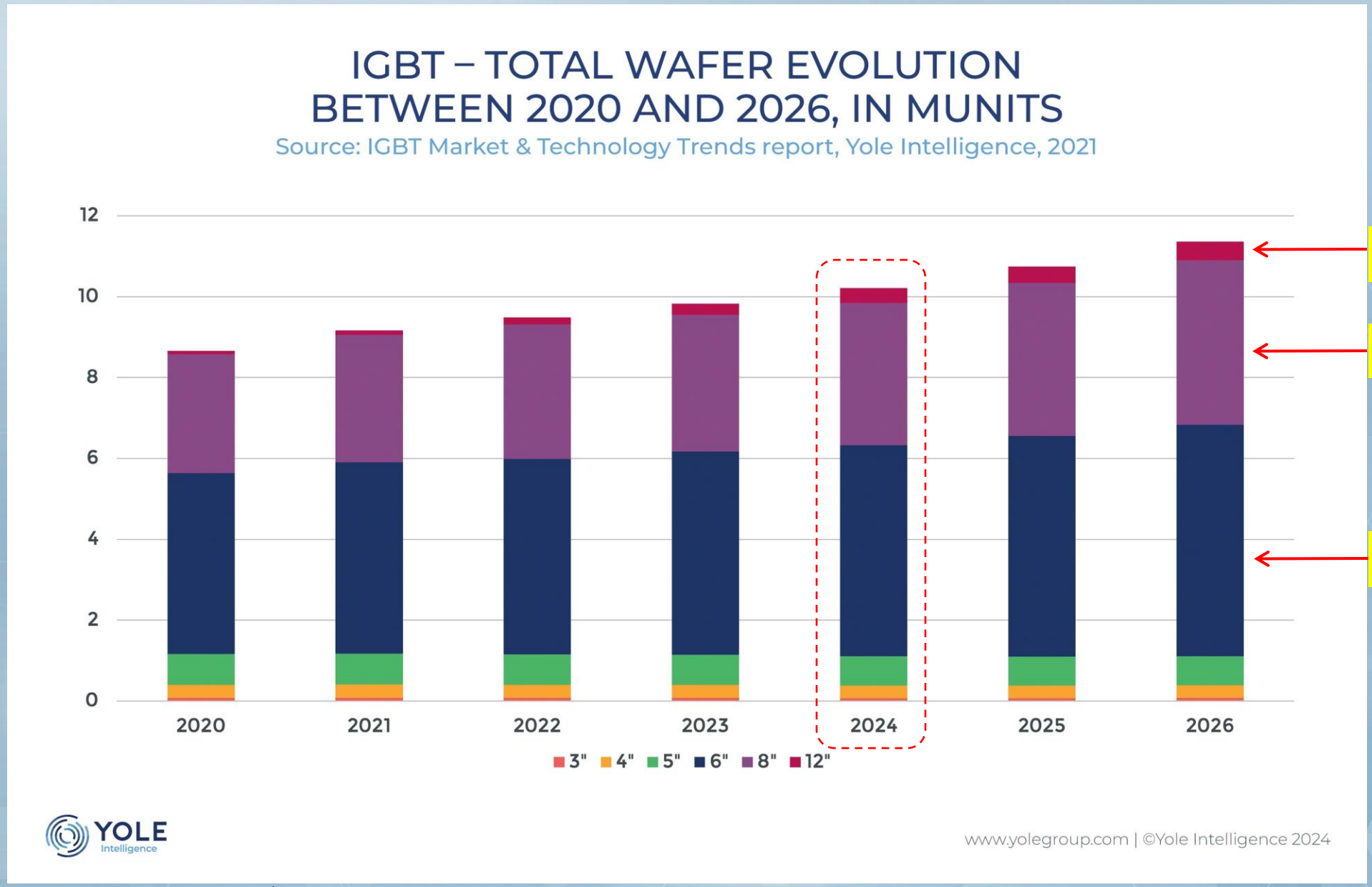
- **Material**

Si: well proven and low cost…

SiC, GaN: fast switching, smaller, lighter and more efficient…



IGBT Market


IGBT – TOTAL WAFER EVOLUTION
BETWEEN 2020 AND 2026, IN MUNITS
Source: IGBT Market & Technology Trends report, Yole Intelligence, 2021
12
10
8
6
4
2
0
2020
2021
2022
2023
2024
2025
2026
3"
4"
5"
6"
8"
12"
12”
8”
6”
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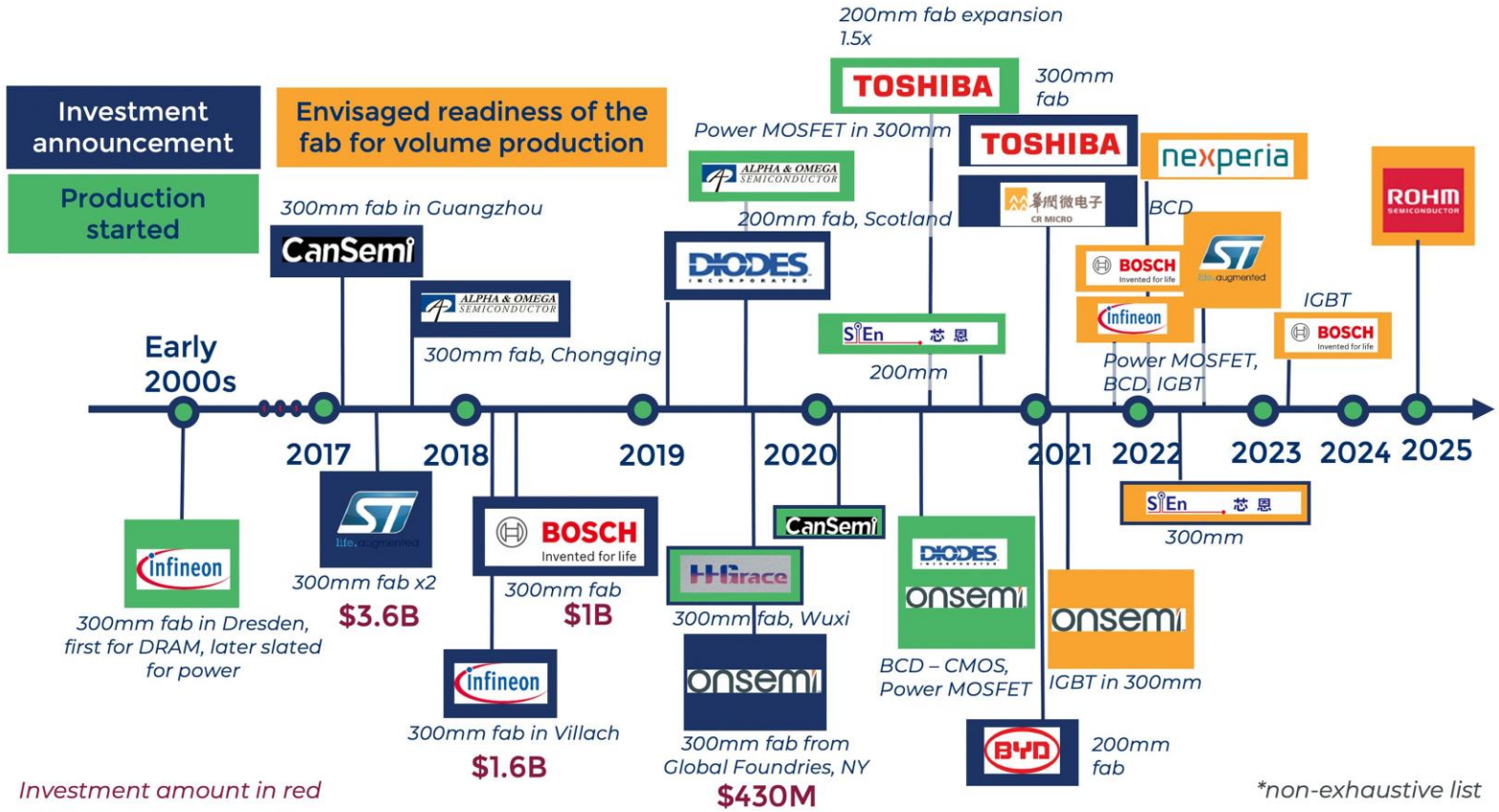
IGBT Market

FAB INCREASE - DEVELOPMENT TIMELINE: 200 & 300 MM FAB EXPANSION

Source: IGBT Market & Technology Trends report, Yole Intelligence, 2021



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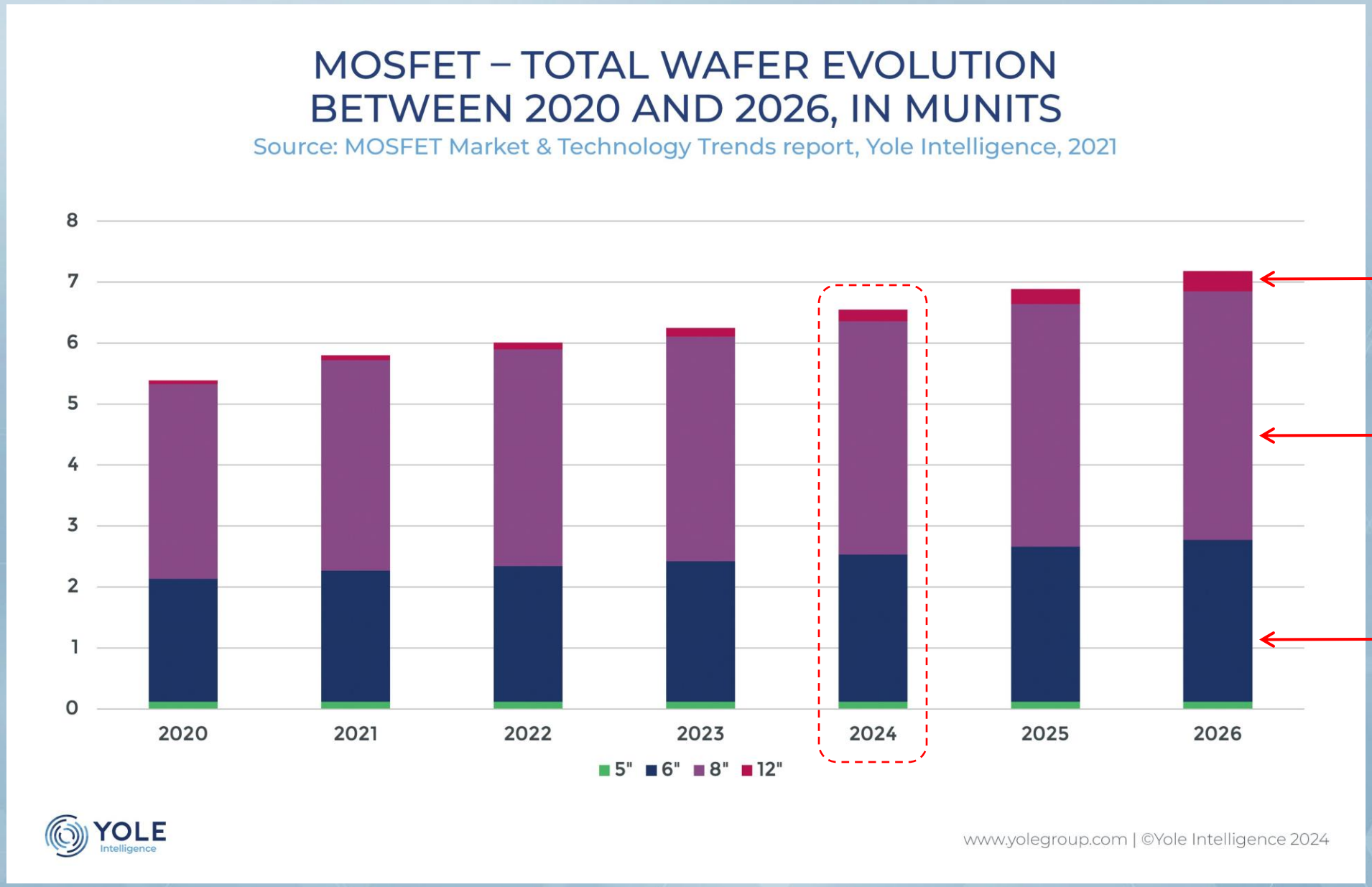
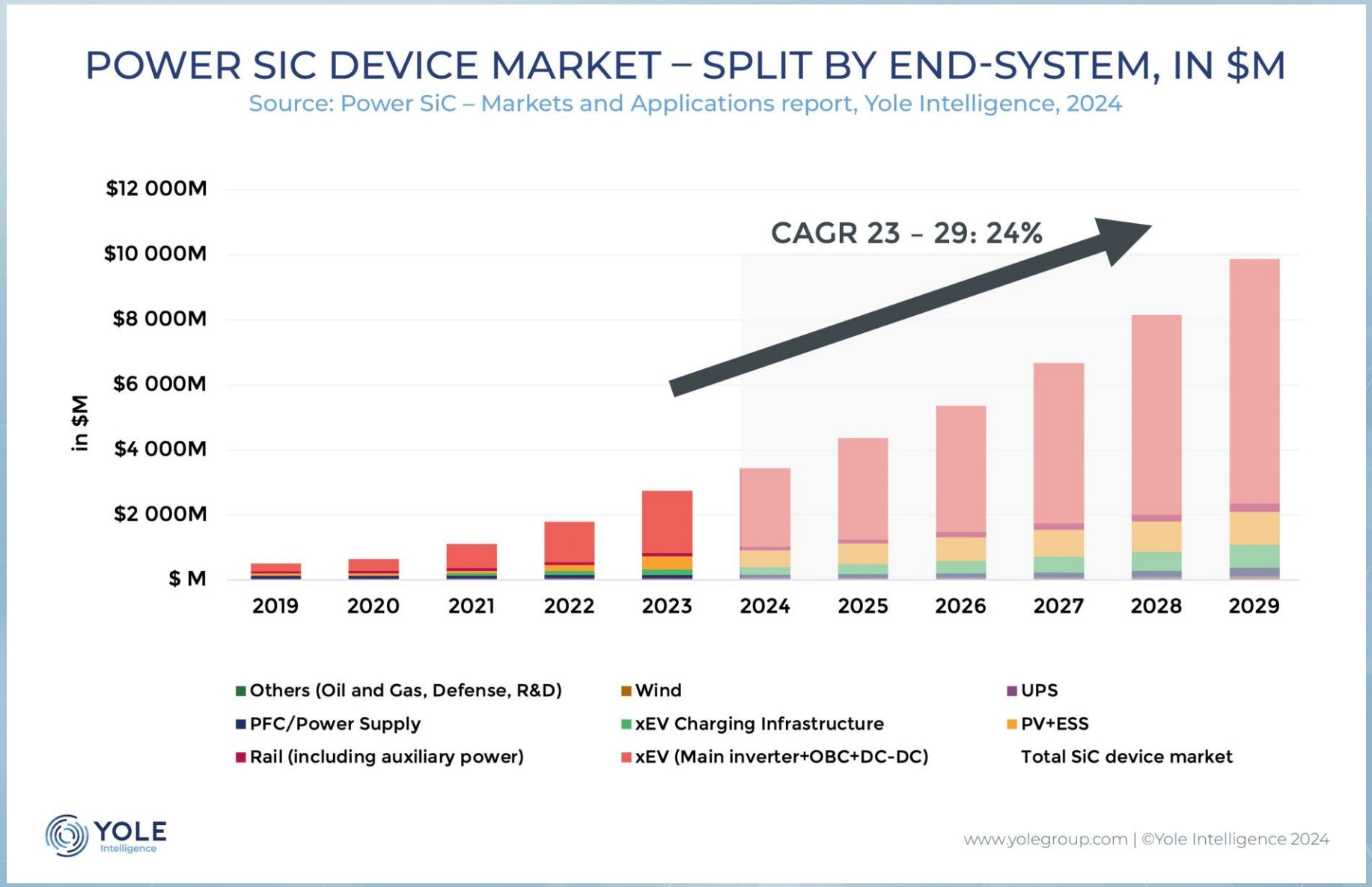
Si MOSFET Market



SiC Device Market Split by application



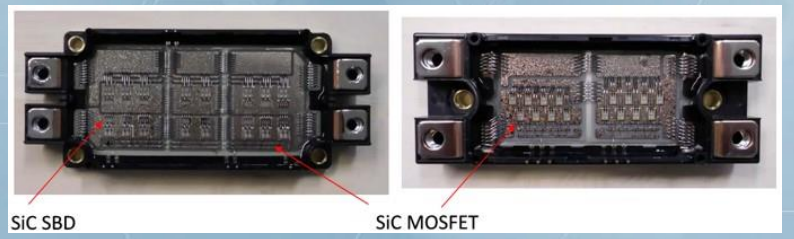
Challenges in Wafer Testing from Viewpoint of Back-end Process

Technological Issues of SiC Device and Future Prospects

To further expand the use of SiC power devices, it is necessary to develop low-cost, highly efficient, and highly reliable device manufacturing technologies. For this purpose, it is important to develop SiC single-crystal fabrication technology with large diameter and low defect density

Challenge 1

Power module consists of some power devices, wafer test process is required to isolate good or bad die as much as possible so that bad die does NOT move on to next process



Goal = Perfect inspection of the device on Wafer

- **DC Test**
- **UIS Test (Unclamped Inductive Switching Test): Screening of die with lattice defect**

Prober side & Tester side

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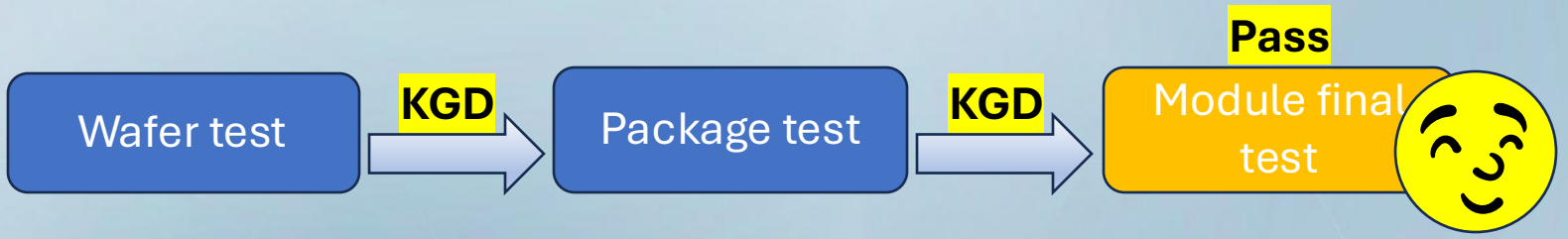
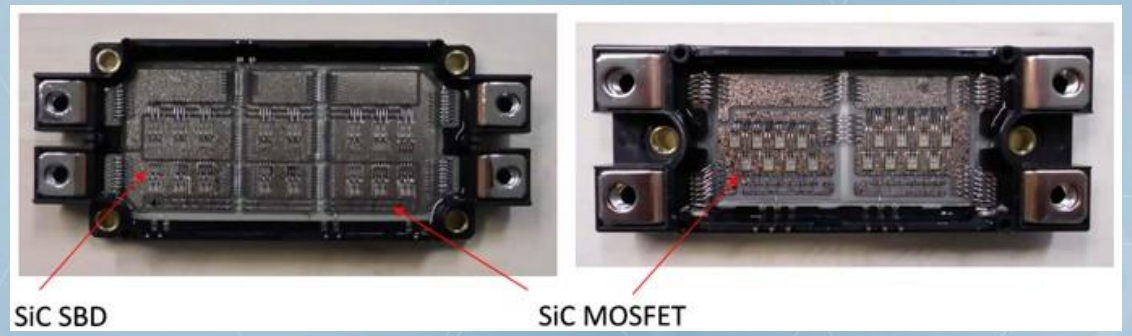
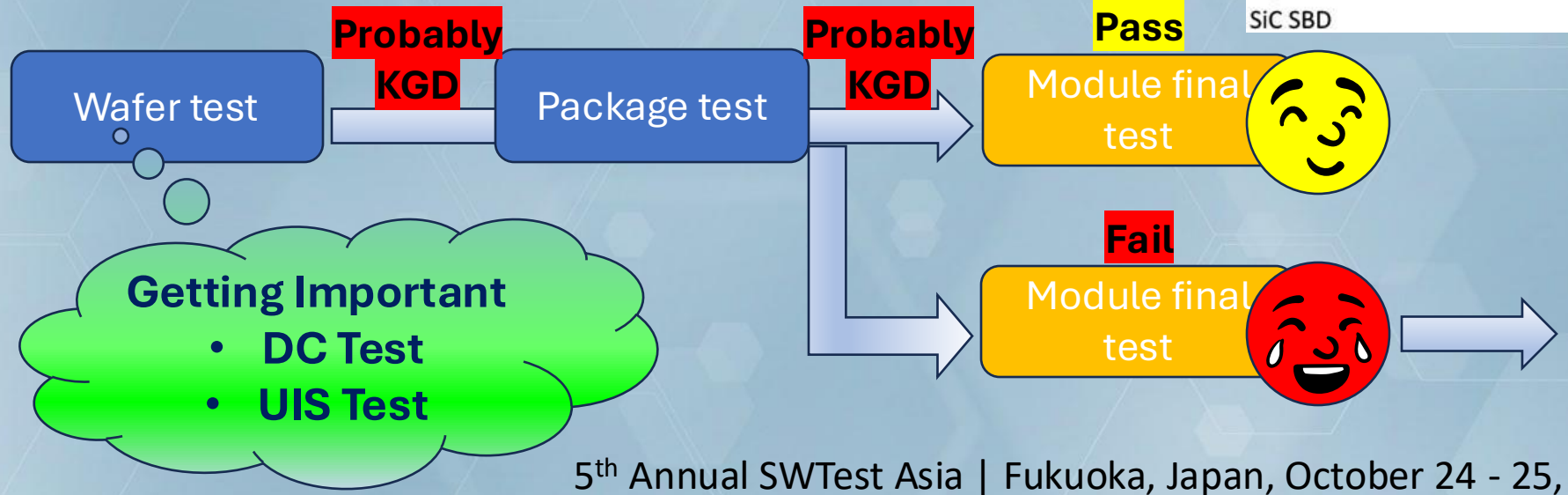
TESEC

Challenges in Wafer Testing from Viewpoint of Back-end Process







Waste

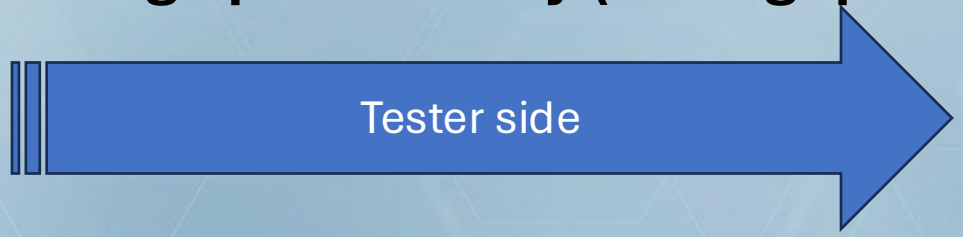
- **Time**
- **Module package**
- **Chip**
- **Wiring…**

Challenges in Wafer Testing from Viewpoint of Back-end Process

Challenge 2

To reduce the number of probing contact

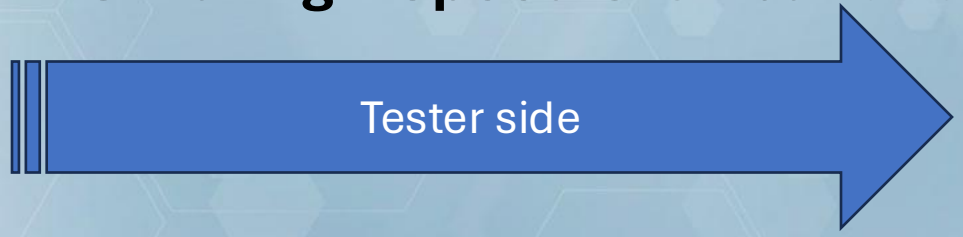
- **It can reduce pad damage risk or apply a small bonding area**
- **High productivity (throughput up)**



Challenge 3

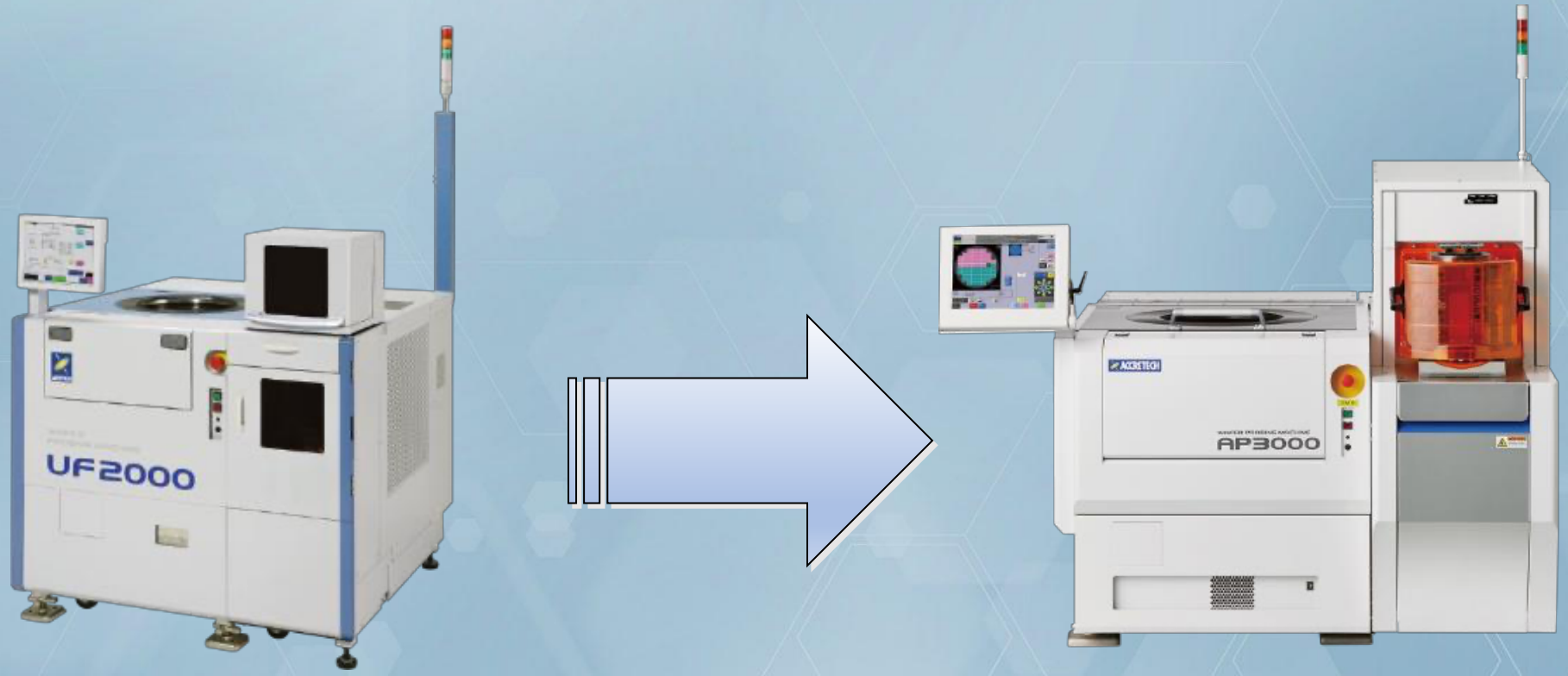
To avoid peripheral die damage during UIS

- **Ultra High-Speed Crowbar circuit < 1 us (During UIS test)**



Solution (Prober)

The power device test technologies are transferred from the experience of 200mm to 300mm prober

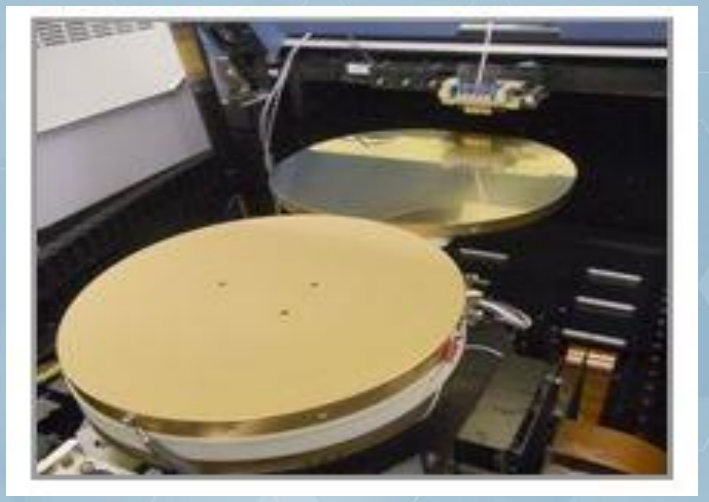


Solution (Prober)

DARUMA Chuck

Fast and stable measurement waveform detection is essential for high-current testing and UIS testing of power devices.
ACCT's prober has the following three features and is ideal for testing power devices. Details are explained on the next.

- **Make measurement path length constant**
- **Minimization of measurement path length**
- **Reduction of inductance(Low Ls)**

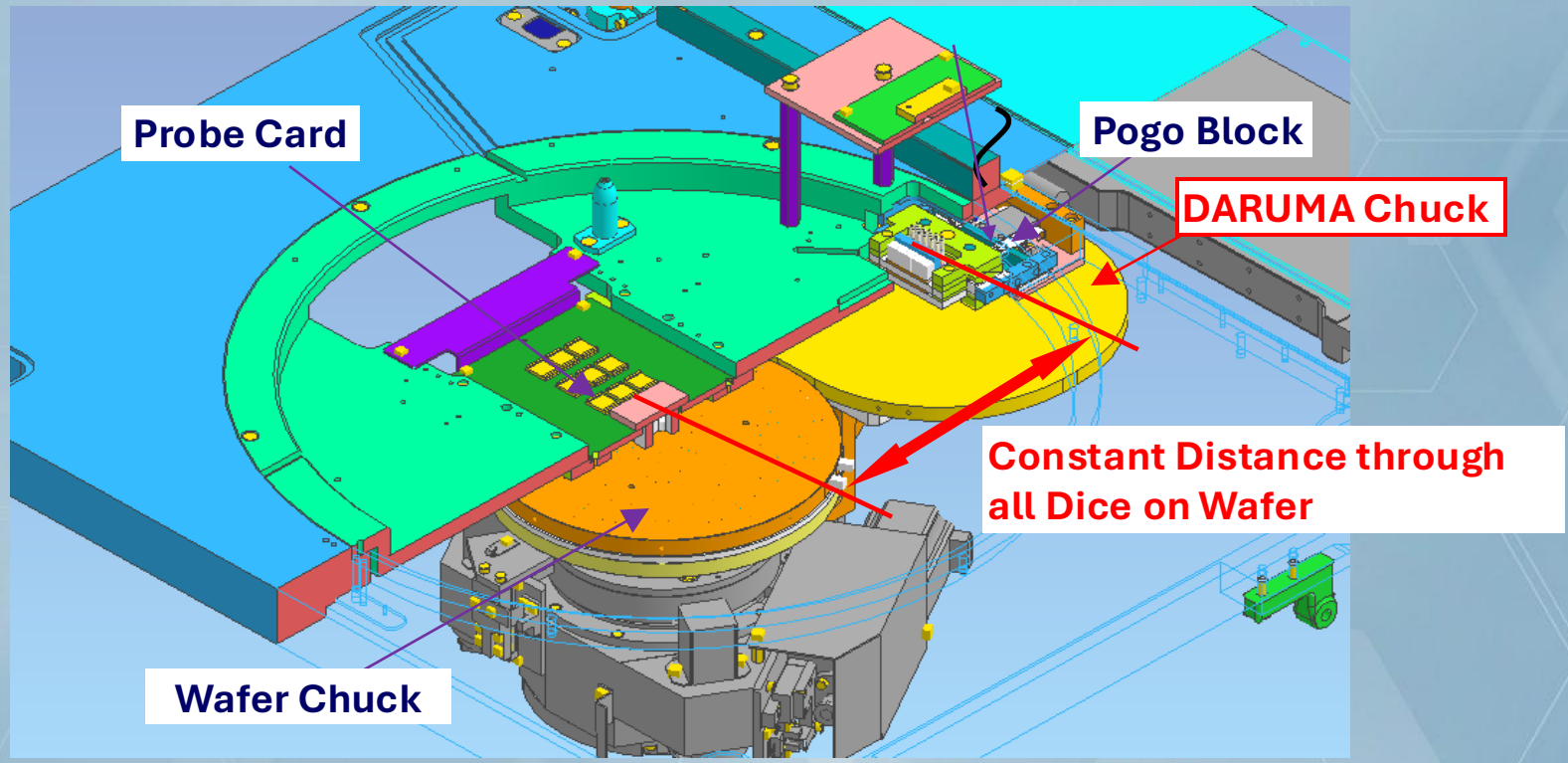


Solution (Prober)

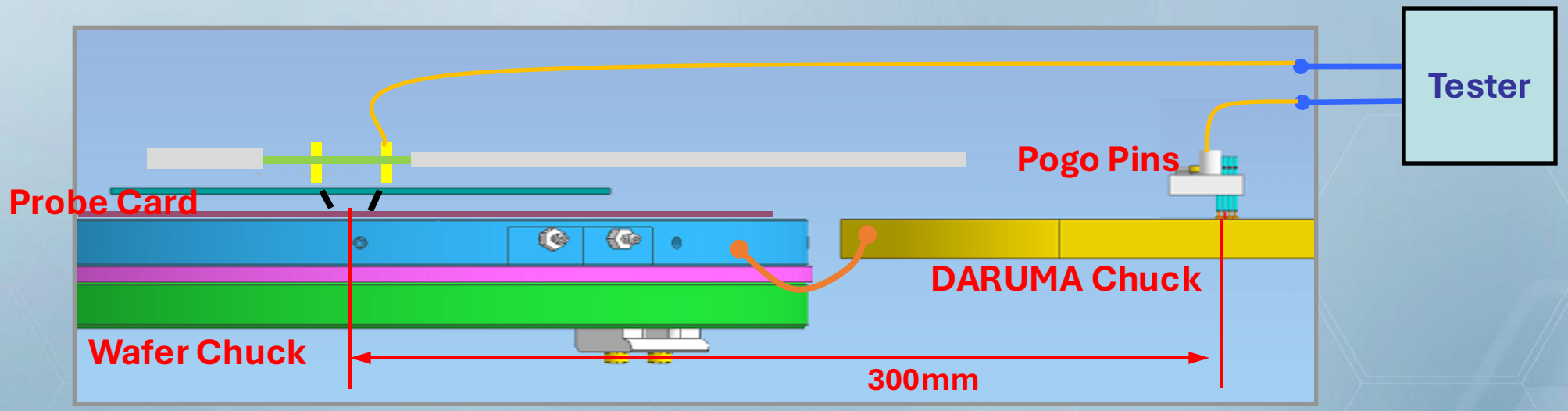
Accretech Patent

➢ Make measurement path length constant

Equipped with a DARUMA Chuck behind the wafer chuck and a pogo block for connecting the chuck electrode, the distance between the probe needle and the pogo block is always constant to equalize the inductance. This concept makes the current waveform stable within a wafer.

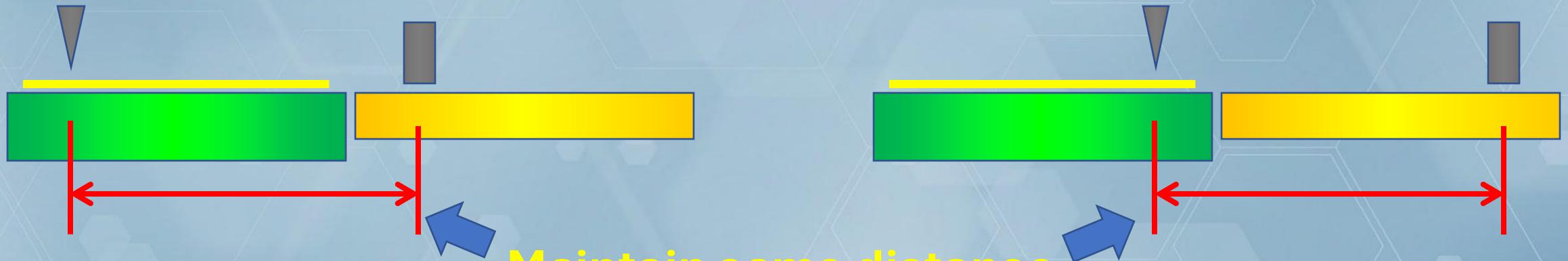


Solution (Prober)



@ Left side of wafer

@ Right side of wafer



Maintain same distance

Solution (Prober)

➢ Minimization of measurement path length

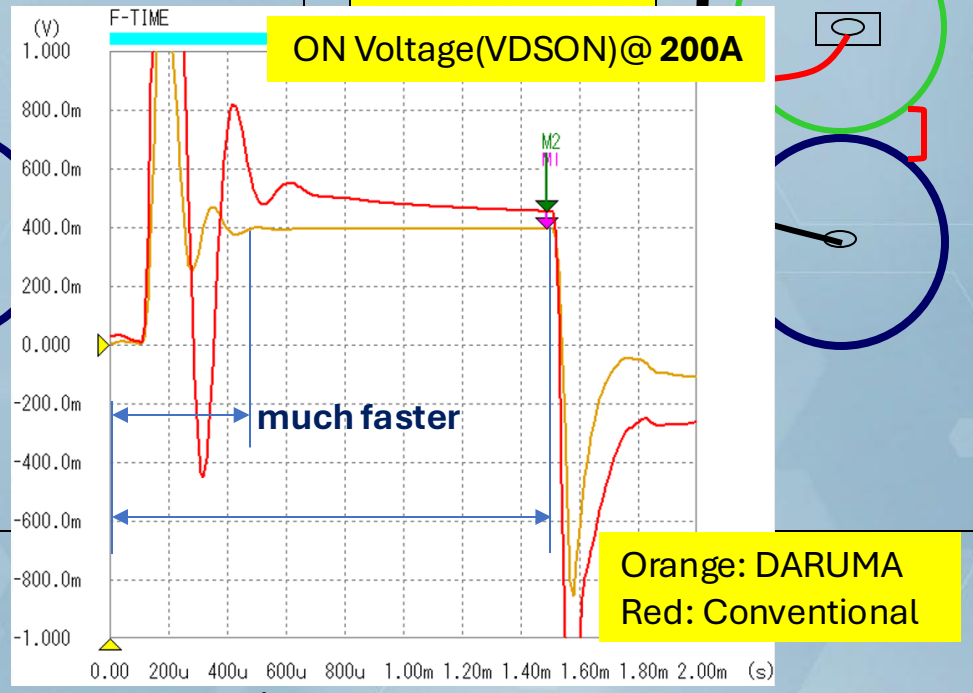
The chuck lead cable of DARUMA Chuck is very short compared to the conventional ones. Therefore, allowing for high speed testing when testing large currents and reducing the heat generated by the device.

Conventional

DARUMA Chuck

Test Head

Test Head

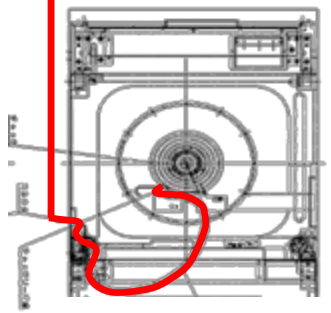


ON Voltage(VDSON)@ **200A**

much faster

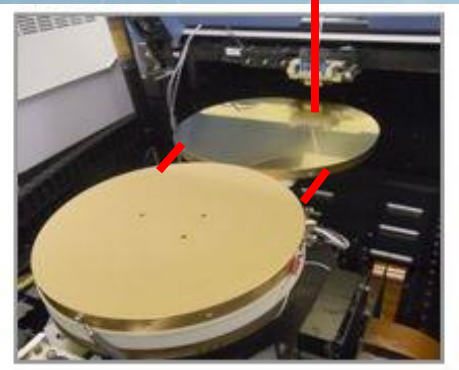
Orange: DARUMA
Red: Conventional

To Tester



Over 2.5m

To Tester

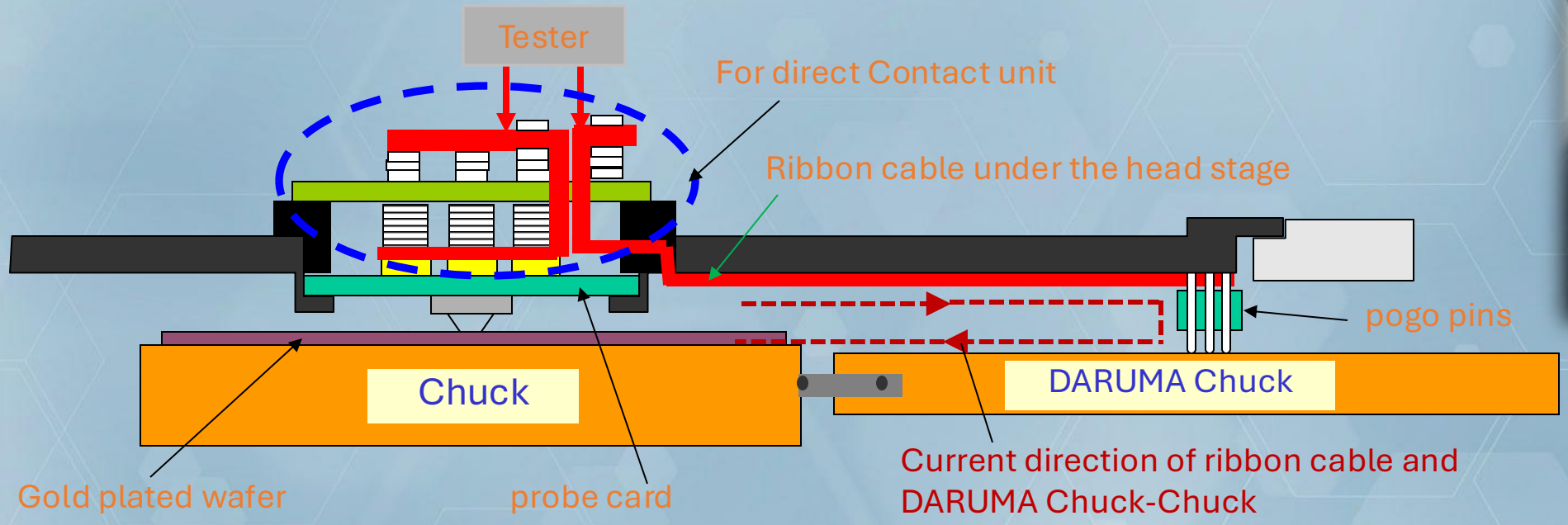


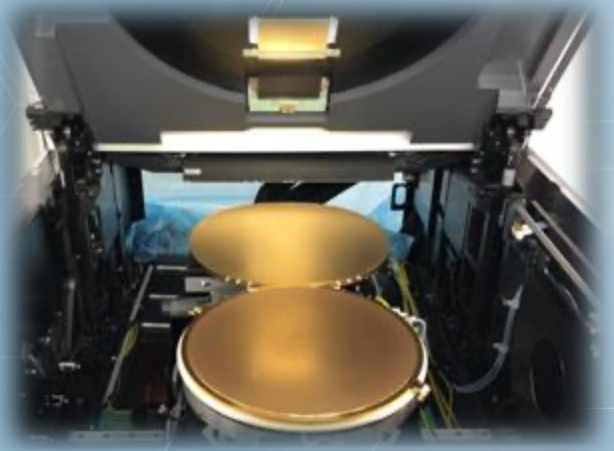
Solution (Prober)

➢ Reduction of inductance(Low Ls)

This is the structure of how to make low Ls.

- ➢ **Shorten the measurement path length by using a direct contact unit.**
- ➢ **Available no variation Ls during chuck move**
- ➢ **Bringing the opposing currents closer together cancels the magnetic field and reduces Ls.**

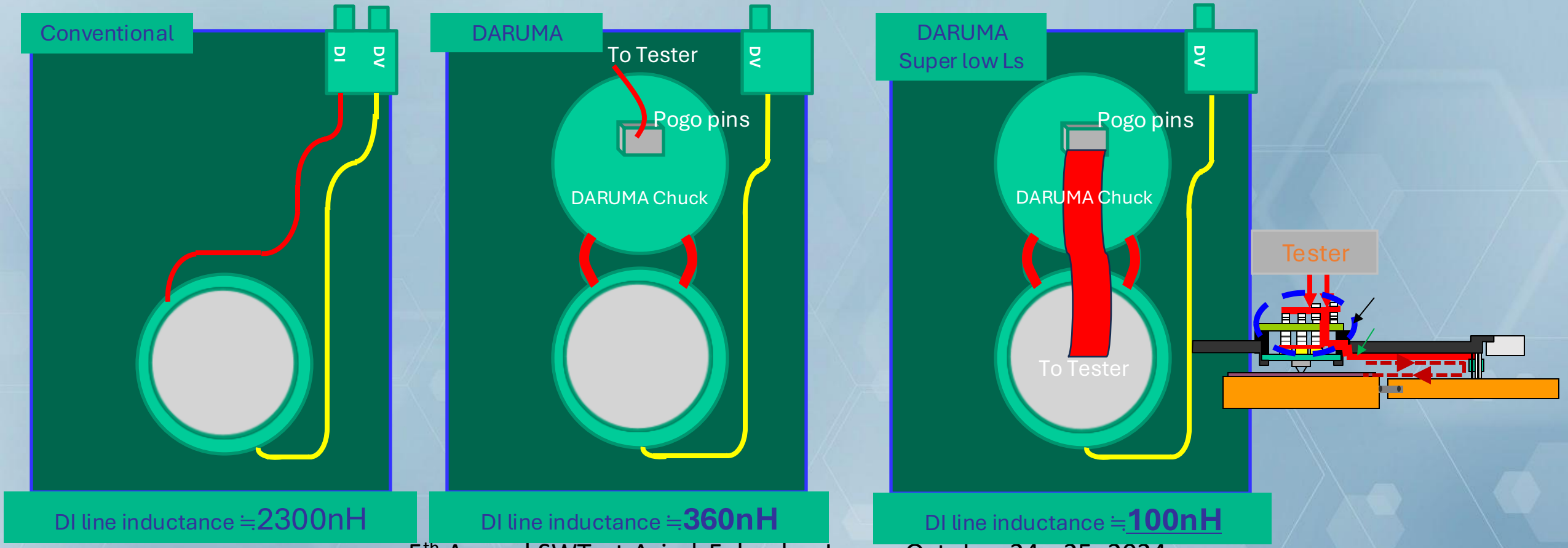




Solution (Prober)

Effectiveness of DARUMA Chuck

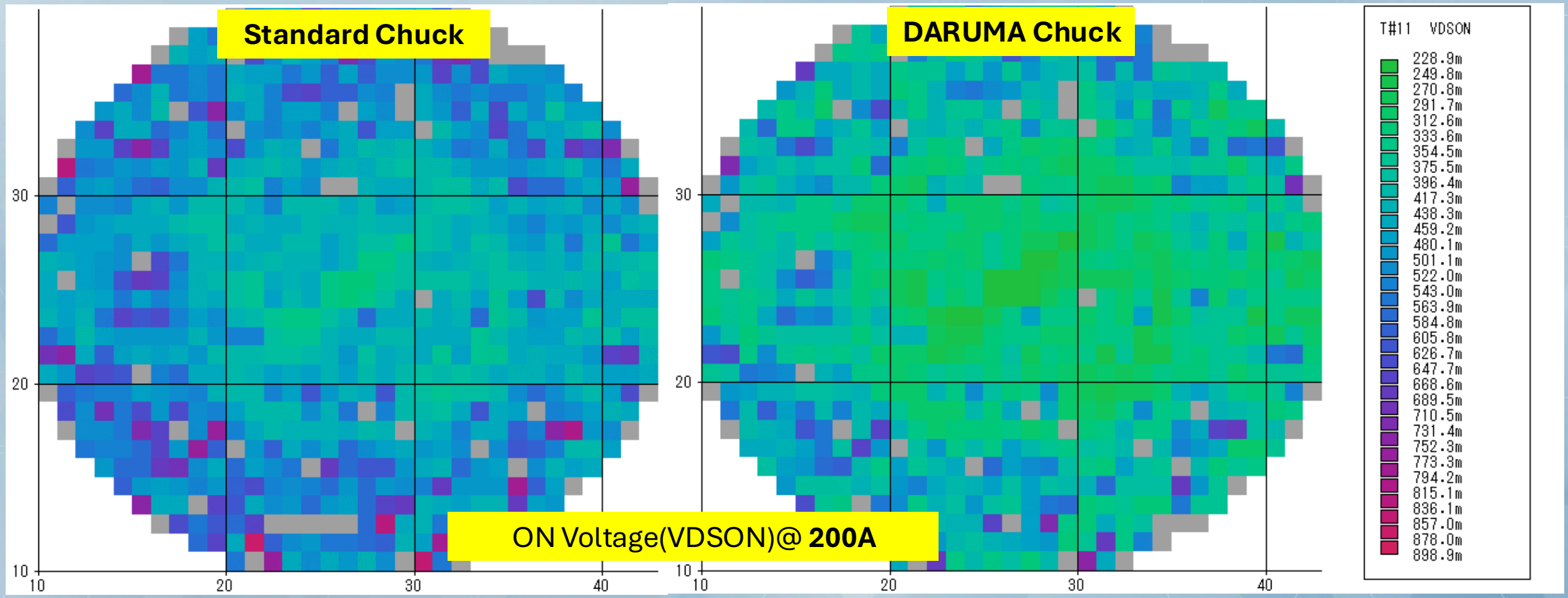
In the wiring method using DARUMA Chuck, inductance is greatly reduced, so the rise of current is fast, and the ON voltage detection response is also fast.



Solution (Prober)

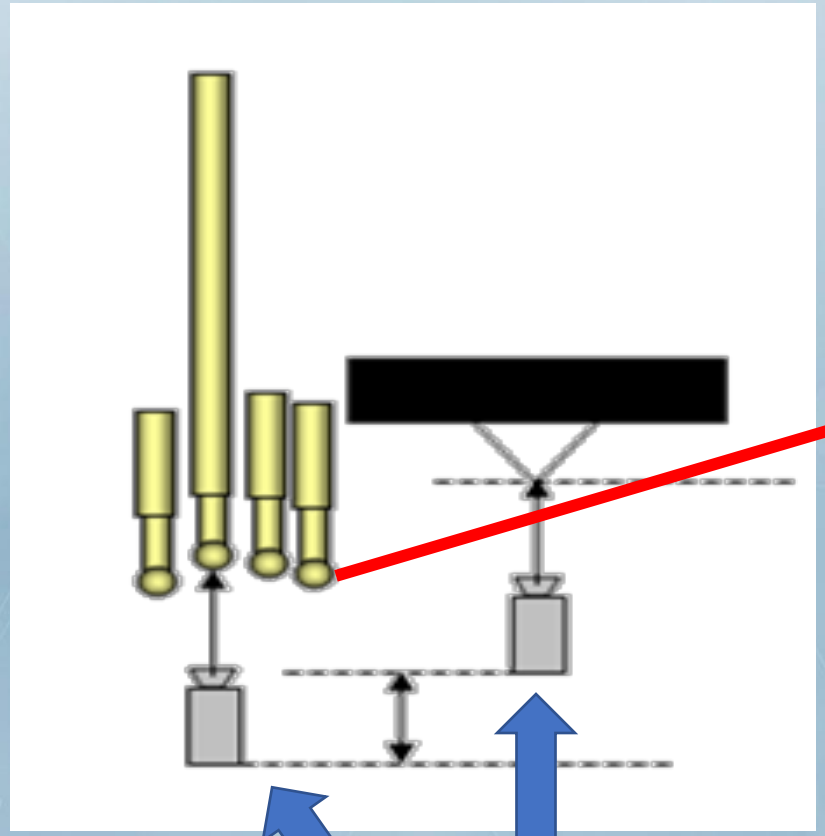
Differences in Wafer Mapping Between Standard Chuck and DARUMA Chuck

- **As a result, comparing the wafer maps of the on-voltage at the same measurement time shows that the improvement in settling speed of the waveform enables more accurate measurements.**

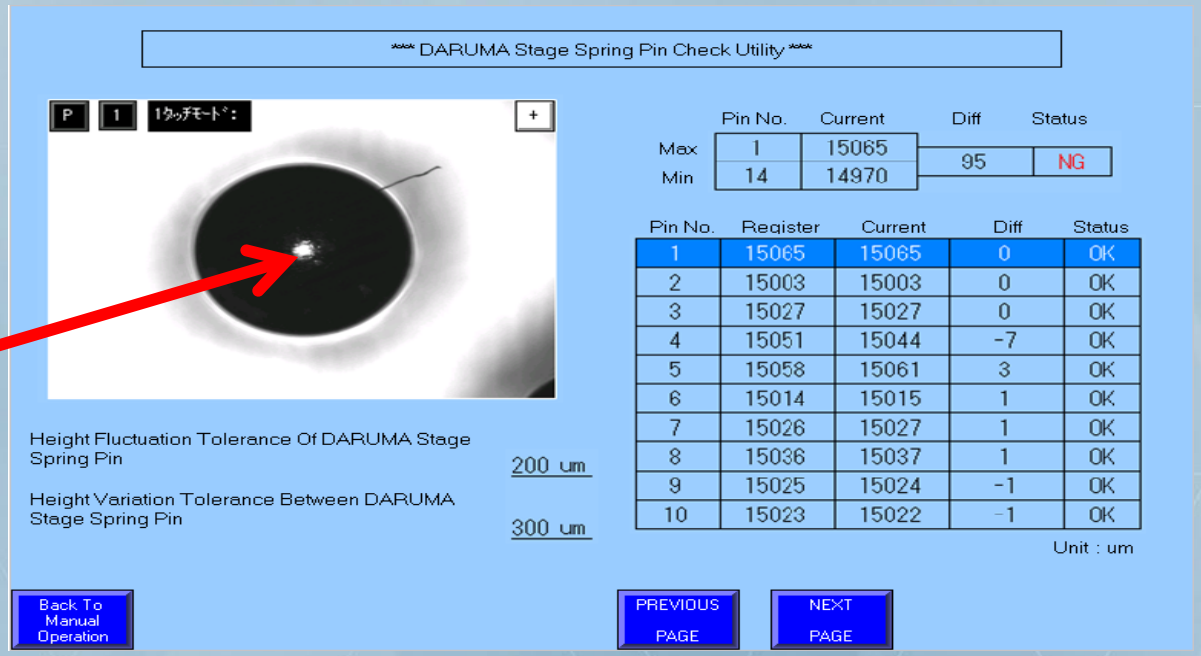


Solution (Prober)

Alignment for Pogo Pins



Probe Alignment Camera



Search pogo pin height and check the difference using the probe alignment camera. Then calculate the best overdrive point for contacting the DARUMA Chuck.

Solution (Prober)

Required periodical chuck top maintenance

Large current/Inductive load test >>> Deteriorating chuck top >>> Affect turn ON voltage/Contact resistance

- **It is easy to exchange the chuck top plate due to suction fixation.**
- **Re-construction of gold coating is available.**
- **Normal wafers and thin wafers with rims can be easily exchanged.**

Chuck can be replaced in 0.5 hours including calibration

Solution (Tester)

One Pass Direct Docking Test System

We have developed a test system that docks directly with the prober, enabling both DC and UIS testing with a single touchdown. This system has the following four features, making it ideal for power device testing.

- DC and UIS measurements can be made with a single contact
- Reduction of inductance by Direct Docking Unit
- Ultra High-Speed Crowbar circuit
- Simultaneous 4-chip measurement

Solution (Tester)

➢ DC and UIS measurements can be made with a single contact

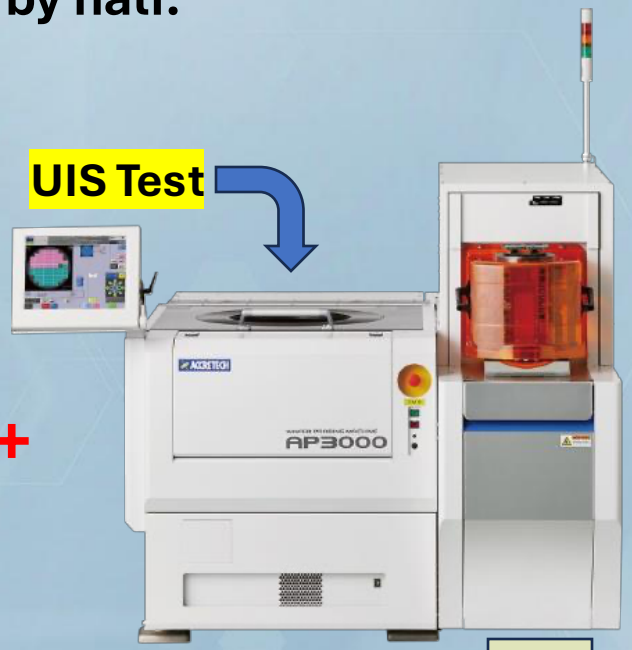
- **A switching mechanism between DC and UIS measurement is provided in the Direct Docking Unit.**
- **Probe marks are reduced by half.**

x 2 times

Probe mark

Wafer load/unload, wafer alignment, chuck indexing, etc...

+



Probe mark

Wafer load/unload, wafer alignment, chuck indexing, etc...

One Pass Test

Only one time

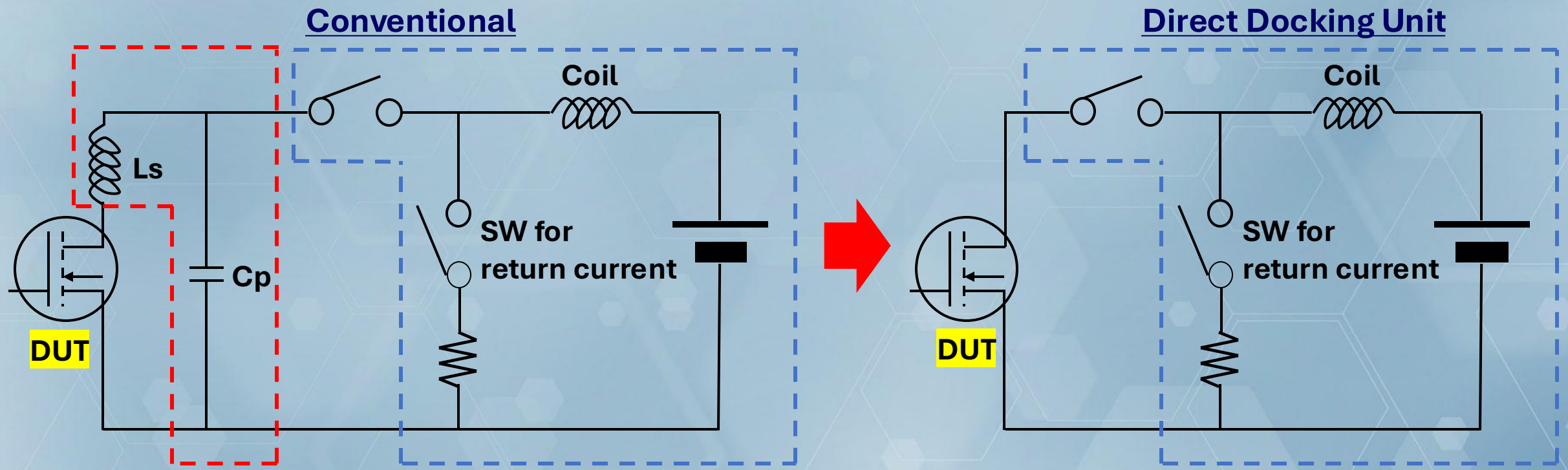
Probe mark

Wafer load/unload, wafer alignment, chuck indexing, etc...

Solution (Tester)

➢ Reduction of inductance by Direct Docking Unit

Direct docking of the tester and probe card shortens the distance between the measurement circuit and the DUT, reducing Ls and Cp. Furthermore, the UIS detection path in the direct docking unit is preferentially placed near the DUT, reducing the effects of Ls and Cp and improving the waveform quality of the UIS measurement.



Solution (Tester)

➢ Ultra High-Speed Crowbar circuit

This function operates when a defective chip is broken during UIS measurement.

Without Crowbar Circuit function

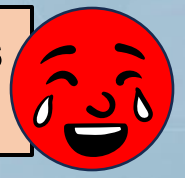
Defective chip broken during UIS measurement

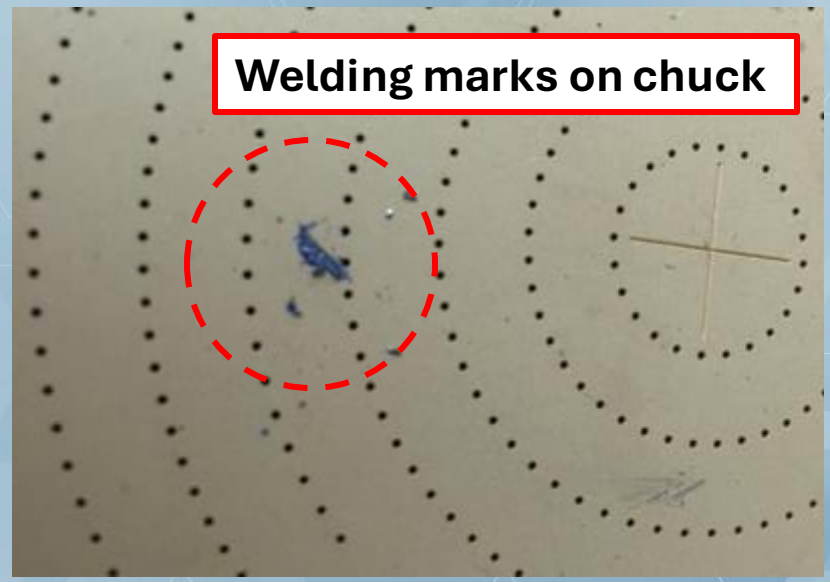
↓

Inductive energy of the coil is released to the surrounding chips

↓

- **Destruction of peripheral chips**
- **Wafer and chuck welding**





Solution (Tester)

➢ Ultra High-Speed Crowbar circuit

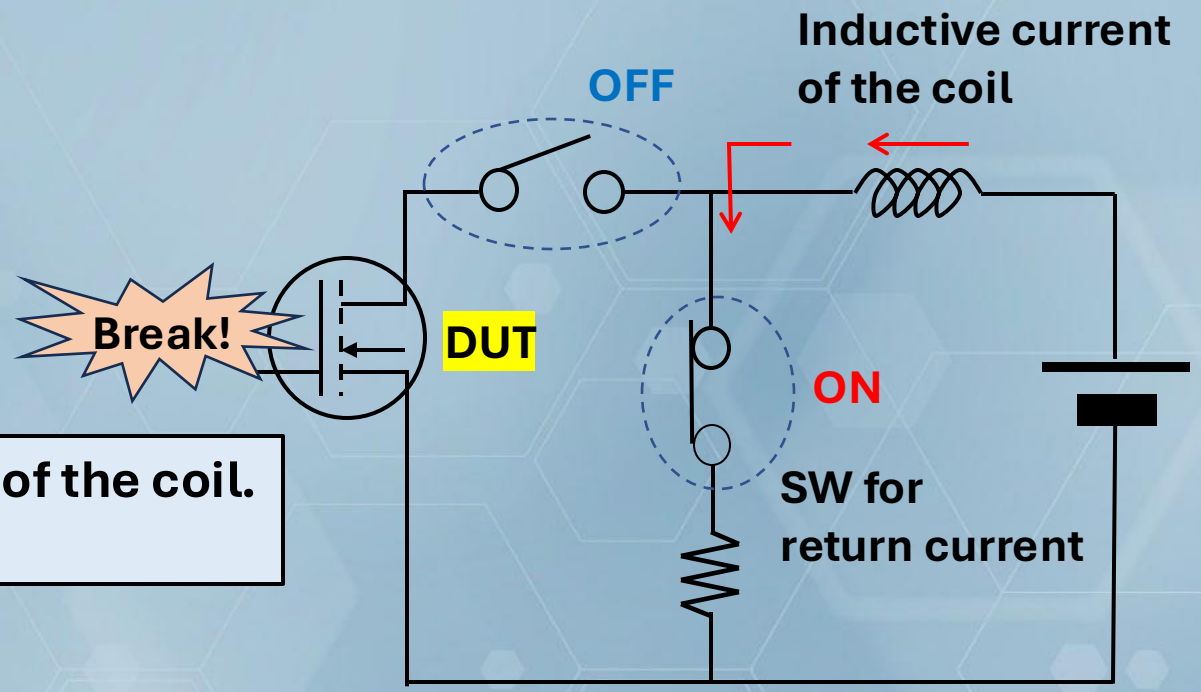
With Crowbar Circuit function

Defective chip broken during UIS measurement

Detect a broken chip

Turns on the path that returns the inductive current of the coil. At the same time, the DUT path is shut down.

- **Wafer Safety**
- **No destruction of peripheral chips**
- **No welding of wafer and chuck**

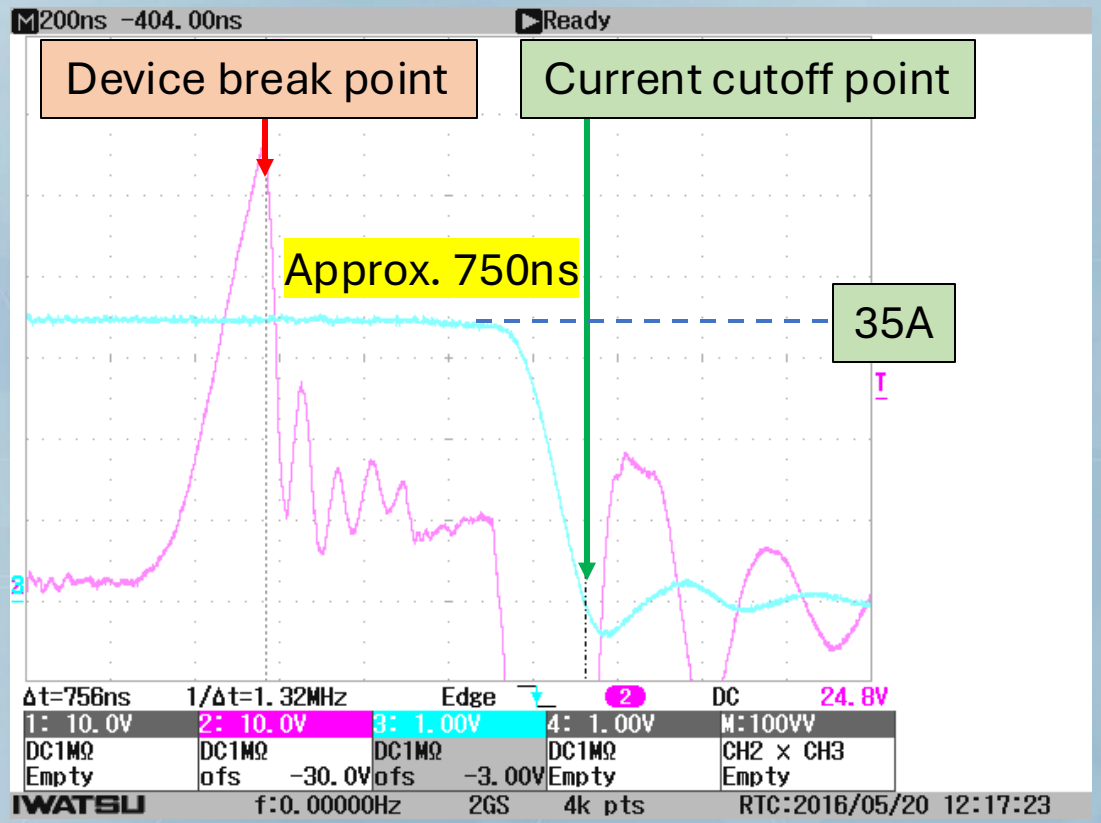


Solution (Tester)

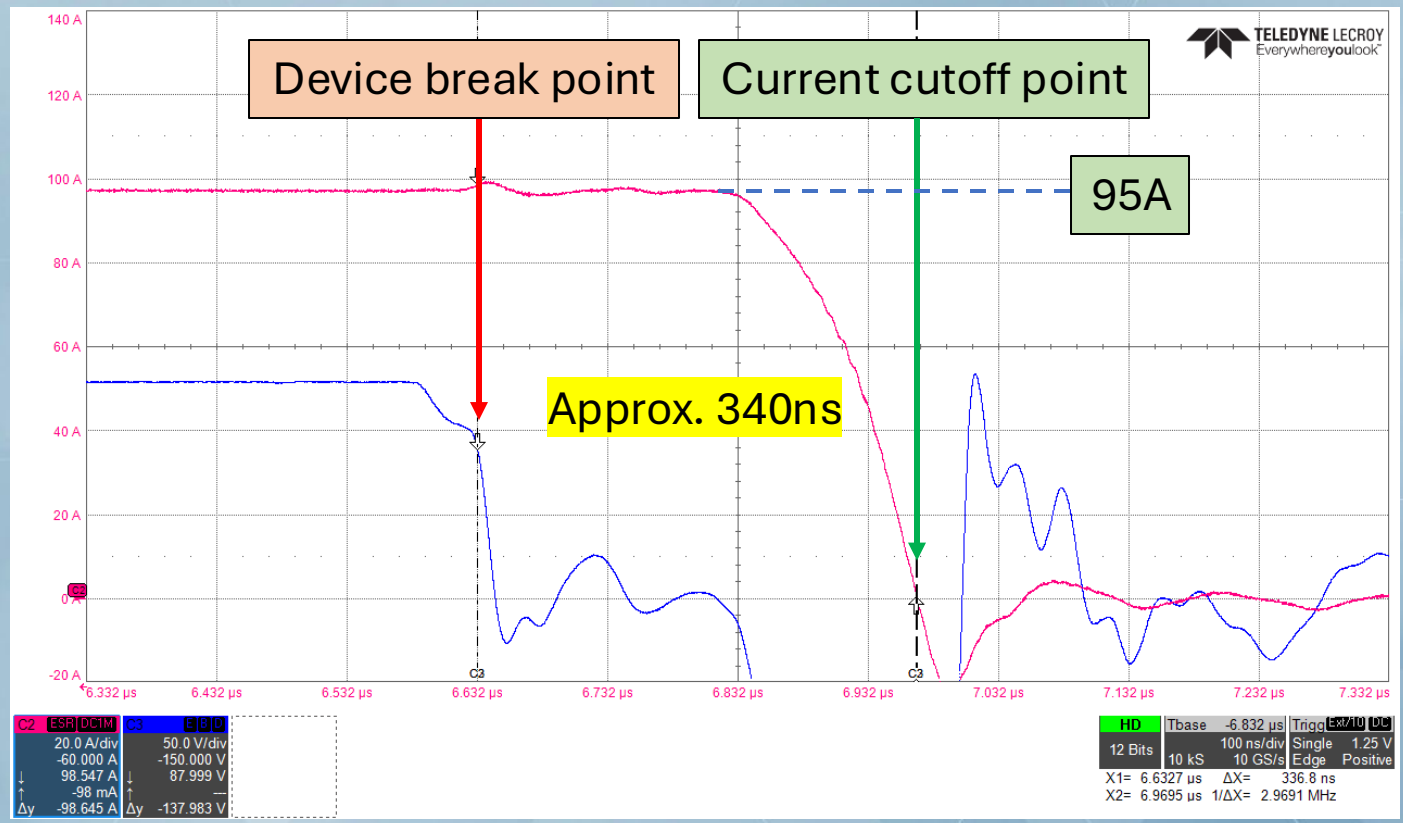
➢ Ultra High-Speed Crowbar circuit

By changing the shutdown device from Si-IGBT to SiC-MOSFET, the time from chip broken failure to current interruption has been reduced by 50% compared to the conventional method.

Conventional (Si-IGBT)



Ultra High-Speed Crowbar circuit (SiC-MOSFET)



Solution (Tester)

➢ Simultaneous 4-chip measurement

To cope with the increase in the number of chips due to larger diameter wafers (which increases inspection time), DC measurement supports simultaneous 4-chip measurement (in some cases, 1-chip measurement), which improves production efficiency by approximately 4 times compared to 1-chip measurement.

Example test sequence

CHIP#	DC test	DC test	High current DC test				DC test	UIS				DC test
1												
2												
3												
4												

4 Parallel 4 Parallel ⟷ Serial test ⟷ 4 Parallel ⟷ Serial test ⟷ 4 Parallel

Conclusion

“Challenges in Wafer Testing” from Viewpoint of Back-end Process

Perfect inspection of the device on Wafer

- **Challenge 1 : Accurate screening tests**
  - UIS measurement on wafer
  - Reduction of inductance by DARUMA Chuck and Direct Docking Unit
- **Challenge 2 : Reduce the number of probing contact**
  - One Pass system of DC and UIS measurement requires only one probing contact
- **Challenge 3 : Avoid peripheral die damage during UIS**
  - Ultra High-Speed Crowbar circuit < 1 us (During UIS test)

Acknowledgements

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We hope these efforts bring further development of products that will contribute to societal advancements.

Thank you