Cleaning Innovations to Maximize OEE for High Volume Memory Test

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Overview

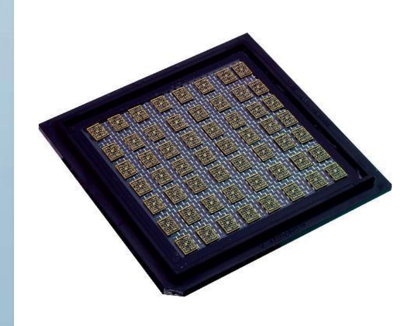
- Gel-Pak and JEM Corporate Snapshots
- Background and Motivation
- Material Design
- Proof of Concept
- Testing and Results
- Summary / Conclusion
- Next Steps

Innovative Solutions that Drive OEE

Three ISO 9001-2015 Certified Manufacturing Facilities:

- Over 95,000 square feet of Materials Manufacturing
- ISO Class 10,000 Cleanrooms
- ISO Class 7 Cleanrooms
- Over 200 Employees
- Global Sales and Applications Support Network

SMALL DIE SHIPPING & HANDLING



Vacuum Release (VR) Carriers

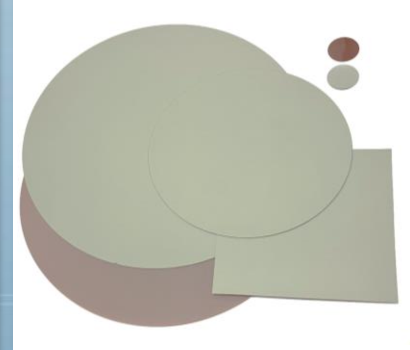
- Automated pick & place applications for bare die and devices ranging from <250 micron to 75mm in size.
- **Suitable for transport and handling MEMs Probes**

TEXTURED CARRIER PRODUCTS

Textured Device Carrier Products

- **Universal Fixture for device handling in-process, singulated die testing, and shipping.**

ELASTOMER PROBE CARD CLEANING FILMS



Gel-Probe Card Cleaning

- Custom coating of highly engineered elastomer films for semiconductor applications.
- **Customizable probecard cleaning wafer and cleaning sheet applications.**

40-Years of Materials Expertise

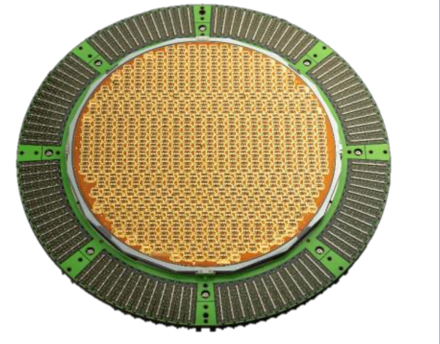
Japan Electronic Materials

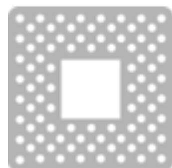
JEM
JAPAN ELECTRONIC MATERIALS

- **Since 1970, JEM has contributed to the growth and development of the global semiconductor industry.**
  - 4 sites in Japan, 6-sites throughout Asia, 1-site in US, and 1-site in EU
- **Key supplier of Advanced MEMs Type Probe cards for Memory and Logic Device Testing**

MC Series - MEMS Micro Cantilever Type for Memory Test

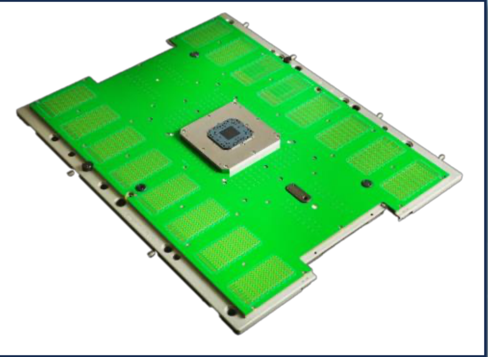
- *High-parallelism testing and fine-pitch pads*
- *High density memory, DRAM, NAND, and Flash*





MT Series - Vertical MEMS Type for Fine-Pitch Area Array

- *High-parallelism testing and fine-pitch pads and Cu pillars.*
- *Area array, Logic Devices, and MPU / AP*



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Mission of Wafer Test | Critical Data

Image Source: Verigy

- Provide Feedback to FAB for Wafer Manufacturing
- Provide Performance Data to Improve Design
- Categorize Devices based on performance
- Maintain High Yields during high volume testing
- Facilitate High Density Multi-Die with "KGD" Solutions
- Reduce Costs of Yield Loss at Final Test

Test Provides Metrology For Entire Semiconductor Value Chain

Source: SWTest Asia 2019 – Ozawa Keynote

Data Quality Attained with Probe Cleaning

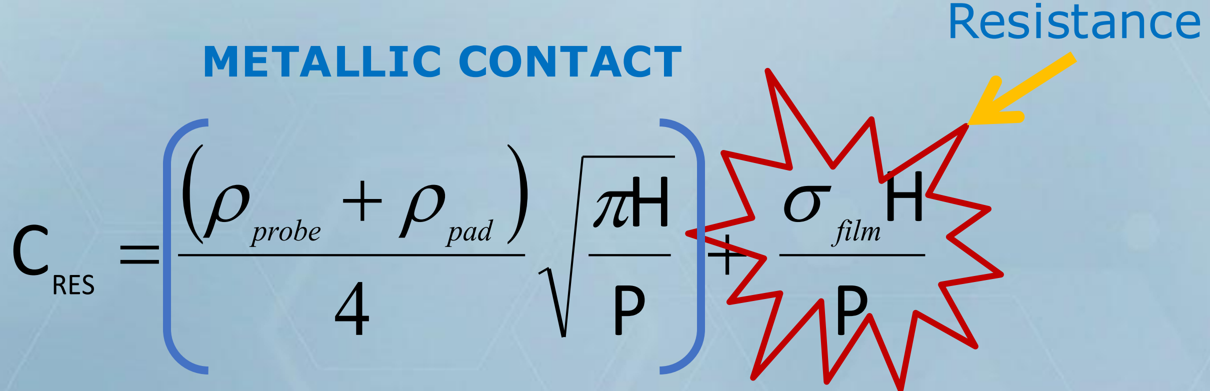
OEE Loss Occurs during Continuous Probing without a Cleaning Process

Efficient Probe Cleaning:

- **Improves test accuracy**: Removes debris, oxides, residuals, etc., that affect test program performance.
- **Prolongs probe card life**: Consistent cleaning maintains performance and reduces offline repair.
- **Reduces risk of contamination**: Prevents probe-related debris from dropping onto the wafer and affecting subsequent processing steps.
- **Increases prober availability**: Assures accurate probe-to-pad-alignment (PTPA) critical for small tips, small device I/Os, fine pitches, and large contactors.

Cleaning Challenge | CRES & Lifetime

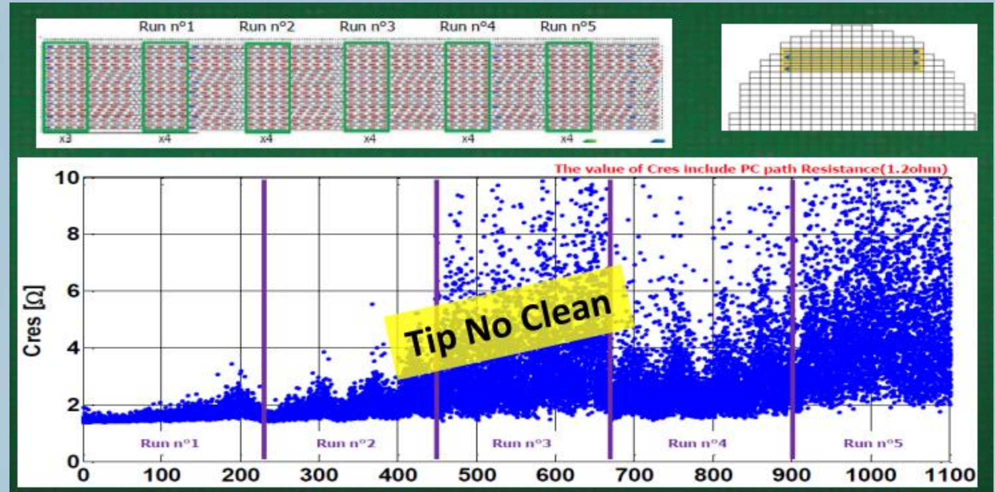
- **Probes touch the DUT, but the Current Might NOT Flow !**
- **Probe cleaning is a "dirty business" and critical for controlling contact.**

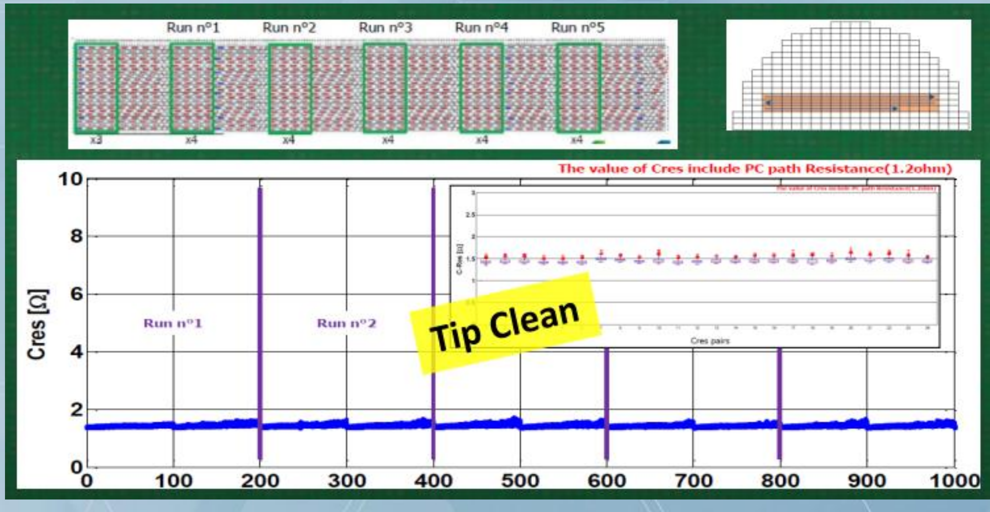


$$C_{RES} = \left(\frac{(\rho_{probe} + \rho_{pad})}{4} \sqrt{\frac{\pi H}{P}} \right) + \frac{\sigma_{film} H}{P}$$

- ρ_{pad}, ρ_{probe}, σ_{film} = resistivity values
- H = hardness of the pads, bumps, pillars, etc.
- P = contact pressure applied by probe

Implement efficient cleaning
to ensure continuously reliable electrical contact.

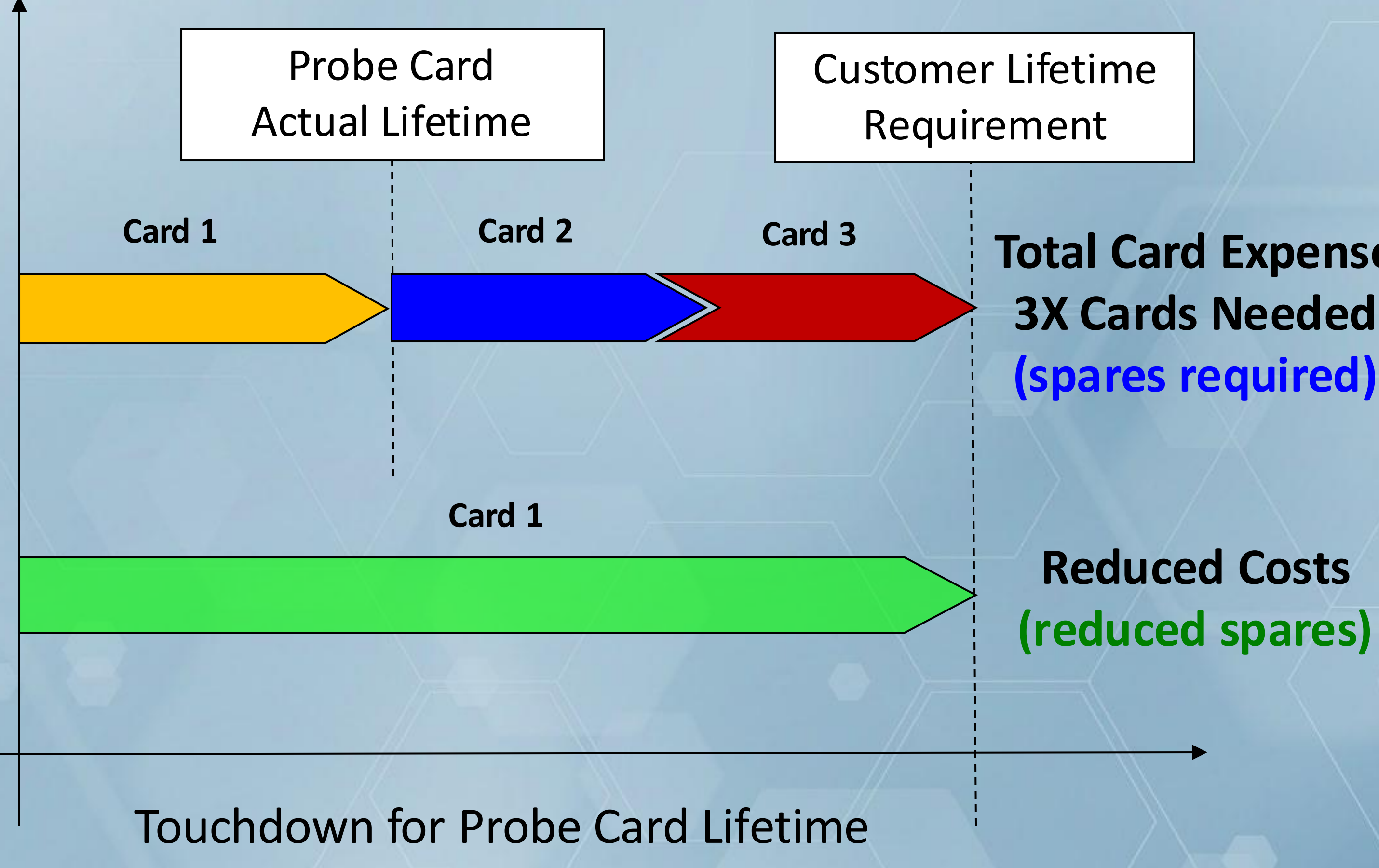




Source: R. Vallauri, D. Perego, M. Prea, J. Kim, and J. Yun, SWTest 2017

Poor Cleaning = High Test Costs !

- Cleaning can consume more **95%** of a probe card lifetime.
- With aggressive cleaning test costs increase.



Source: J. Broz, SWTest 2007

High Volume Probers for Improved OEE

Multi Test-Cell Systems

- Accommodate large array and full wafer testing.
- Handle multiple probe cards
- Can handle multiple cleaning wafers with execution steps to maintain probe card life-time

Probe Card Cleaning Challenges

- Probe card technology + cleaning material tracking is critical.
- One material may be fully utilized before the other.
- Loading & unloading multiple cleaning wafers can reduce OEE.

TEL Cellcia Modular Prober

Minimizing Number of Cleaning Materials Can Improve OEE

Sources: Accretech and TEL websites

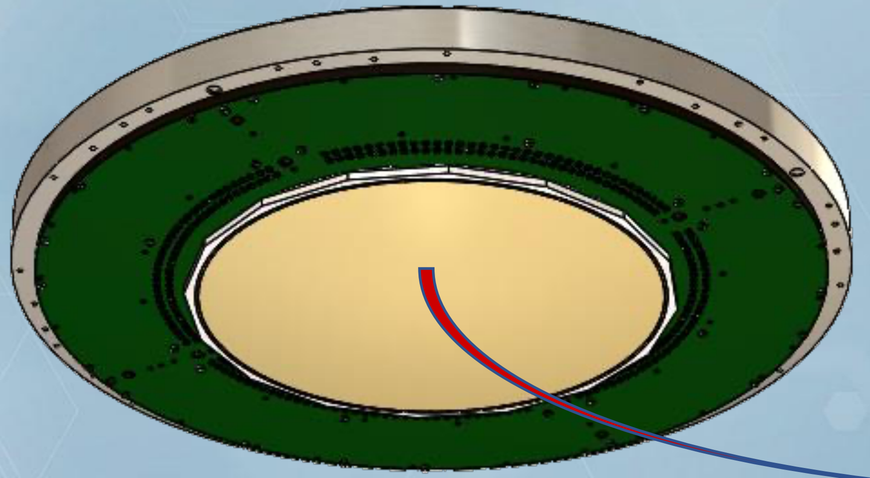
One Touch Memory Probe Cards for Improved OEE

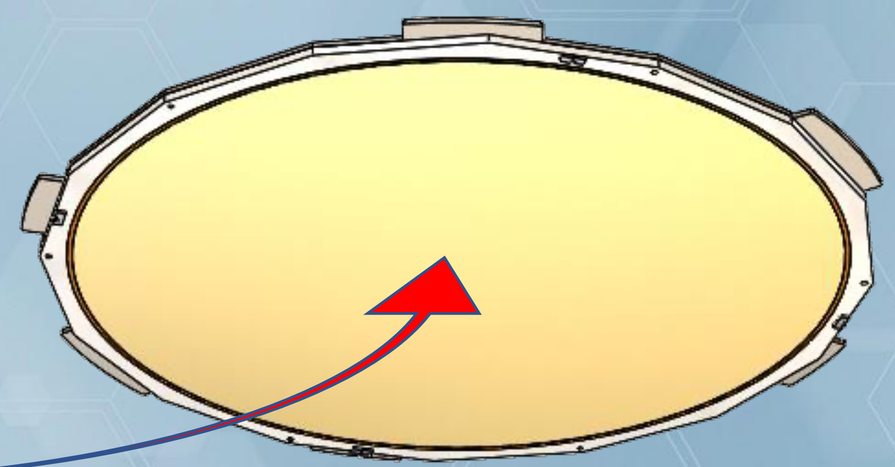
JEM MC Series MEMS Micro-Cantilevered

- Fine Pitch and High Pin count
- High Density with MEMS Technology
- High Speed Application
- More Design & Production Capacity
- Mounted onto PCB & Stiffener

JEM ML Series MEMS Micro-Cantilevered

- Fine Pitch and High Pin count
- High Density with MEMS Technology
- Specifically designed for Multi Probing System
- Simple structure without PCB and IC-pin
- Lighter weight due to lighter stiffener, easy to handle

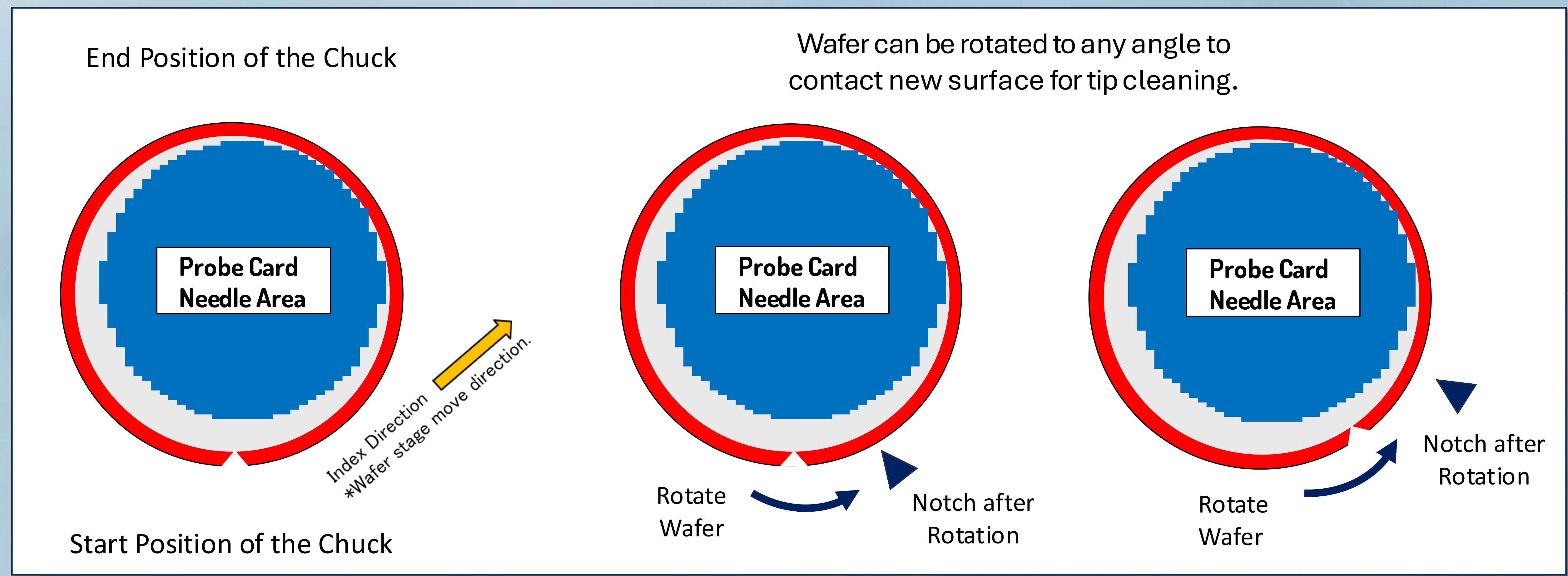




Ideal cleaning material must address advanced probe card technologies

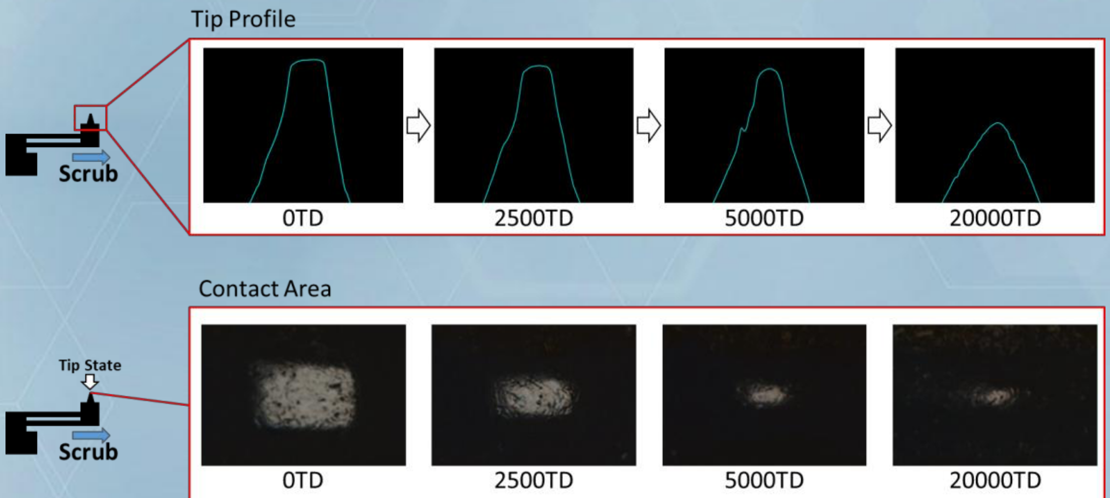
Cleaning a Full Wafer Contactor

- Cleaning wafers stored within the prober are required for single wafer probe card technologies.
- Stepping and indexing during cleaning execution is critical for optimal probe tip maintenance.

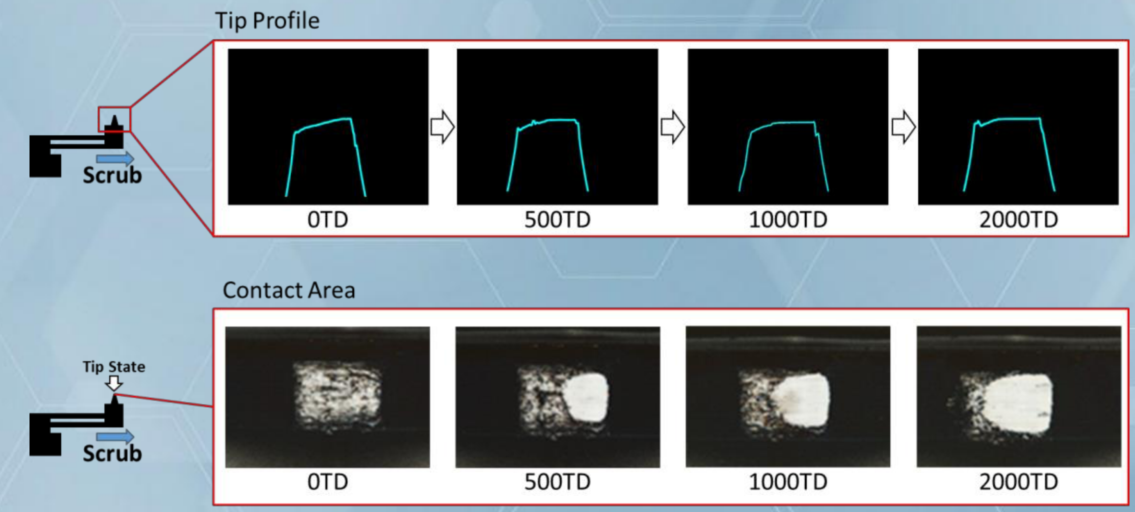


Current Cleaning Strategies

- ## Gel-Probe Refine-H3 Cleaning Wafer
  - Abrasive loaded elastomer for online cleaning.
  - Effective for debris removal and tip cleaning
  - Overall, low wear rate for long lifetime
  - Difficult to maintain overall probe tip shape



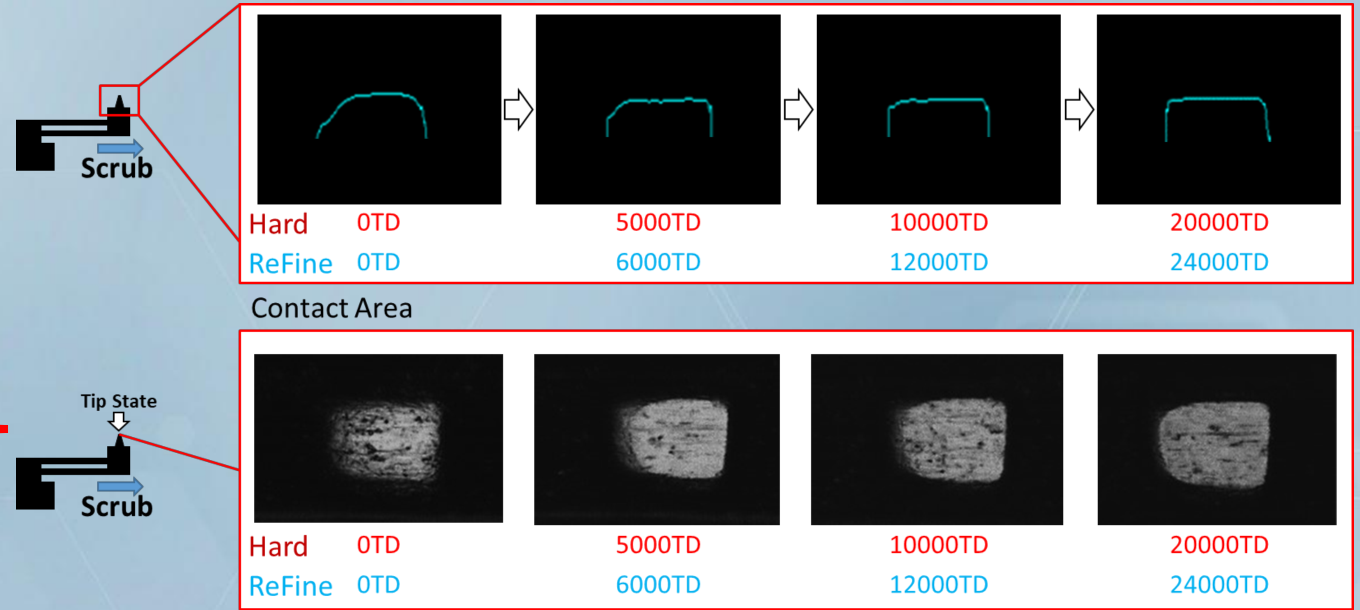
- ## Textured silicon cleaning wafer
  - Hard cleaning wafer
  - Effective for probe tip texture and maintaining a flat tip
  - Overall, high wear rate for short lifetime
  - Tip size becomes too large.



Combination Cleaning Process

Multiple cleaning wafers required

- Wafer Test (Contact on Al Pad)
- Unload Device Wafer
- Load Cleaning Wafer-1
- Needle alignment
- Cleaning Execution
- Unload Cleaning Wafer-1
- Load Cleaning Wafer-2
- Needle alignment
- Cleaning
- Unload Cleaning Wafer-2
- Load Device Wafer
- Wafer Test Resumes



- **Dual Wafer Cleaning**
  - Tip shape and size are well-maintained
  - Effective for debris removal and tip cleaning
  - Effective for probe tip texture and maintaining a flat tip

Optimizing the Cleaning Process

Multiple cleaning wafers required

Wafer Test (Contact on Al Pad) → Unload Device Wafer → Load Cleaning Wafer-1 → Needle alignment → Cleaning Execution → Unload Cleaning Wafer-1 → Load Cleaning Wafer-2 → Needle alignment → Cleaning → Unload Cleaning Wafer-2 → Load Device Wafer → Wafer Test Resumes

Combination Clean Wafer Cycle will Impact OEE and Cost of Test

- 2 x load/unload cleaning wafer
- 2 x needle alignment
- Approx. 15 minutes

Single Clean Wafer Cycle

- 1 x load/unload cleaning wafer
- 1 x needle alignment
- Less than 5 minutes

Single Wafer

Wafer Test (Contact on Al Pad) → Unload Device Wafer → Load Cleaning Wafer-1 → Needle alignment → Cleaning Execution → Unload Cleaning Wafer-1 → Wafer Test Resumes

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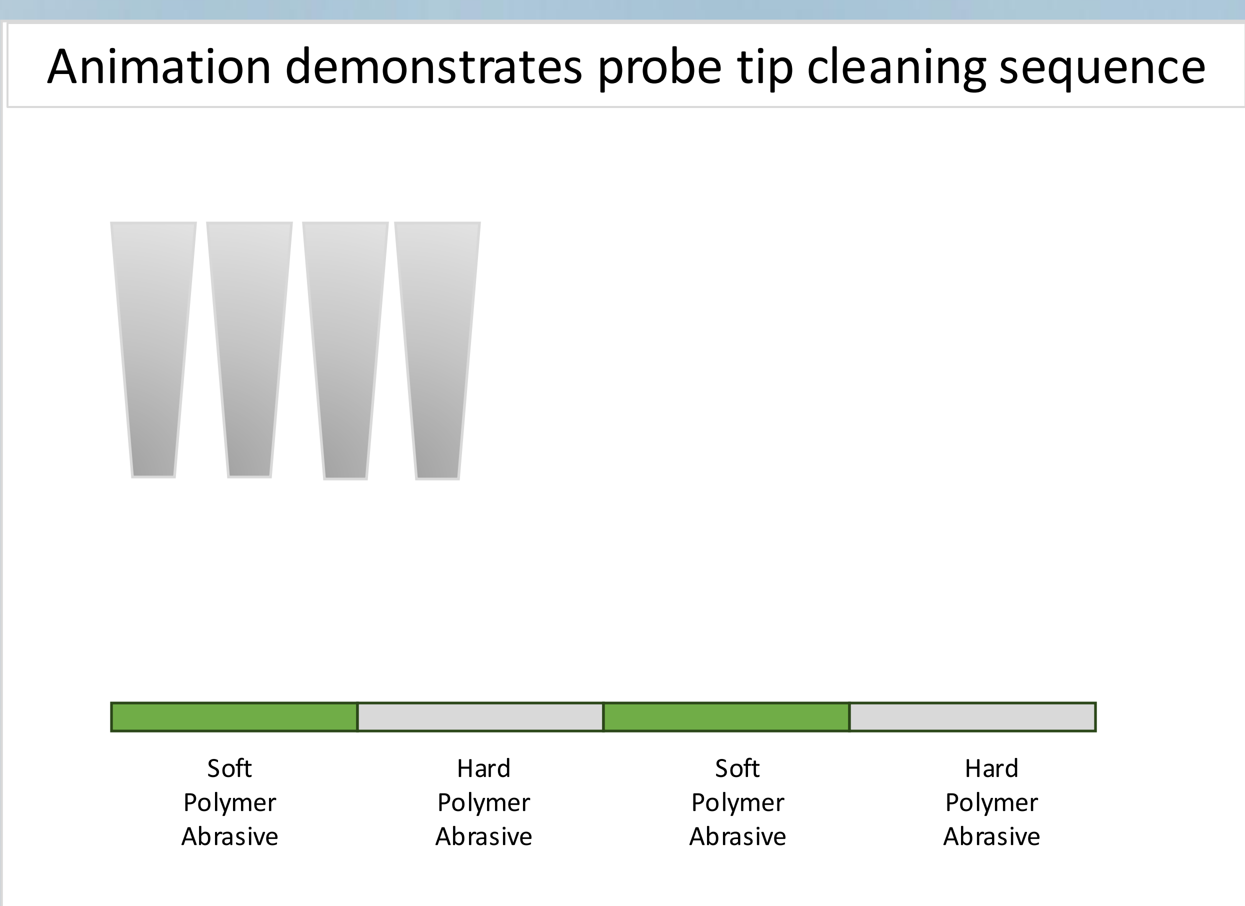
Challenge | Multizone Cleaning Material

Goal:

Eliminate the need for a multiple-cleaning-wafer strategy for full wafer contact probe cards to improve OEE.

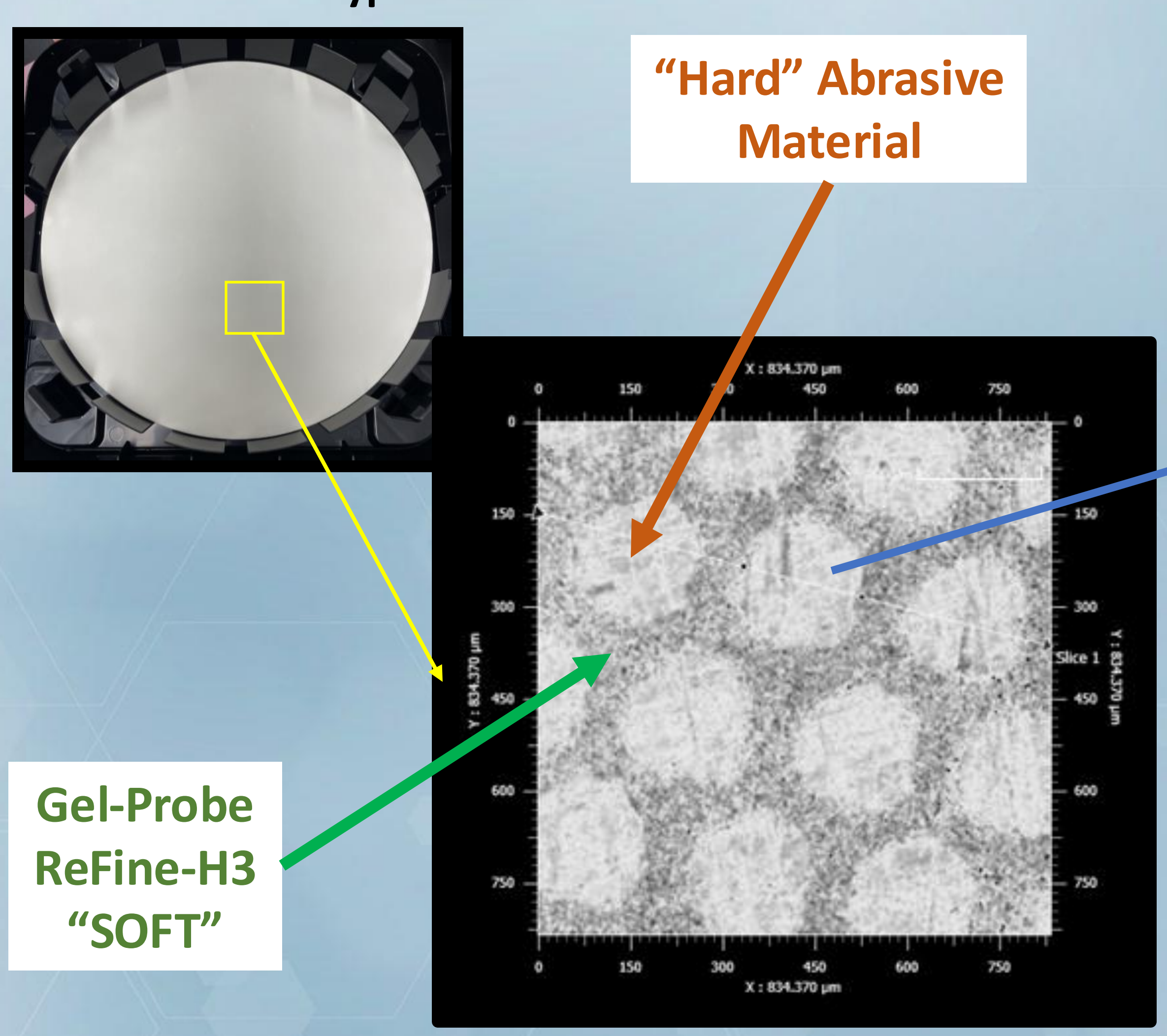


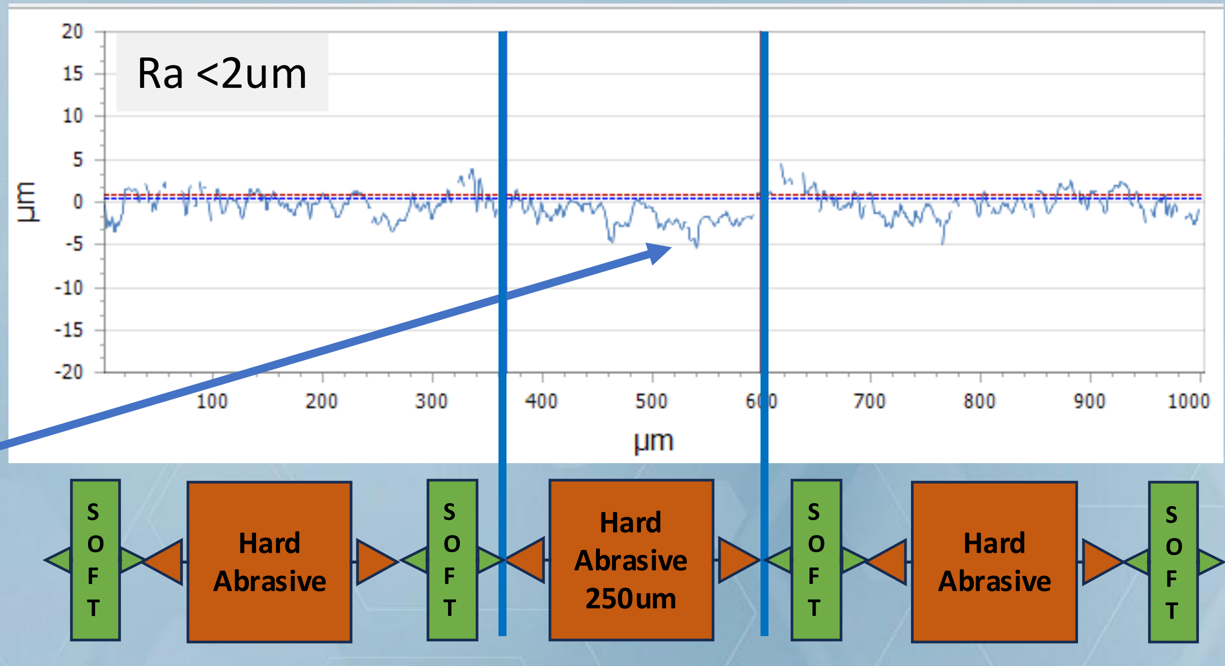
Critical Design Requirements:

1. Zones of hard and soft polymer are planar with a low variability (Rt, peak-to-valley) and TTV.
2. Probe-tips will contact both hard and soft abrasive polymer zones during cleaning cycle indexing.
3. All zones across the cleaning wafer are thermally stable.
4. Zone size, location, and material type are customizable.

Patent Pending

Surface Morphology





✓Design Requirement:

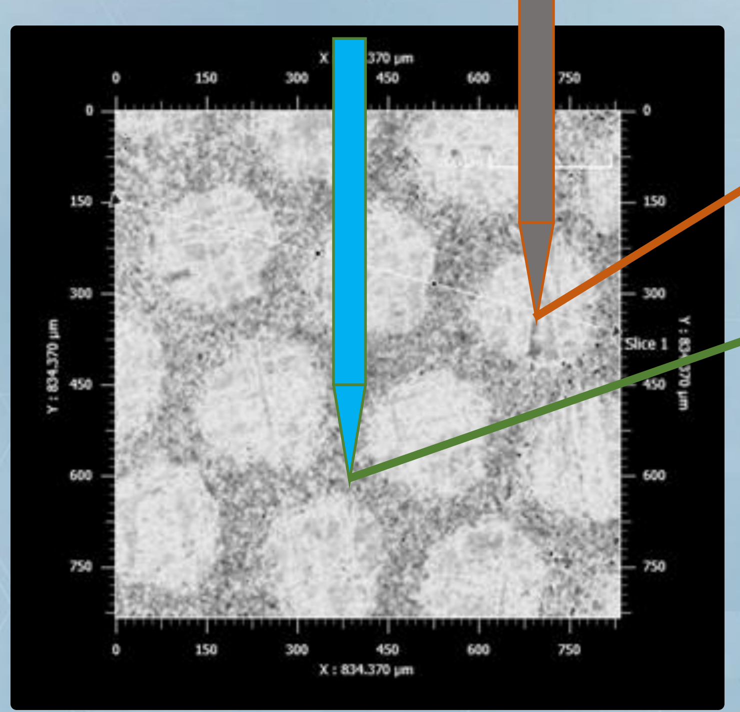
Polymer abrasive and shaping materials are flat and planar at the surface with a low TTV and controlled surface roughness.

Patent Pending

Insertion Hardness (Force vs. OT)

✓Design Requirement:

Probe-tips will contact both hard and soft abrasive polymer zones during cleaning cycle indexing.



Force (gf) vs. Overdrive (um)

Hard Abrasive

Gel-Probe
ReFine-H3

Probe Force (gram)

Overdrive (um)

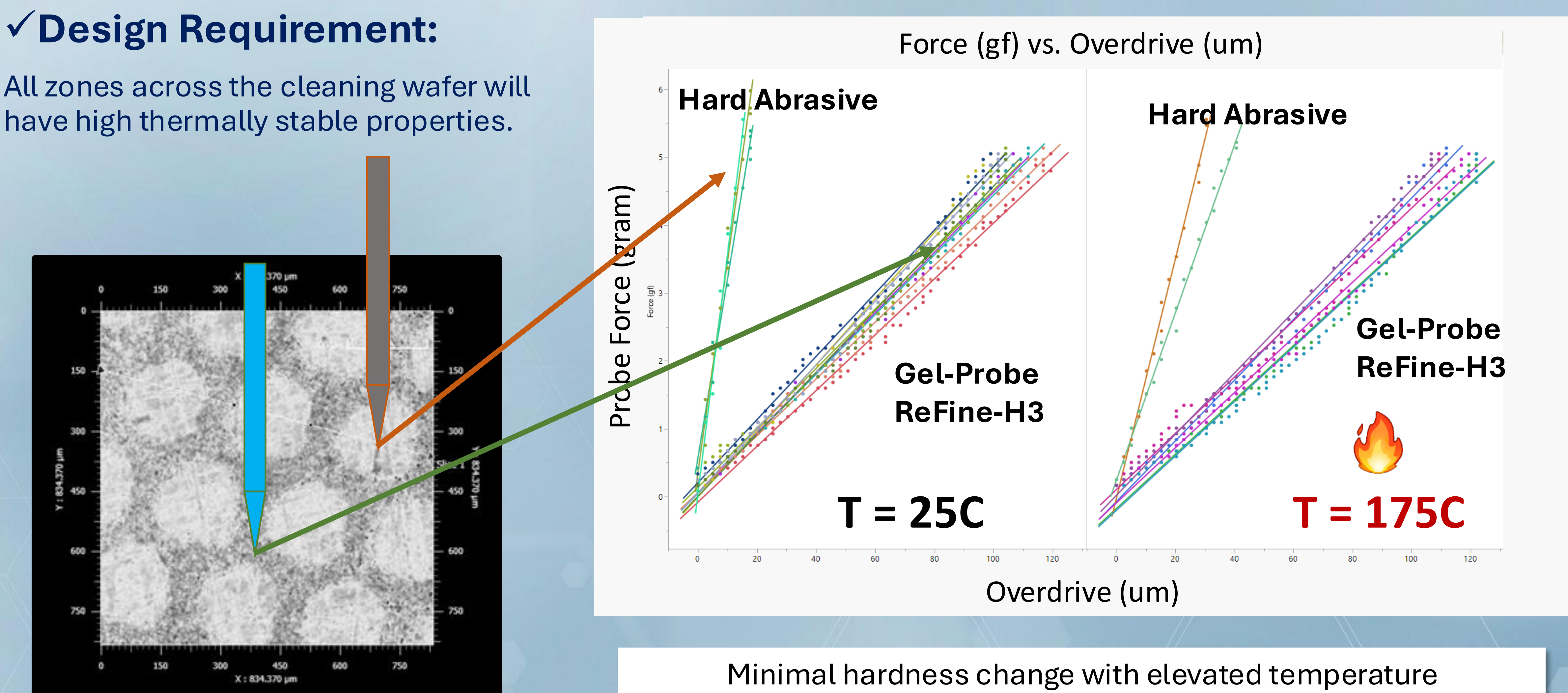
- Hard Abrasive is significantly harder than ReFine-H3
- Touchdown sequence is a 3:8 ratio of hard to soft

Patent Pending

Temperature Stability

✓**Design Requirement:**

All zones across the cleaning wafer will have high thermally stable properties.



Minimal hardness change with elevated temperature

Patent Pending

Customized Surface

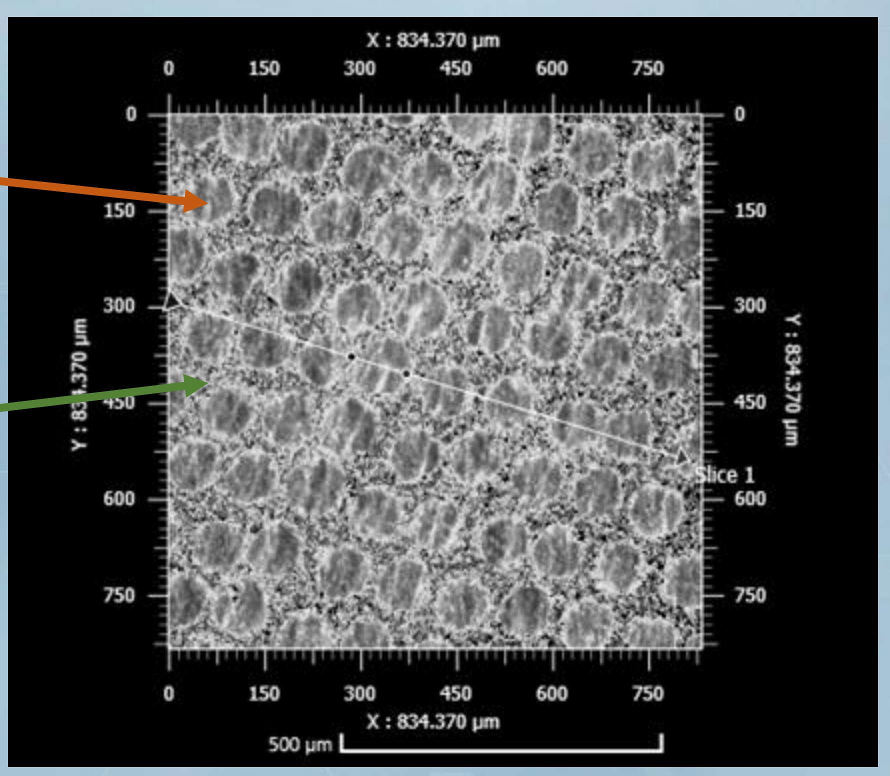
✓Design Requirement:

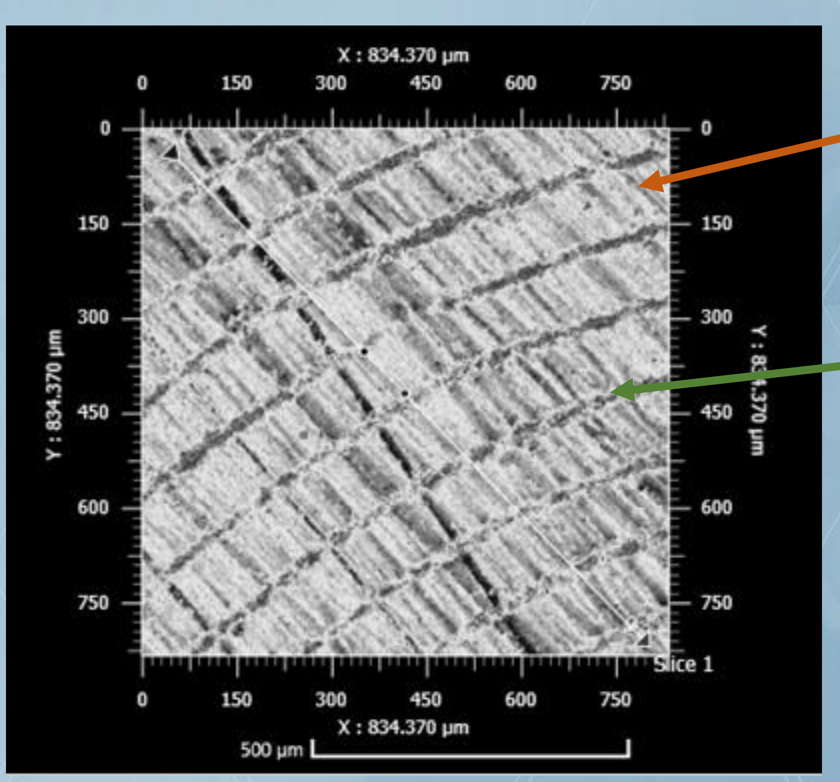
Domain size, location, and material type are customizable.

“Hard” Abrasive Material

Gel-Probe ReFine-H3 “SOFT”

Feature sizes <80um





“Hard” Abrasive Material

Gel-Probe ReFine-H3 “SOFT”

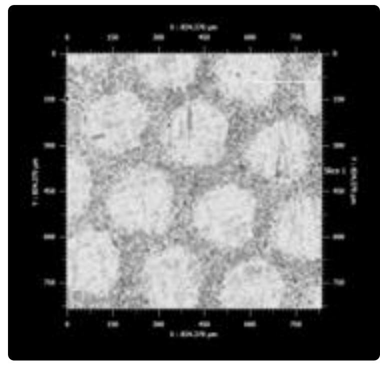
Tunable materials and patterns to match probe card design, prober and cleaning requirements

Patent Pending

Collaborative Project

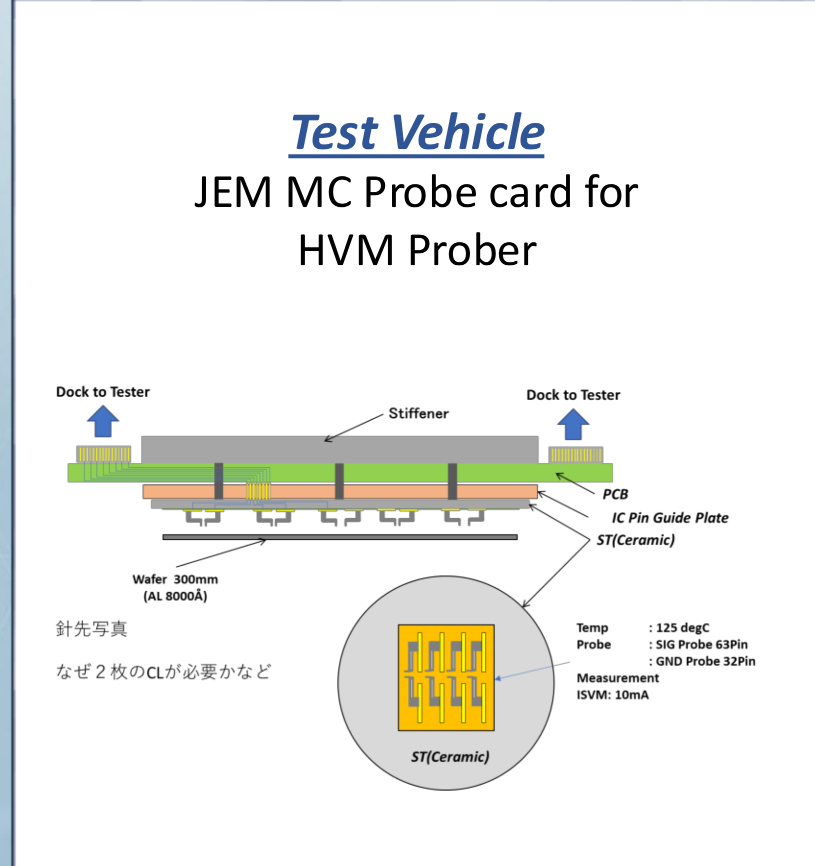
Cleaning Materials

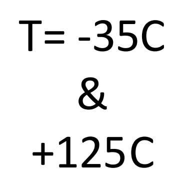
300 mm Multi-zone wafer
250 um diameter hard clean domains



vs

Combination Cleaning
Gel-Pak GP Refine-H3 (soft cleaning)
Silicon Cleaning Wafer (hard cleaning)





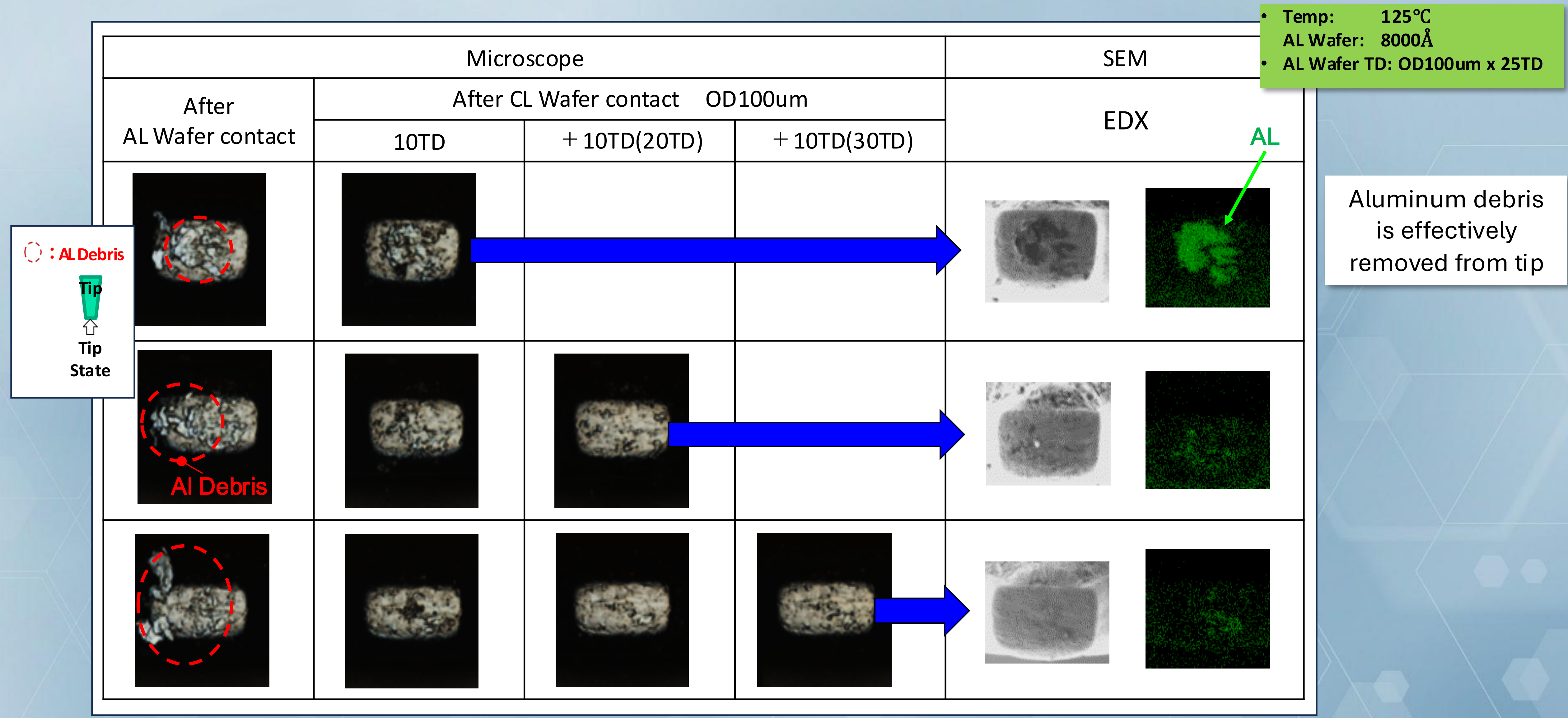
8000A
Blanket Al
Wafer

OEE Evaluation

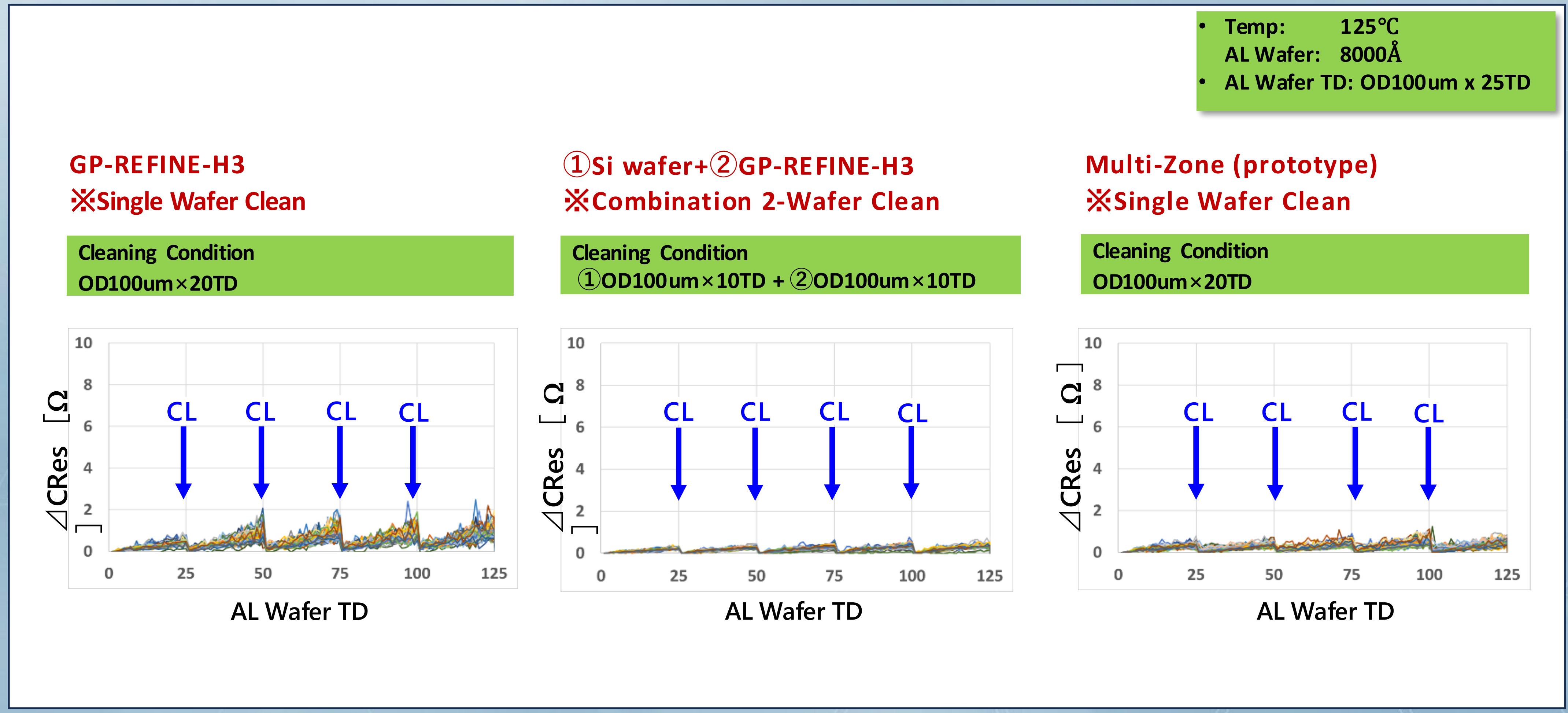
- Debris Removal Efficiency
- CRES Recovery
- Tip Wear Rate

Patent Pending

1-Wafer Process | Multi-zone Prototype



1-Wafer Process | Multi-zone Prototype



CRES recovery of multi-zone prototype is comparable to combination 2-wafer cleaning.

Low Temp Wear Assessment (T= -35C)

- Temp: -35℃
  AL Wafer: 8000Å
- AL Wafer TD: OD100um x 25TD

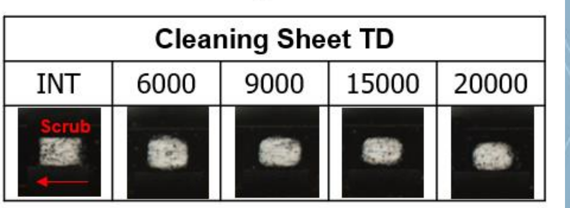
①Si wafer+②GP-REFINE-H3
※Combination 2-Wafer Clean

Cleaning Condition
Silicon : Polishing = 5TD : 5TD

Multi-Zone (prototype)
※Single Wafer Clean

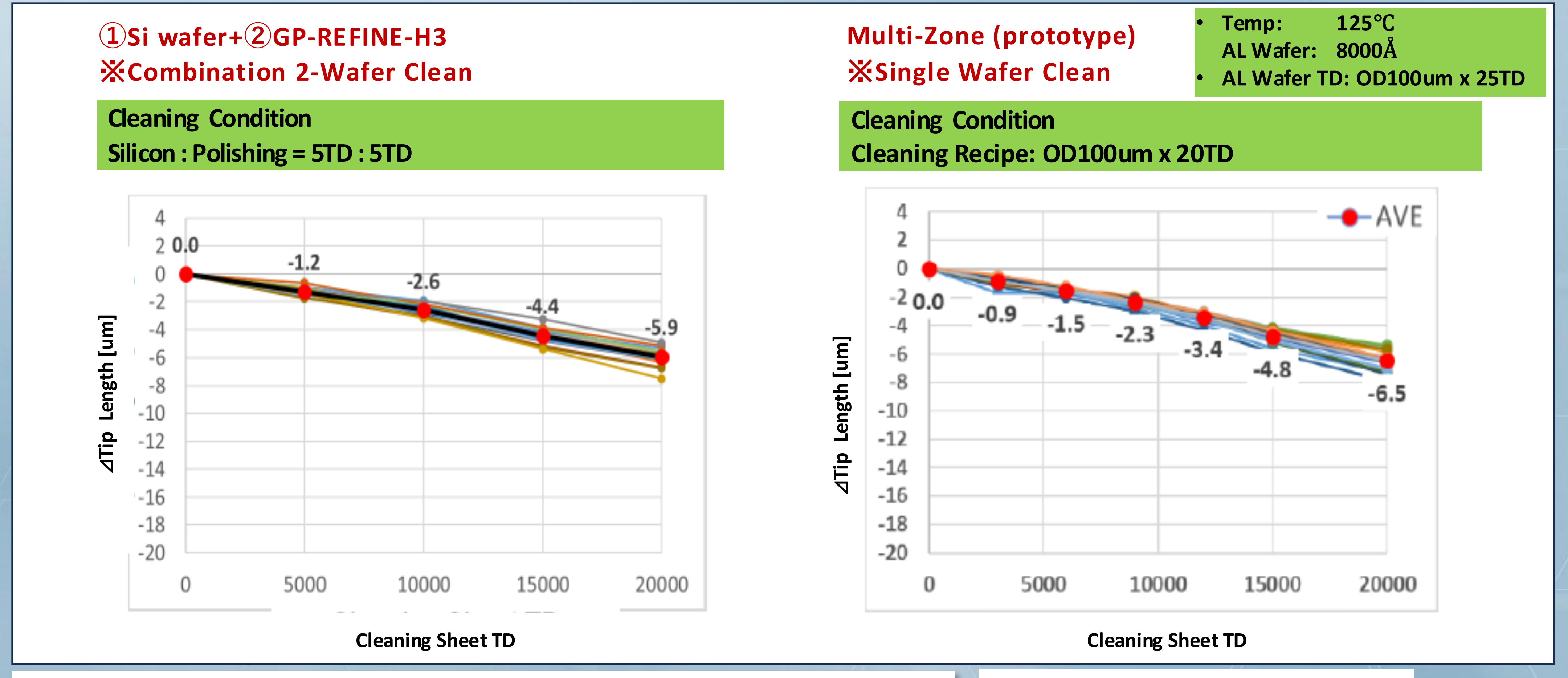
Cleaning Condition
Cleaning Recipe: OD100um x 20TD

Tip wear of multi-zone prototype is comparable to combination 2-wafer cleaning.



Cleaning Sheet TD				
INT	6000	9000	15000	20000

High Temp Wear Assessment (T= 125C)



Tip wear of multi-zone prototype is comparable to combination 2-wafer cleaning.

Cleaning Sheet TD				
INT	6000	9000	15000	20000
Scrub				

Summary | Improved OEE

- **Innovative, Multi-zone, single two step cleaning wafer developed**
  - Overall cleaning performance result is comparable to combination cleaning conditions.
  - High temp and low temp wear rates are equivalent to combination cleaning
  - Design and materials are customizable to develop specialized cleaning.
  - Simplifies the overall process flow for cleaning single wafer contactors.

- **Eliminates time-consuming, 2-wafer cleaning process for improved OEE.**

OEE Impact **(Overall Equipment Effectiveness)** Availability x Performance x Quality	**Productivity Loss in Manufacturing**	**1-Wafer Cleaning Process vs. 2-Wafer Cleaning Process**
Availability Loss	Downtime	Minimize
	Wafer Exchanges	Minimize
Performance Loss	Minor Stops	Fewer
	Reduced Speed	Fewer
Quality Loss	Yield	Maximize
	CRES Stability	Maximize

Next Steps

- Low volume manufacturing
- Customer collaboration and qualification

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