



# Advanced Testing Technology for Future Requirement



**CP Testing Division**

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# Overview


- **Introduction of KoreSemi**
- **The Opportunity for Advance Testing Technology**
- **Relevance of Product Development and Advance Probing Challenges**
- **Ideal Testing Structure & Integration**
  - Introduction of unmanned handling technology
  - EDA System further integration & Development
- **Conclusion**
- **Follow-On Work**

# About KoreSemi

- Foxconn Technology Group and the Qingdao government jointly invested in the establishment of KoreSemi in Qingdao in July, 2020 .
- KoreSemi belongs to S Business Group which is under Foxconn Technology Group to support **3+3 strategy**
  - 3 Innovative Industry : Electric Vehicles, Digital Health, Robotics
  - 3 Core Technology : AI, Semiconductors, Next-Gen communications

**A** 

Smart Phone ·  
automation  
equipment ·  
Precision tool ·  
3D & Cover  
glass



**B** 

Wearable  
device · tablet  
· Notebook ·  
Smart Speaker  
Mini



**C** 


Precision mold ·  
mechanical part  
· Applied  
Materials




**D** 

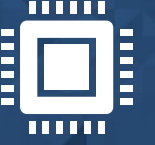
PC · IPC ·  
interactive  
whiteboard ·  
printer ·  
displayer



**E** 

LCD TV ·  
game console ·  
Photography  
Equipment ·  
intelligent  
robot



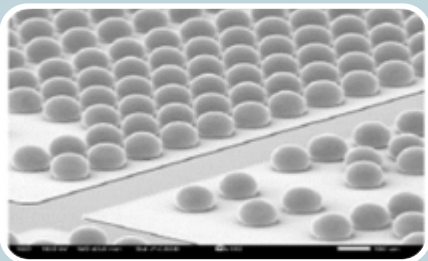
**S** 

Wafer Technology  
· Assembly &  
Testing · Design  
Service · Power IC  
· Sensor IC ·  
Module · Channel



# KoreSemi Turn-Key Solution

- 3 Production Lines in MP : Bumping / RDL, WLCSP, DPS and CP.
- FOStrip is ready for customer new tape out.



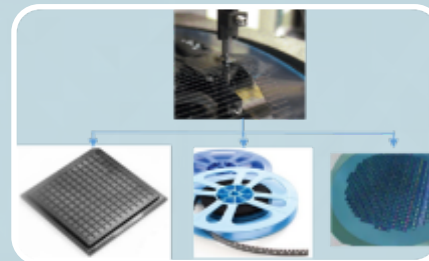
## WLP

- Cu Pillar Bump
- Lead Free Bump
- RDL
- WLCSP
- Glass Wafer RDL
- Gold bump



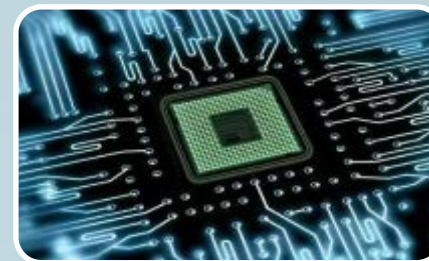
## CP

- Memory (DRAM , Flash, MCPs)
- Logic (Mixed-signal, digital, Analog)
- CIS
- Driver device



## DPS

- Grinding
- Laser Marking
- Saw
- Wafer , Reel, or Tray



## Turnkey Service

- Bumping + CP + Assembly + FT
- SMT and Module
- FATP(Final Assembly, Test and Packing)



## RD & FOStrip®

- 2D/2.5D Tech.
- 3D Integration
- Wafer on Wafer
- AiP

# The Opportunity for Advance Testing Technology

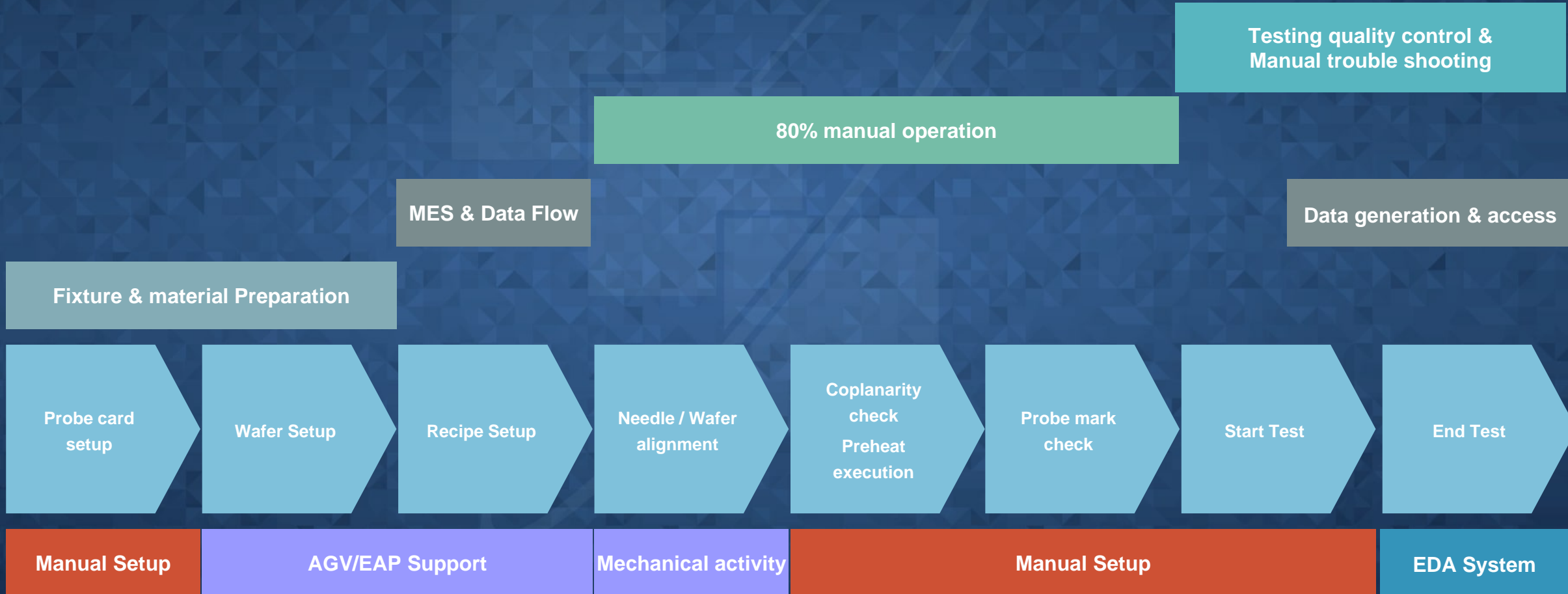
More new technologies and products for heterogeneous integration, Those business opportunities are for advanced packaging and high-end testing. The trend of heterogeneous integration led by "advanced packaging and testing" technology is clear, and it also brings out the highlights of 3D wafer stacking technology, which will cooperate with 2D miniaturization of advanced processes to build an era of "surmount Moore's Law".

# Relevance of Product Development and Advance Probing Challenges

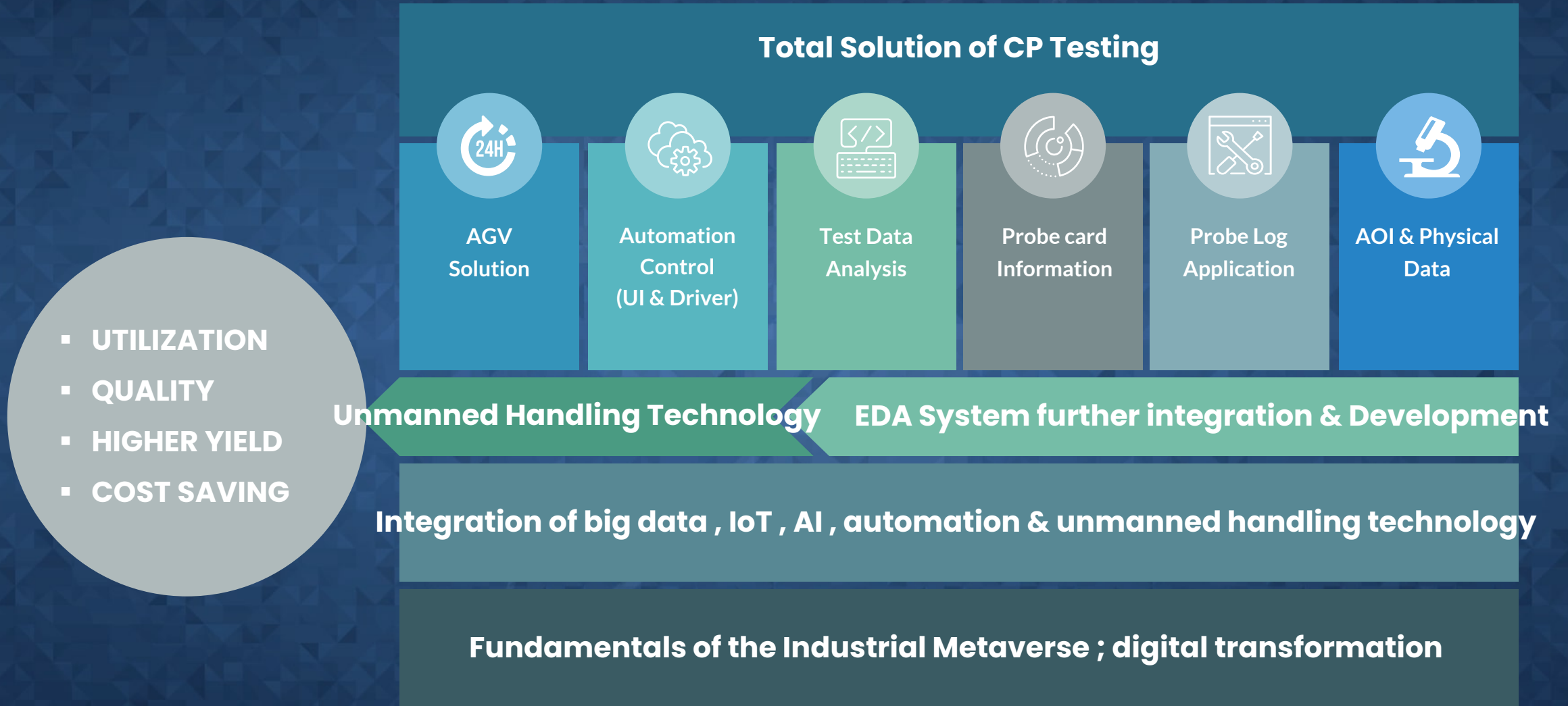
- Trends of next-generation product development
- In response to product development, upcoming challenges
- The requirement of Probing Capability and Service

# CP Testing Flow

CP Testing Flow



# Ideal Testing Structure & Integration





# Ideal Testing Structure & Integration

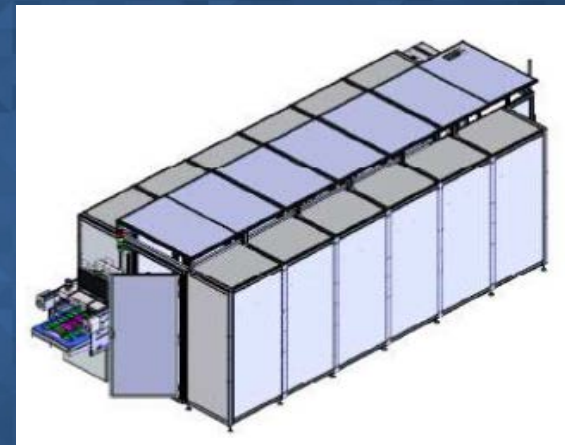
- **Unmanned Handling Technology**
  - a. AGV Application (Probe Card/Wafer)
  - b. Application of Automated Control
- **EDA System further integration & Development**
  - a. Integration of testing result & probe data
  - b. Application of probe log analysis
  - c. AOI & PMI data using
  - d. Smart auto-retest

# Ideal Testing Structure & Integration

- **Unmanned Handling Technology**
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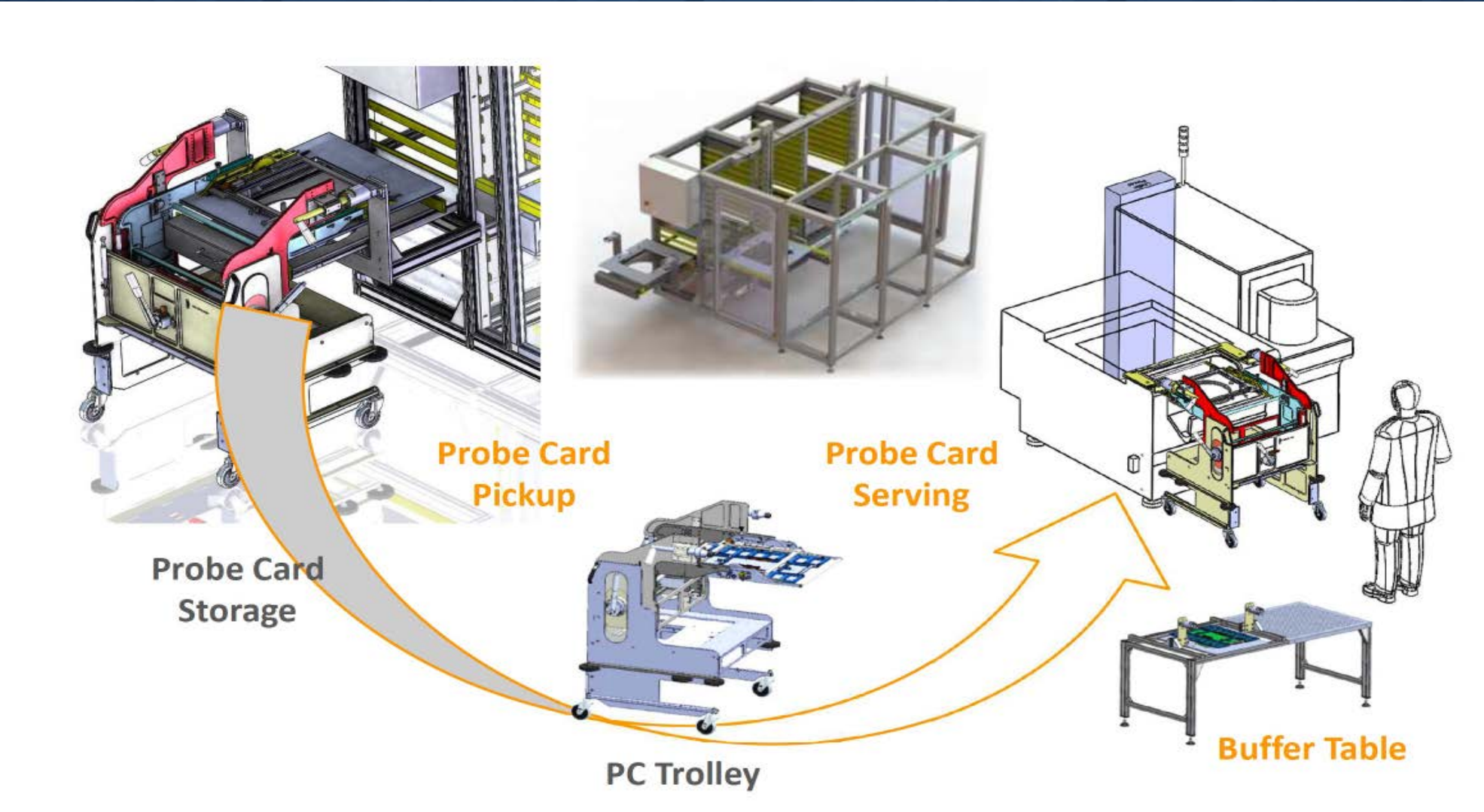
# Storage System with Probe Card Trolley

Scenario set for 12 Cabinet of V93K/P1600 , the total capacity is estimated **342 pcs**.  
(The first cabinet will be 23 pcs and others are about to hold 29 pcs per cabinet – totally will be  
 $29 \text{ pcs} \times 11 \text{ cabinets} + 23 \text{ pcs} = 342 \text{ pcs}$ )

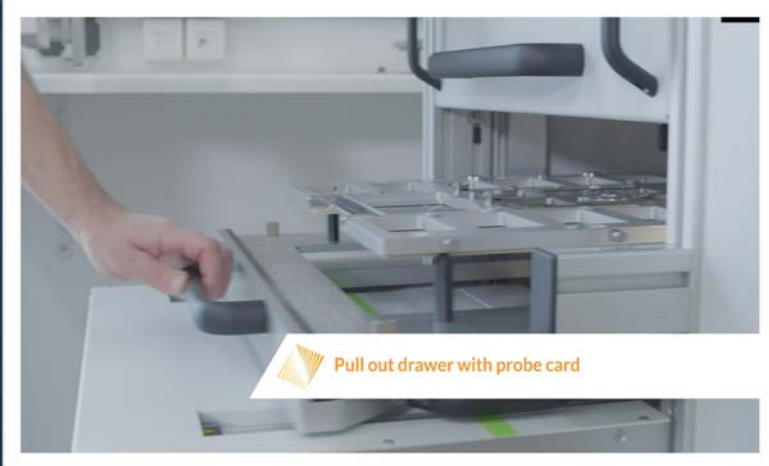
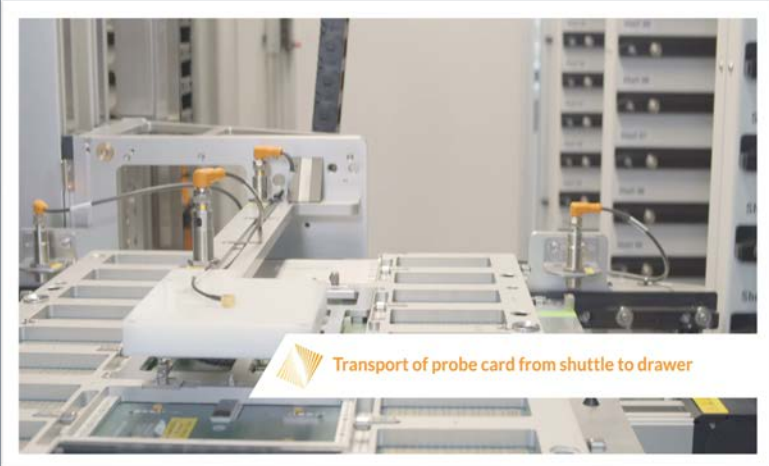
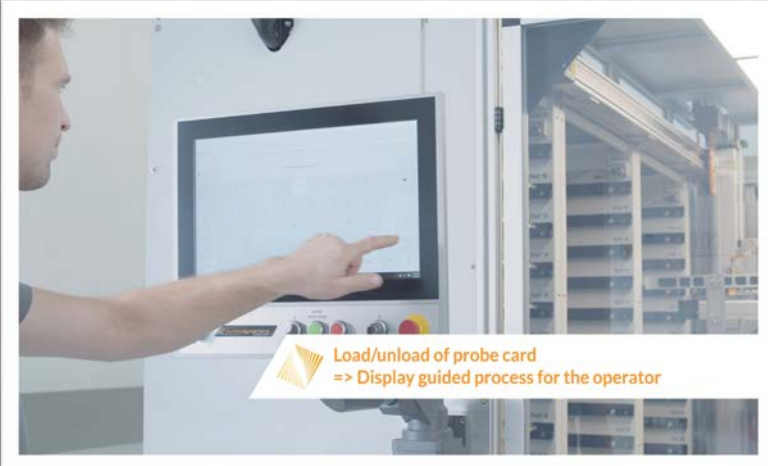


TD Storage Cabinet  
stack up illustration  
(sample shown for 6x Cabinets)

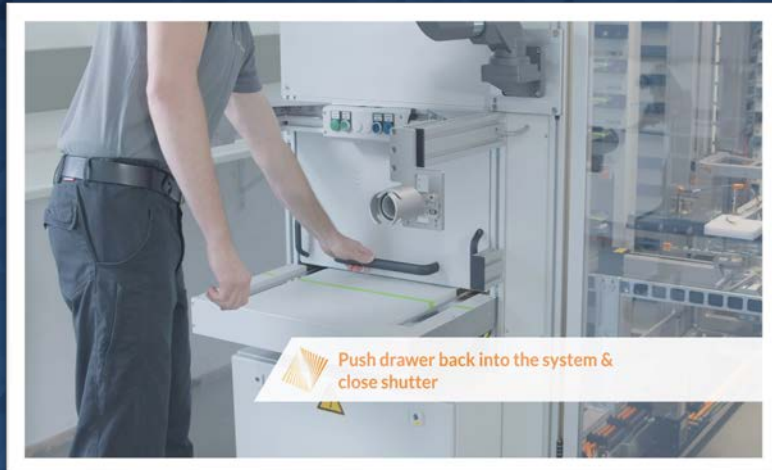
# Probe Card Trolley



# Probe Card Trolley

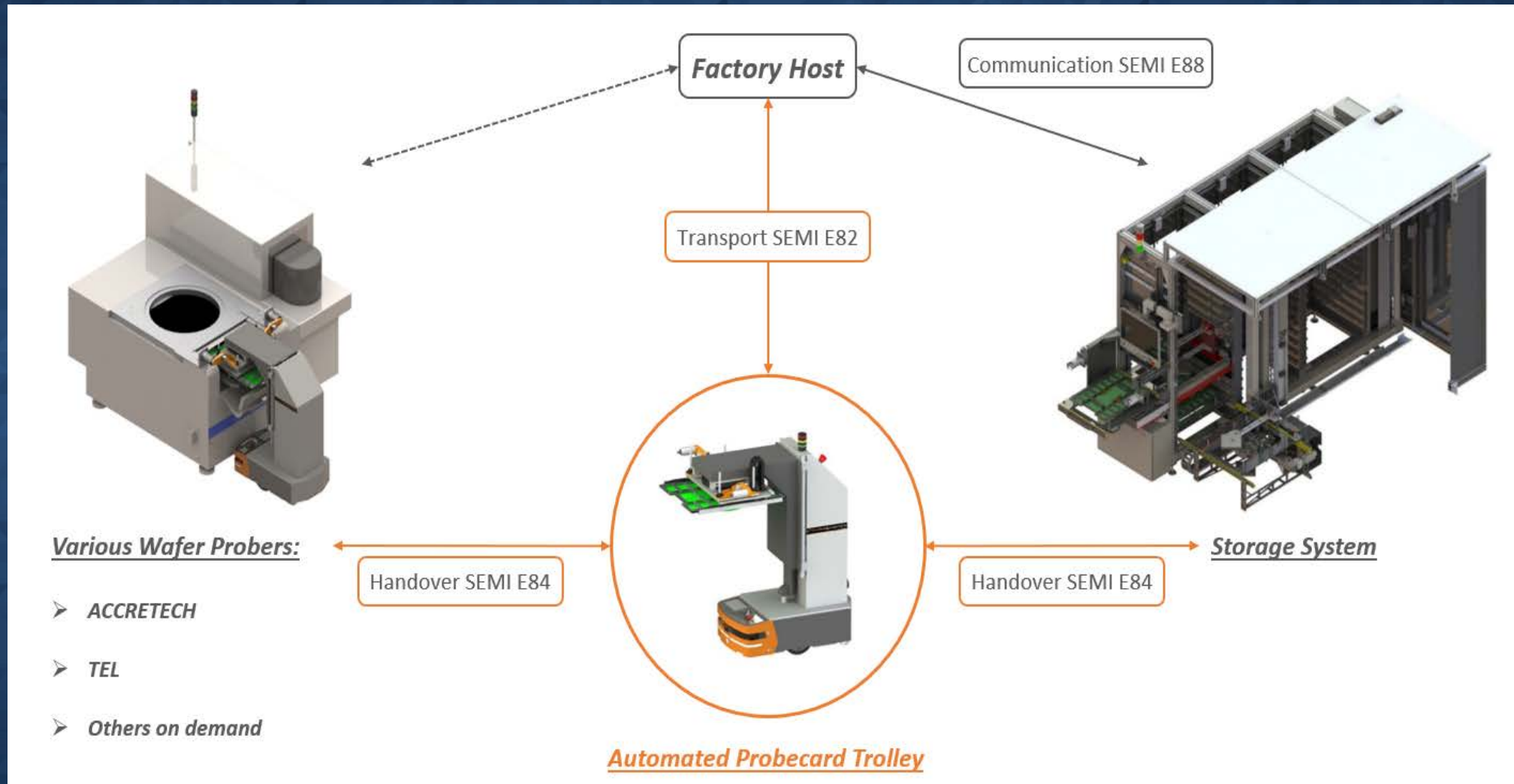


# Probe Card Trolley



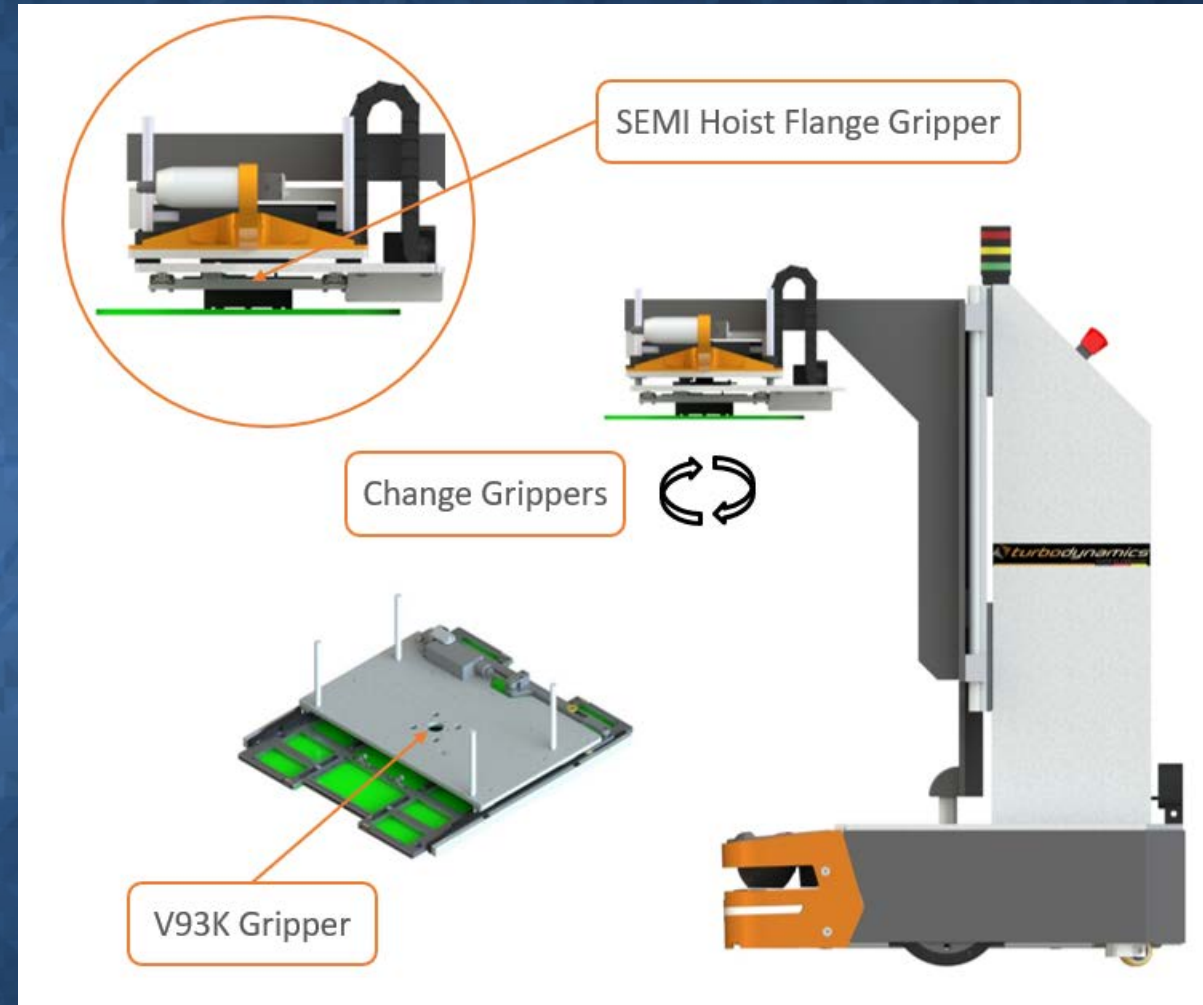
- **Structured Work Flow & Process**
- **Secure handling & storage of high cost fixture**
- **Hands-free process / Avoid human error**
- **Relief from heavy carriage**
- **Efficient usage of floor space**
- **Universal Device Carrier for different**
- **SECS/GEM Interface / Industrial 4.0 ready**

# Automated Material Flow



# Modular Design

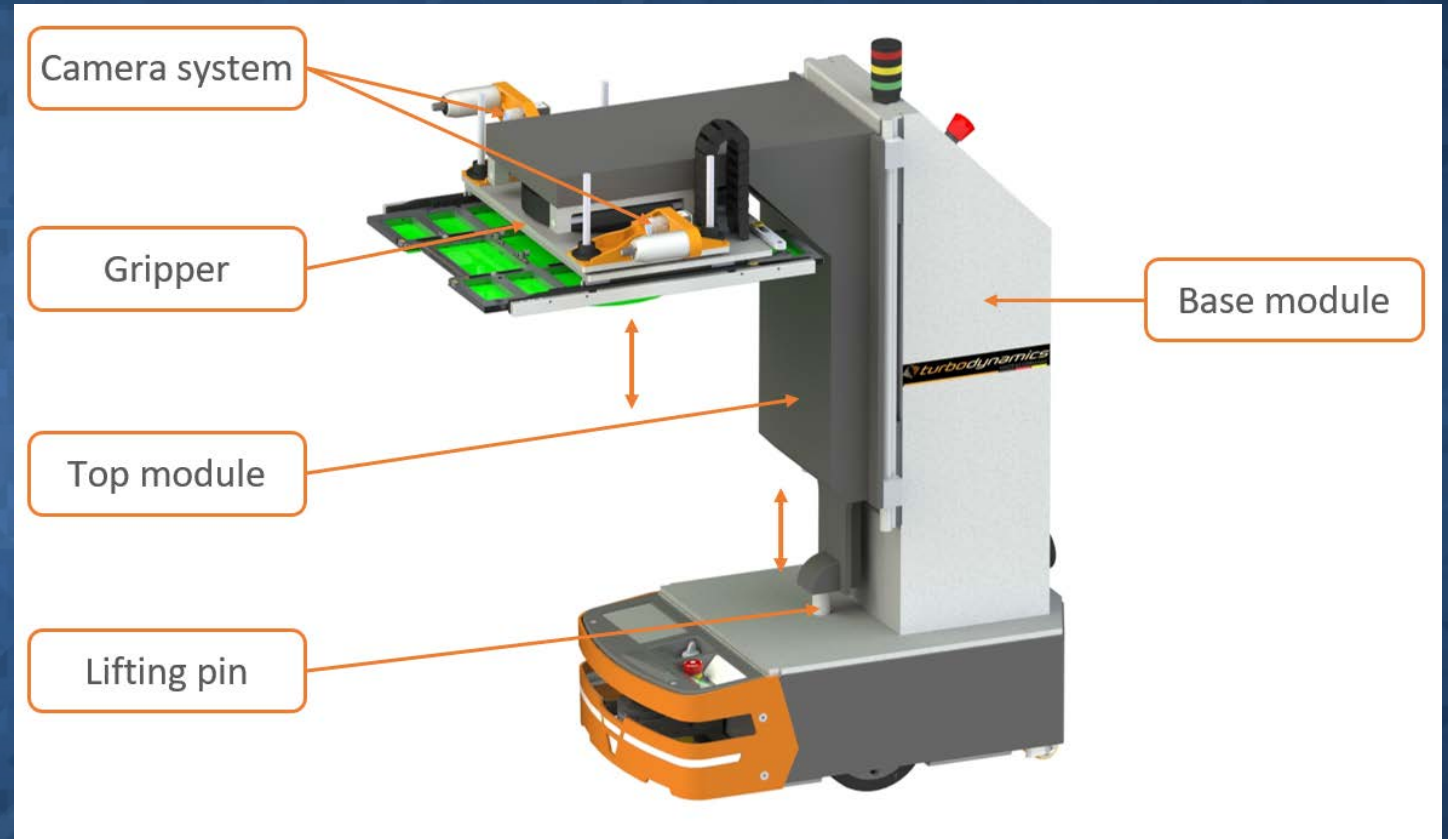
- Modular design for handling of different stiffeners/flanges:
  - Advantest: T2000, V93K
  - Teradyne: U-Flex, M-Flex
  - SEMI Hoist Flange
- This is achieved by manually changing the individual grippers ( $\leq 1$  hour)
- The change of the grippers is monitored through an RFID- technology and is transferred to the host





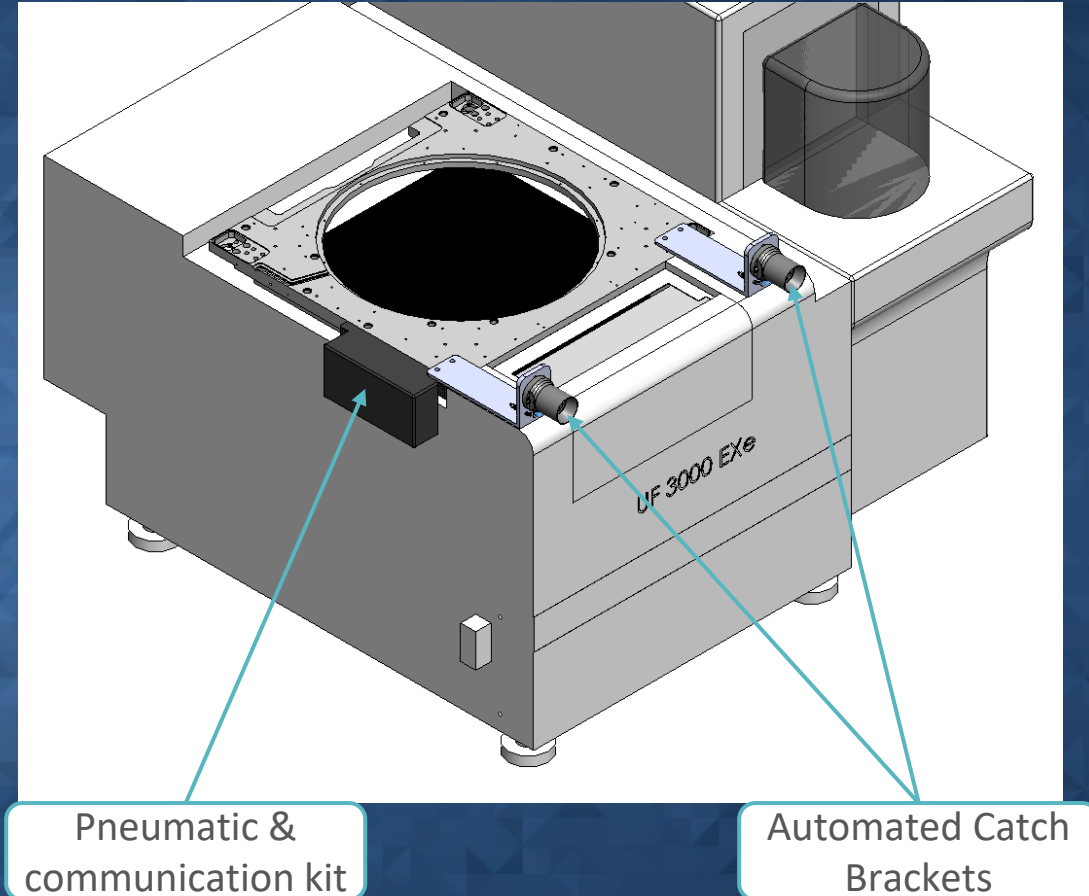
# Probe card Handover

- Alignment to the height of the auto catch brackets is achieved by an intelligent camera system
- A deviation of the different heights of the probers can be compensated
- Handover according to the SEMI E84 standard via parallel I/O interface



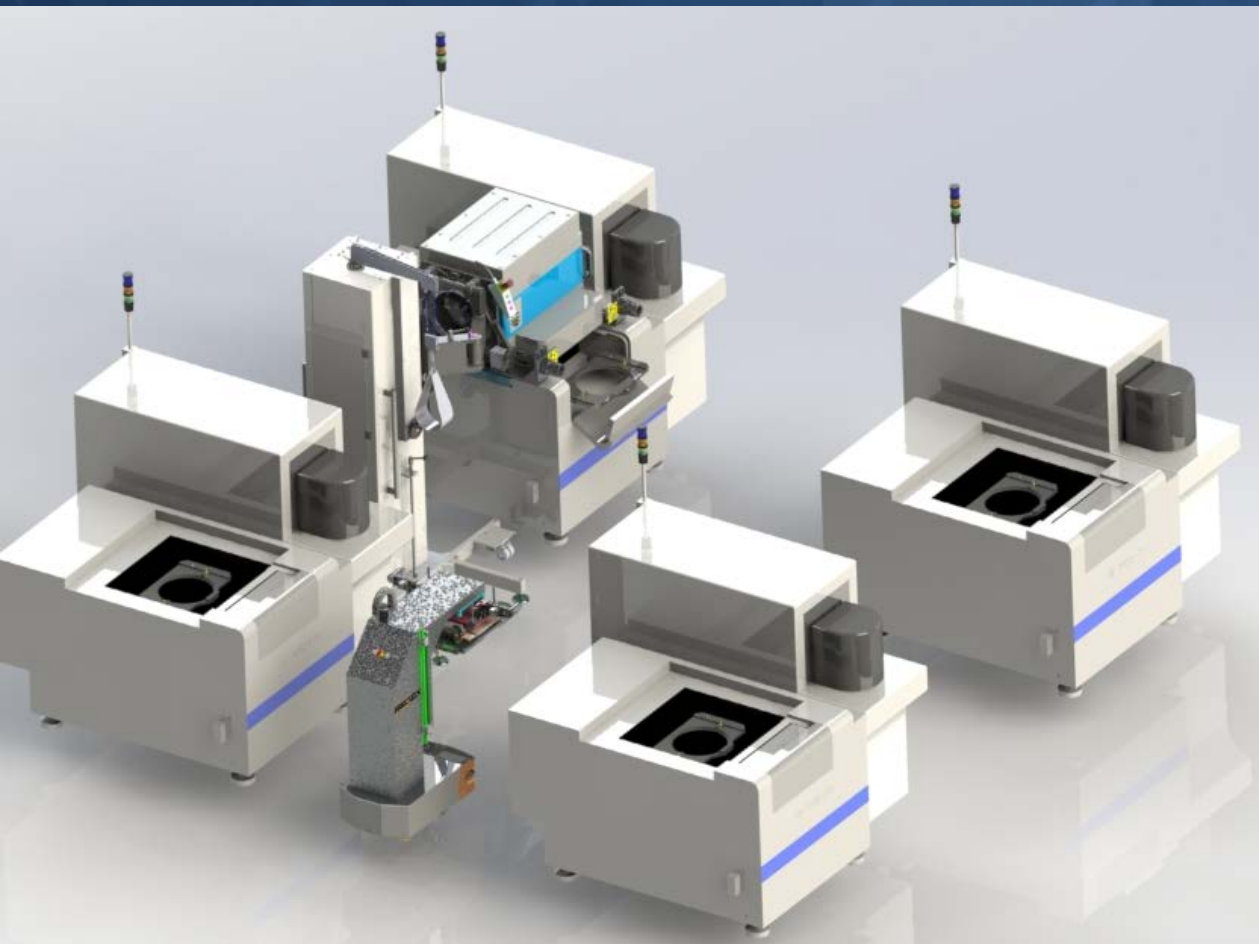
# Prober Preparation

- Attaching the automated catch brackets to the head plate
- Attaching the pneumatic & communication kit to the side of the head plate (size 300x150x80 mm)
- Simple installation
- Automatic open front access door is required



# Workflow on UF3000EXe test floor with V93k and auto trolley

AGV Trolley moving in the corridor



AGV Trolley at docked position onto UF3000 Exe



# AGV Application for Wafer



# Ideal Testing Structure & Integration

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# Application of Automated Control

SmartSetupTool ver.1 powered by Wellitech.com

Lot Info DC

**DC Step**

TranDC  
LotStart  
AutoSoak  
AutoDC  
TranProd  
DataIn

**DC Display**

1 2 3 4  
5 6 7 8

ManuDC

**DC Log**

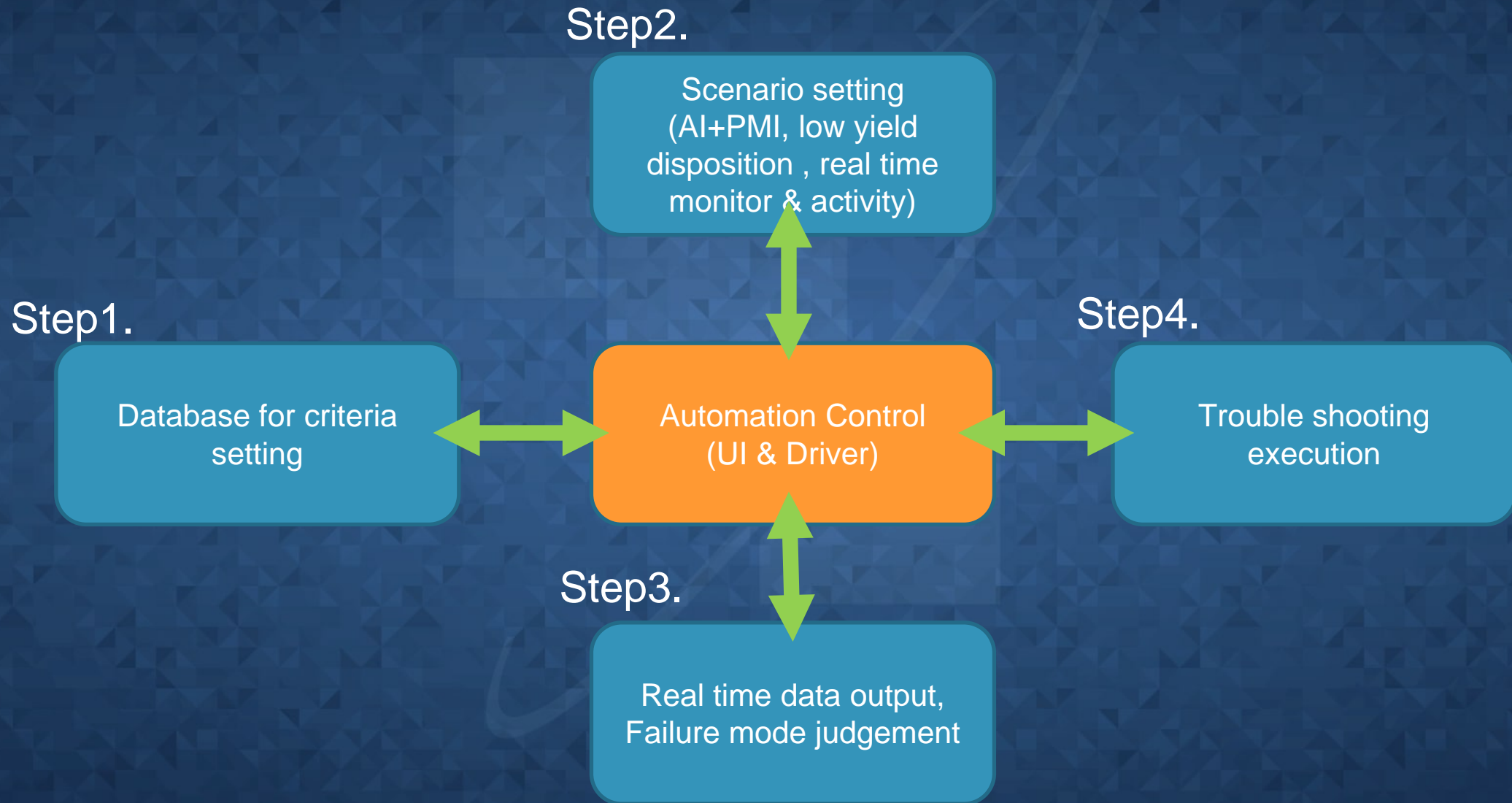
```
0|FAFFFFFFF
10|FAFFFFFFF
11|FAFFFFFFF
12|FAFFFFFFF
13|FAFFFFFFF
14|FAFFFFFFF
15|AAFAFAAAA
16|AAFAFAAAA
17|PAAPAAAAP
18|PAAPAAAAP
19|PPPPPAAP
20|PPPPPAAP
21|PPPPPPPP
10|FAFFFFFFF
AUTODCPASS
TRANPRODSTART
Tran Prod Pgm Done
TRANRODPASS
DATAINSTART
DATAINPASS
```

**DC Step**

Index	Height	D1	D2	D3	D4	D5	D6	D7	D8
96	10	F	A	F	F	F	F	F	A
95	21	P	P	P	P	P	P	P	P
94	20	P	P	P	P	P	A	A	P
93	19	P	P	P	P	P	A	A	P
92	18	P	A	A	P	A	A	A	P
91	17	P	A	A	P	A	A	A	P
90	16	A	A	F	A	F	A	A	A
89	15	A	A	F	A	F	A	A	A
88	14	F	A	F	F	F	F	F	A

- Lot information Setup
- Testing Program Download
- Probe File Setup & Probe Start
- Probe Setup
- Testing parameter check
- Log record for setup process
- Real time yield ,condition monitor
- Real time control & machine stop
- On line repair & parameter change

# Structure of Automated Control



# Ideal Testing Structure & Integration

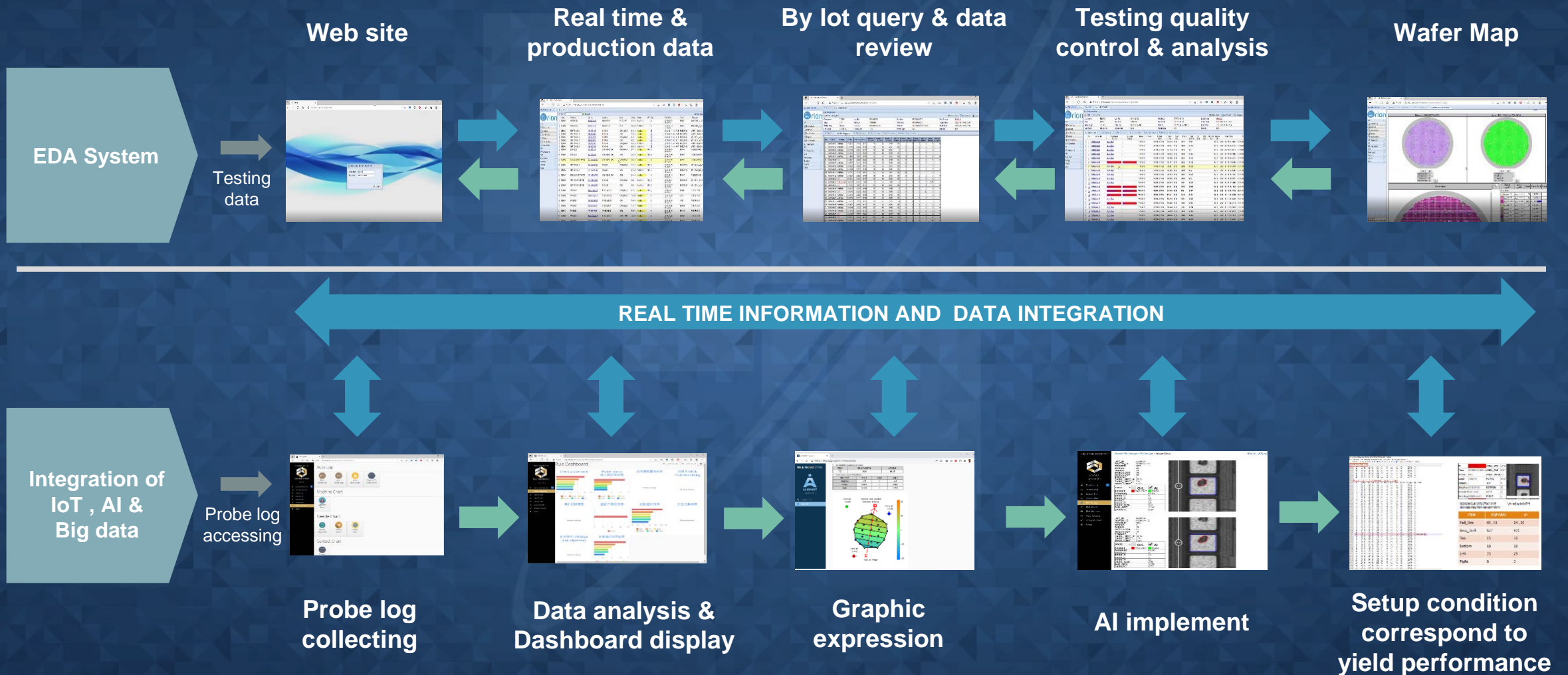
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# EDA System Development

- **EDA is not only used for testing data analysis after wafer testing**  
ex. Combine with data log, physical data & parameter to have more value
- **How to integrate real time data & automated function for quality control**  
ex. Realize execution of dynamic trouble shooting by real time monitor
- **How to integrate probe log & AOI data for further analysis**  
ex. For alarm analysis, early warning of PM , probe card status confirm
- **How to provide useful information to scheduling system for best testing combination or condition**
- **How to provide the useful testing information for yield improvement**

# Integration of testing result & probe data



# Application of probe log analysis

**Auto-log**

Auto Log

Machine Chart

Needle Chart

Contact Chart

**Log statistics**

Rule Dashboard

Check probe mark

Prober alarm

自動量針時間

針位自動補償

**Graphic expression**

ALIGNKIT system PE

TYPE	PLANARITY	ANGLE
T2	30.8	18.53

AI Machine Learning process

3D diagram of probe tip with labels: Cone #2 (Seed), Cone #1 (-0.9), Cone #3 (-4.2), Front of Prober.

**Report generation**

Error Reports

Needle Reports

Device Reports

**AI implement**

ESM2 system PE

LOT ID	AS091A
WAFER ID	A5091A-12
PROBER	M05
SITENO	20
PADNO	19
SITECOORDX	59
SITECOORDY	48
AMOUNT	7
DARK_LIMIT_H	30 %
DARK_LIMIT_L	3 %
EDGE_LIMIT	0 mtr

AI implement

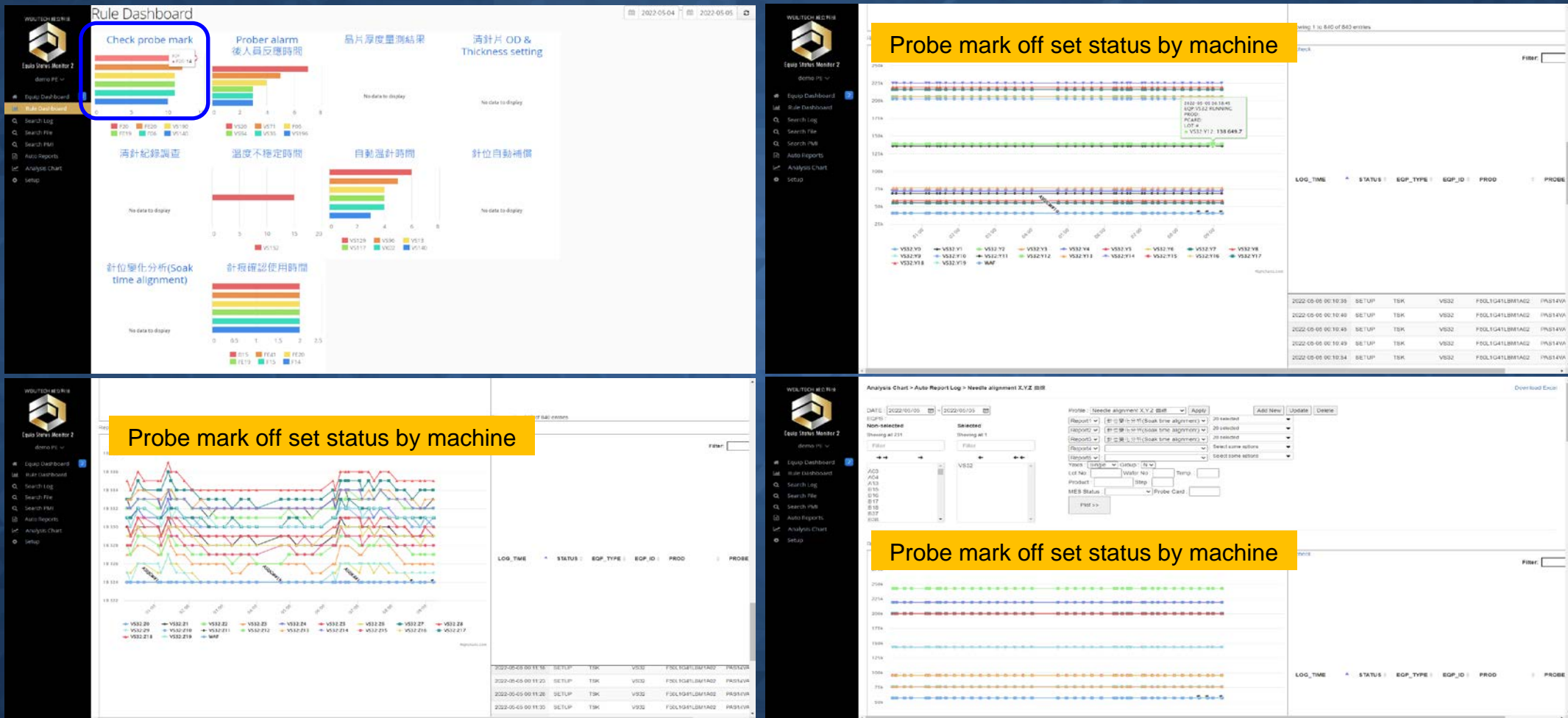
**Best Parameter**

ITEM	EQP:M05	AI
Pad_Size	65, 51	64, 50
Area_Dark	527	501
Top	15	16
Bottom	18	19
Left	23	23
Right	0	0

Best Parameter

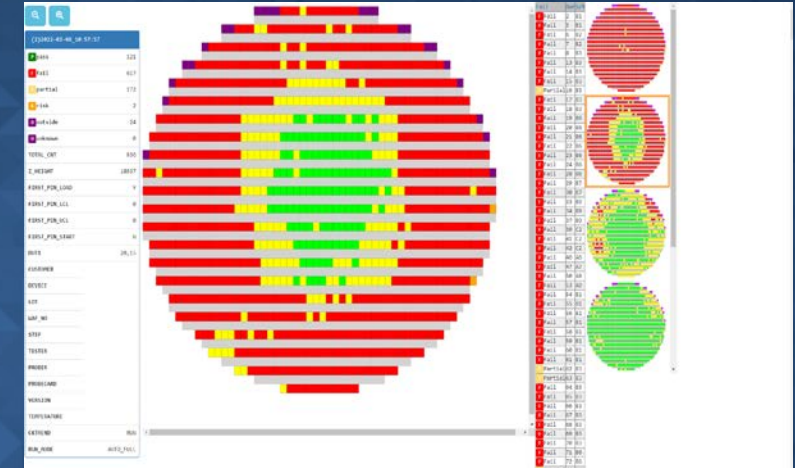
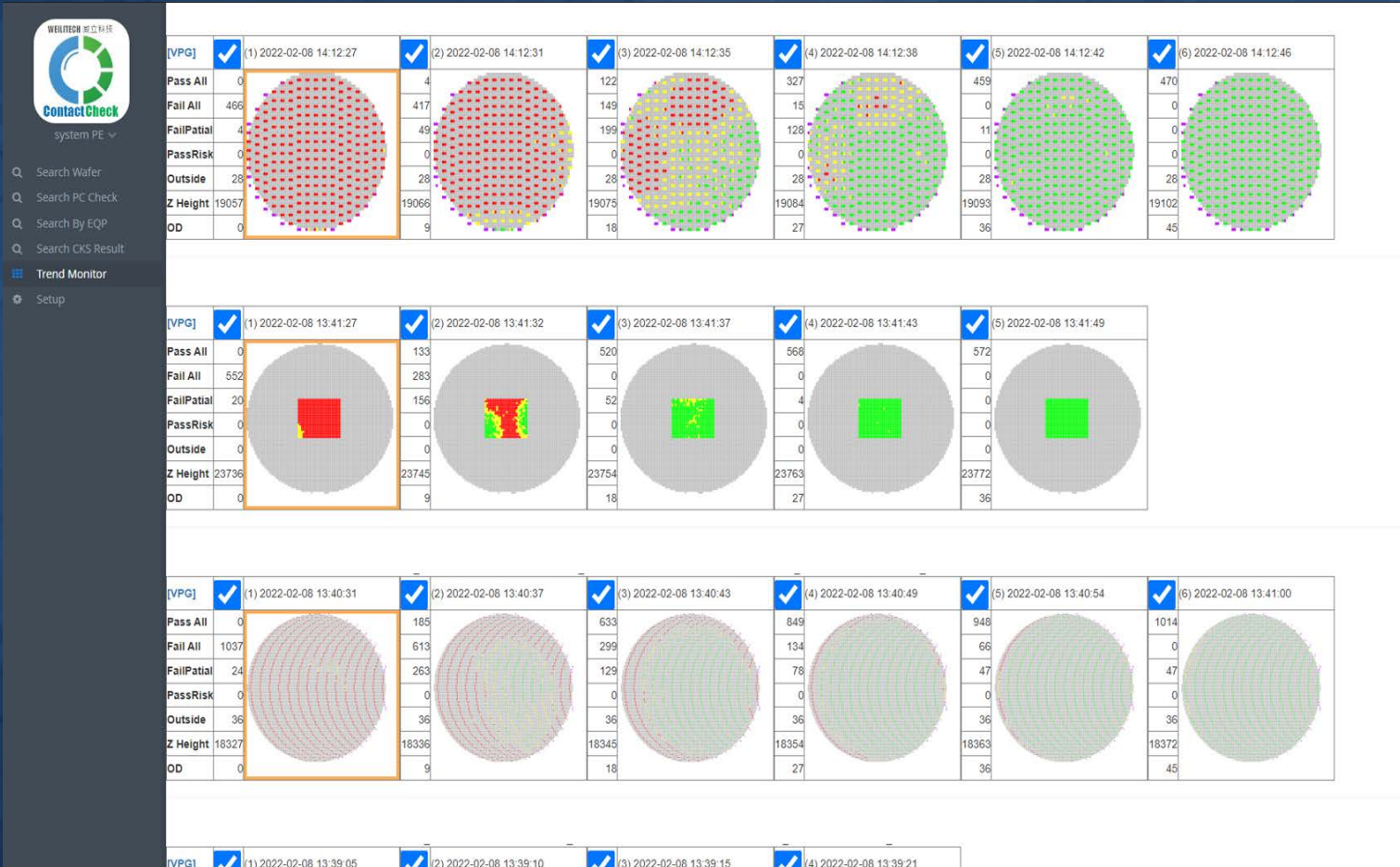
# Application of probe log analysis

## Probe mark status monitor

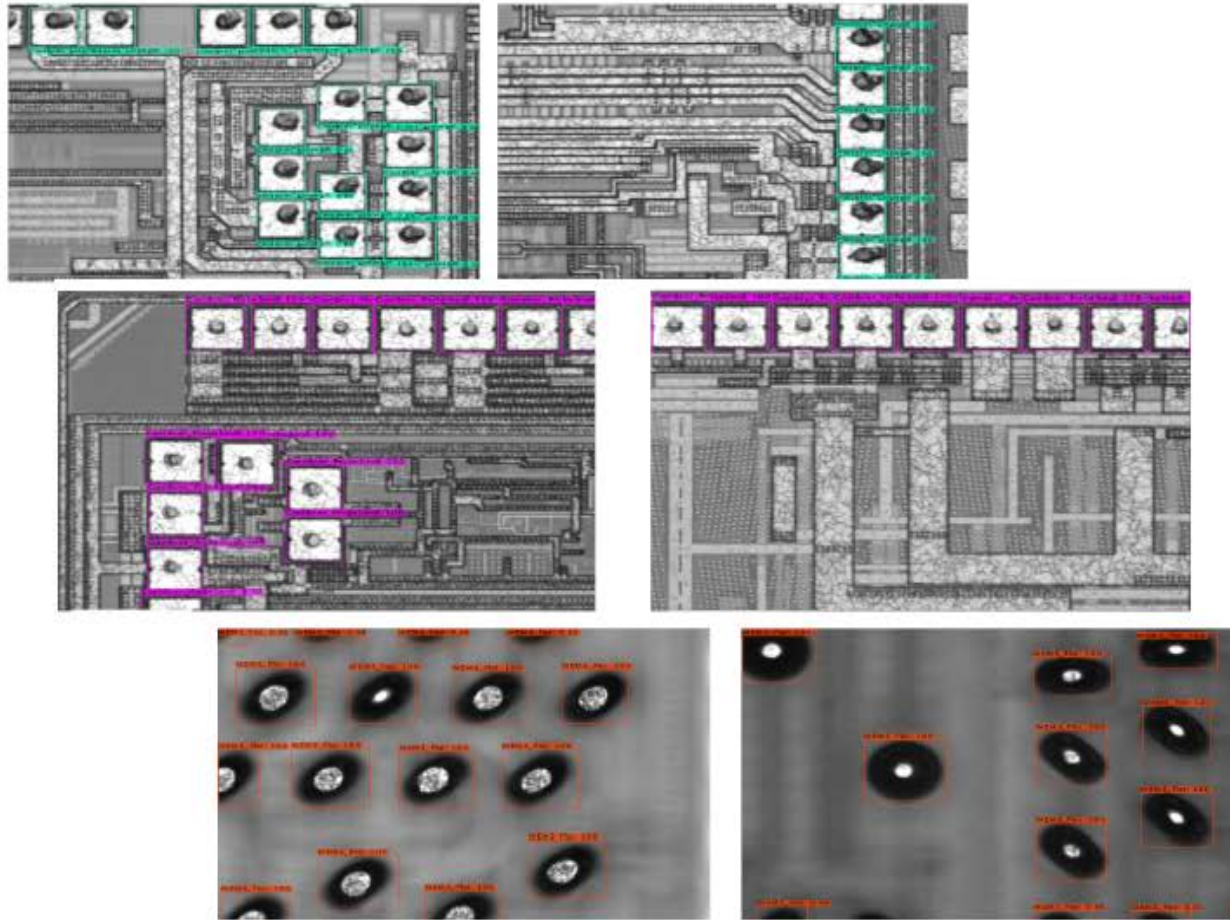


# Application of probe log analysis

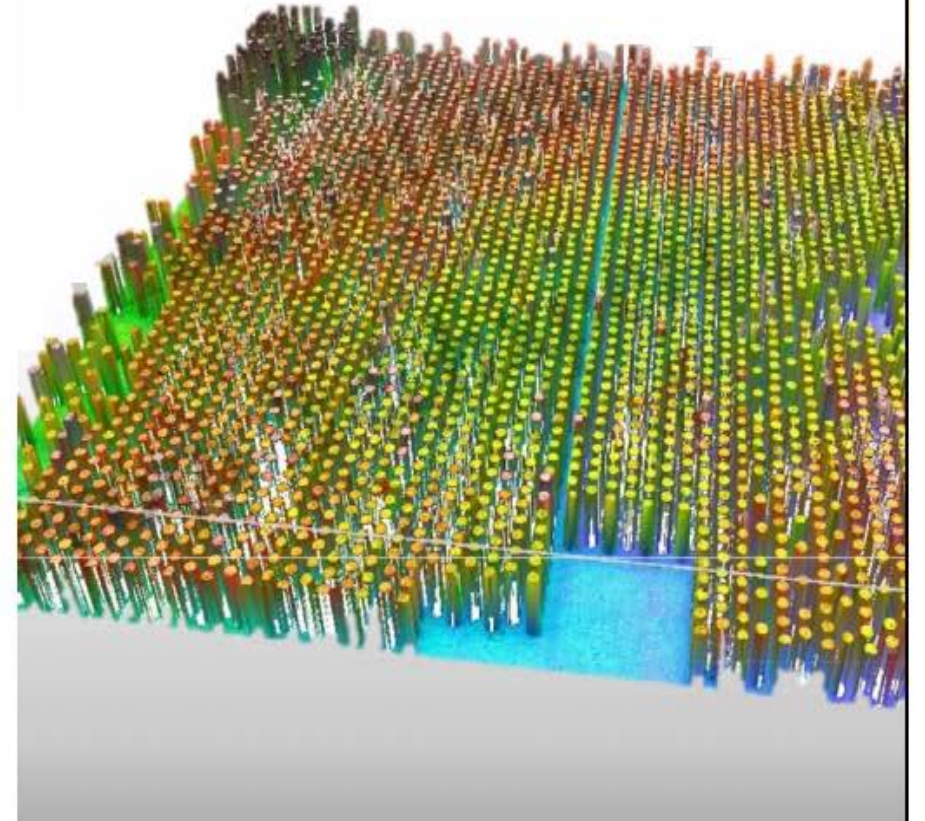
## ■ Contact / Coplanarity Check Display



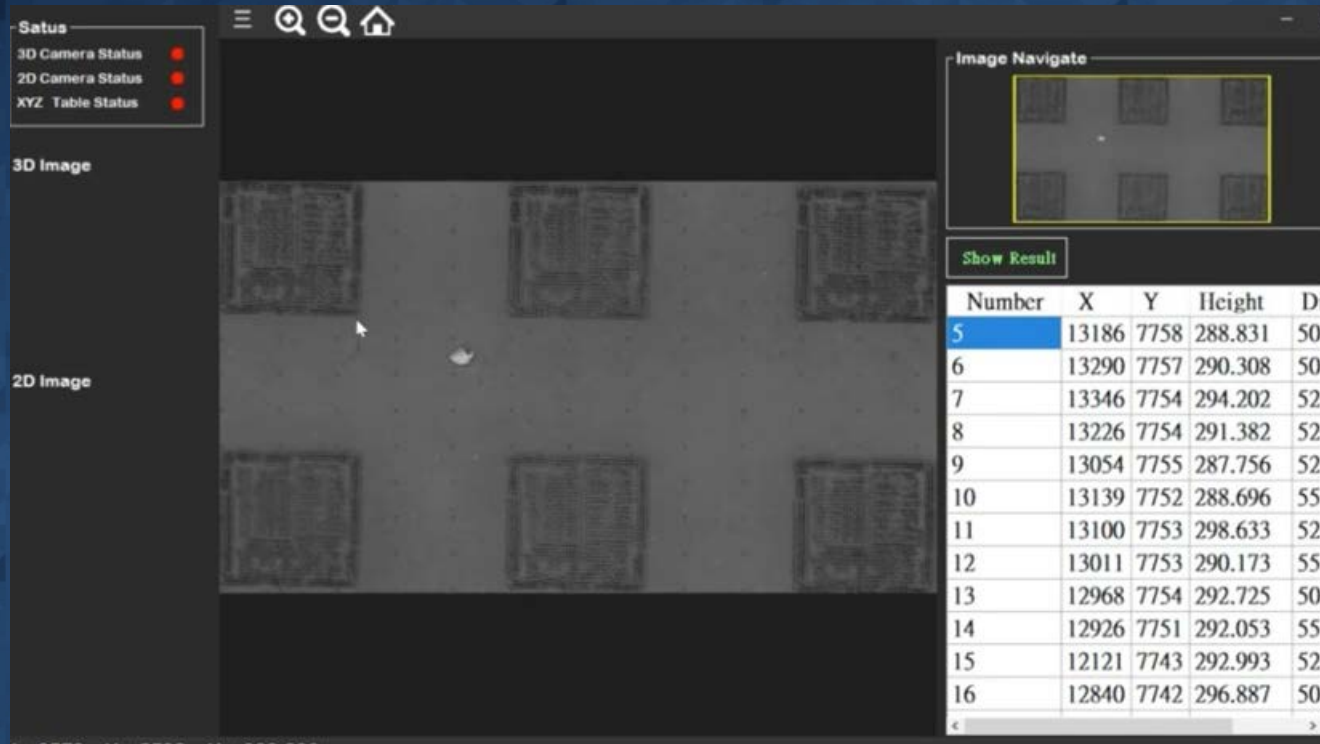
# Off line PMI & Probe Card Check



1. All Pins scanning & mapping to needle position
2. Confirm unhealthy probe mark & dut's yield status



# Off line PMI & Probe Card Check



Satus

- 3D Camera Status
- 2D Camera Status
- XYZ Table Status

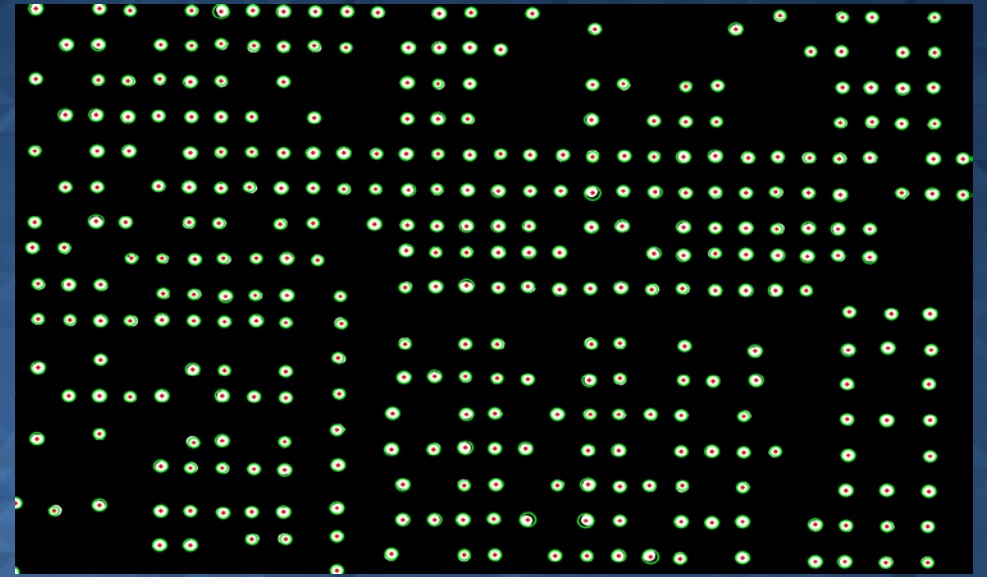
3D Image

2D Image

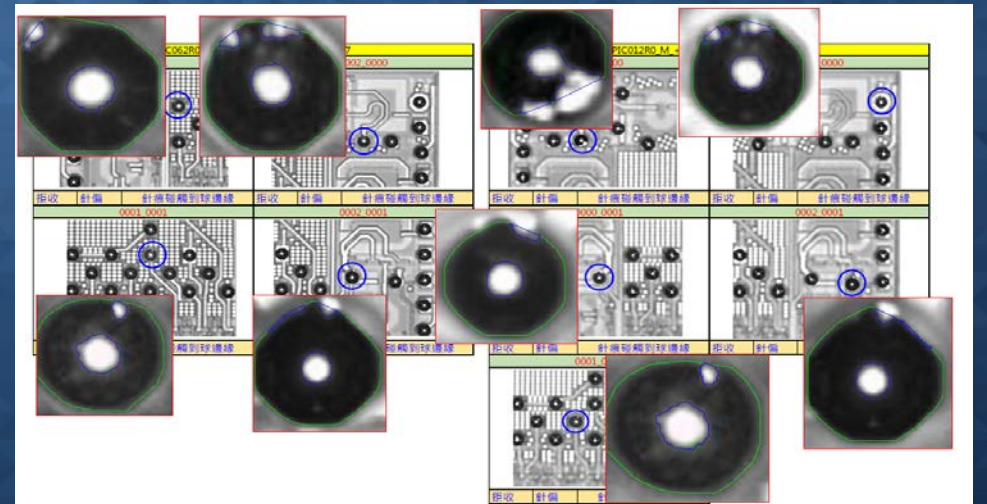
Image Navigate

Show Result

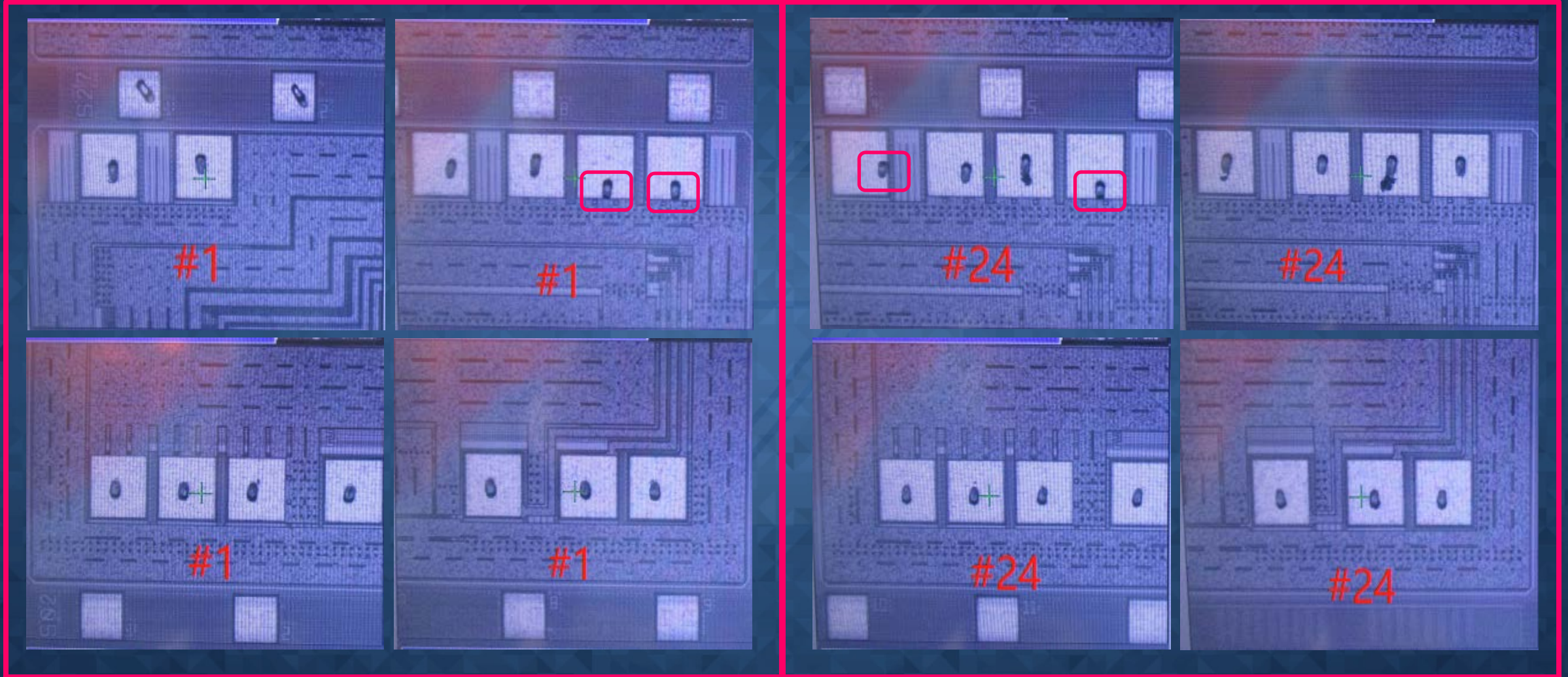
Number	X	Y	Height	D
5	13186	7758	288.831	50
6	13290	7757	290.308	50
7	13346	7754	294.202	52
8	13226	7754	291.382	52
9	13054	7755	287.756	52
10	13139	7752	288.696	55
11	13100	7753	298.633	52
12	13011	7753	290.173	55
13	12968	7754	292.725	50
14	12926	7751	292.053	55
15	12121	7743	292.993	52
16	12840	7742	296.887	50



- New algorithm can support to judge result of bump to confirm needle status

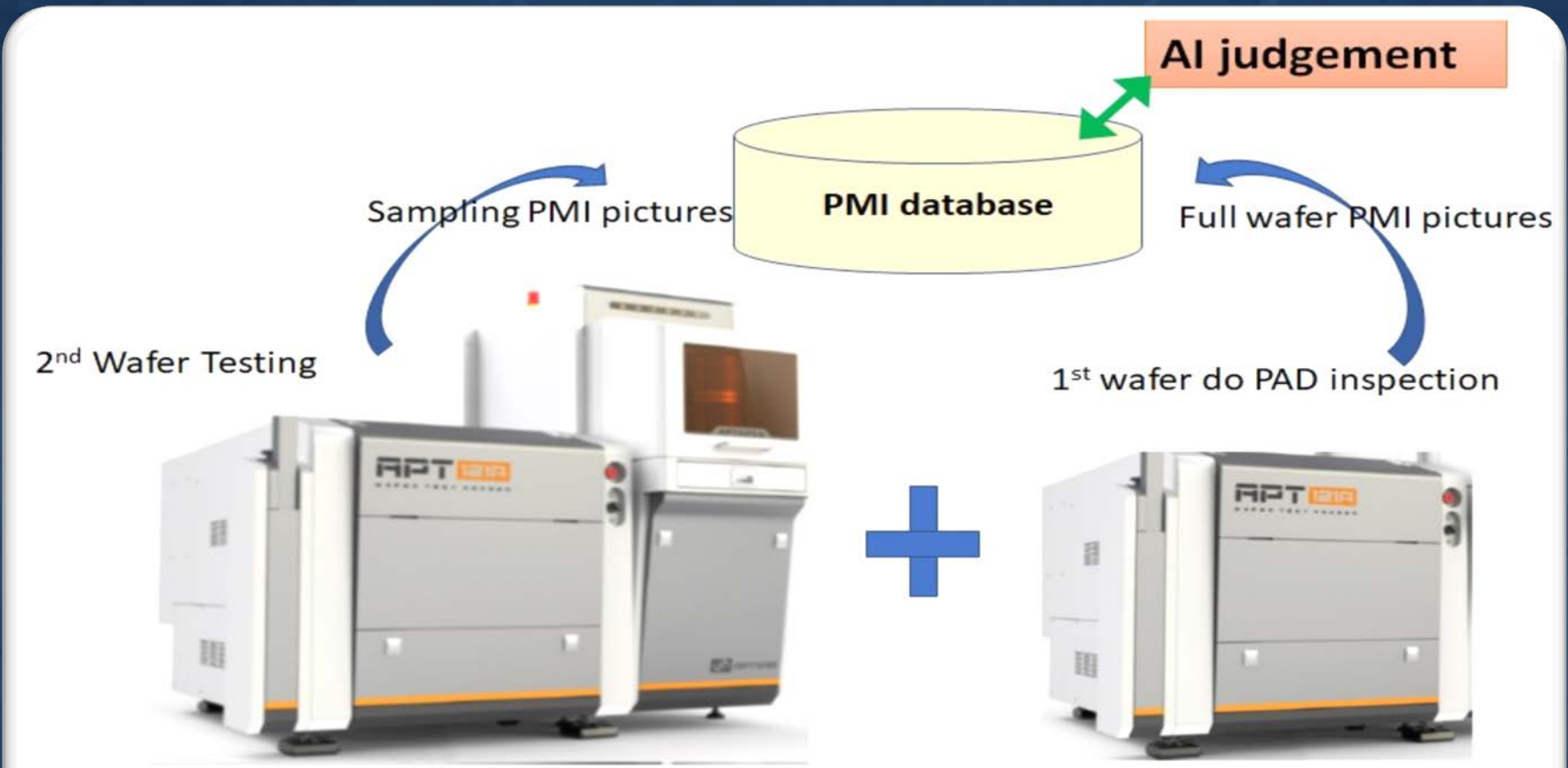


# Single Pin Shift Issue For High Pin Count Device





# On line PAD Inspection & Quality control

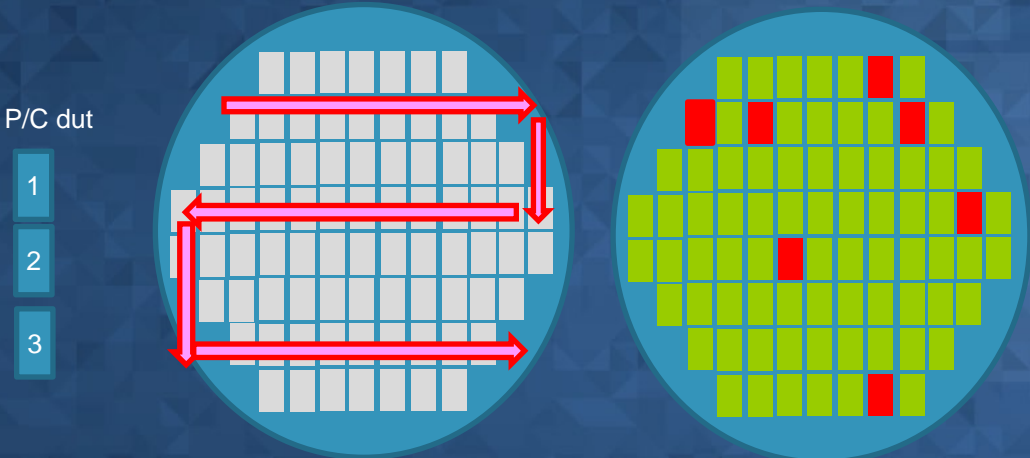


- 1. Two stage for probing quality control
- 2. Probe mark data base record
- 3. Need shift detection
- 4. Control wafer impact under two wafers

coming soon !!

# Smart on-line retest

- To replace the same dut retest the same fail die
- To enhance final yield



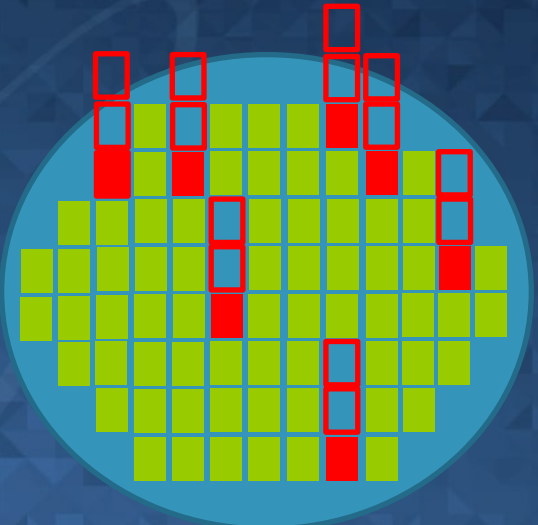
1<sup>st</sup> test yield :  $73/80 = 91.25\%$

Dut1 yield =  $27/29 = 93.10\%$

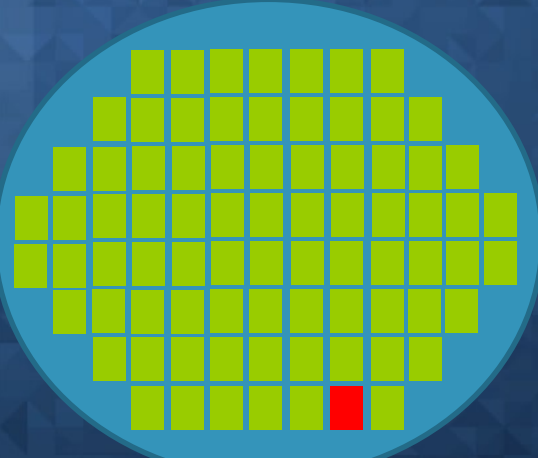
Dut2 yield =  $24/29 = 82.76\%$

**Dut3 yield =  $22/22 = 100\%$**

dut1  
dut2  
dut3  
dut1  
dut2  
dut3  
dut1  
dut2



Take duts 3 to retest fail bin



Gain more yield than retest by original dut

Final test yield :  $79/80 = 98.75\%$

# EDA further integration in the future



## Testing data

Timing for data analysis will be from wafer end to during testing to make real time & dynamic monitor



## Prober log

For real time environment & condition check. Statistics for machine alarm ,efficiency & performance



## Probe Card Information

Make effective disposition when low yield or overkill occur. Real time monitor abrasion status of needle

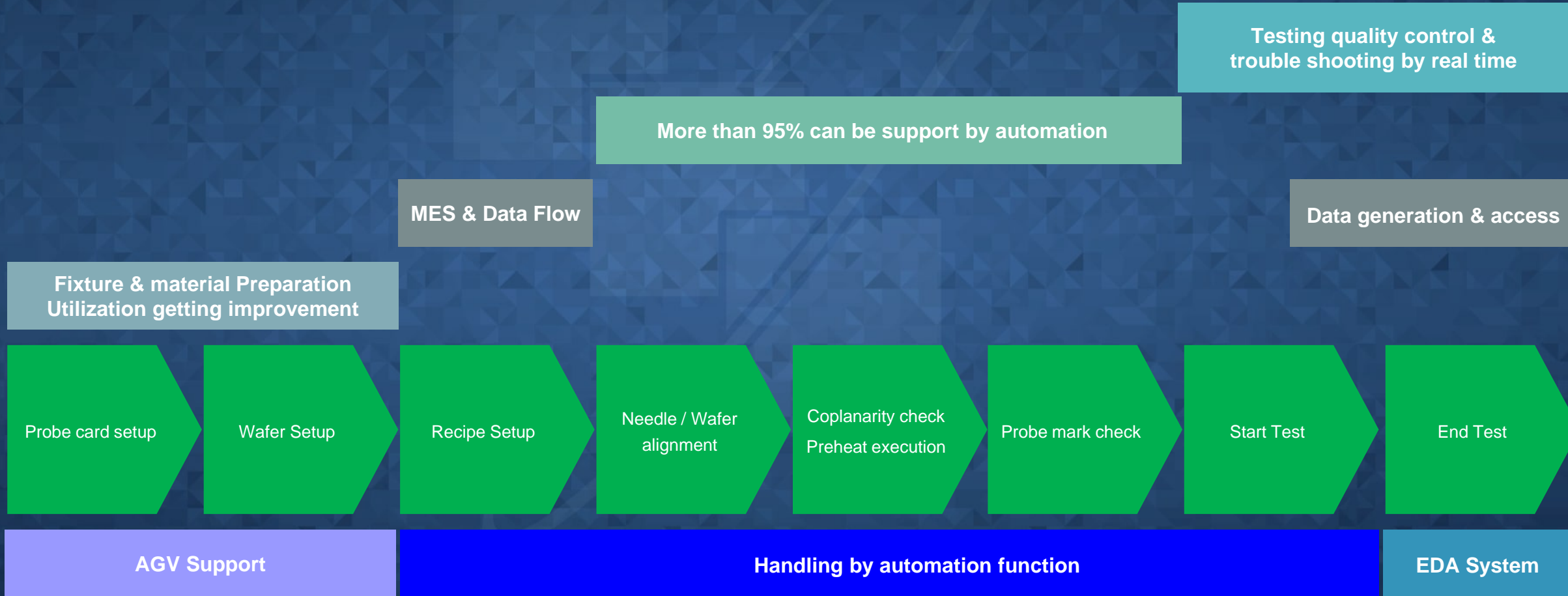


## AOI & PMI Data

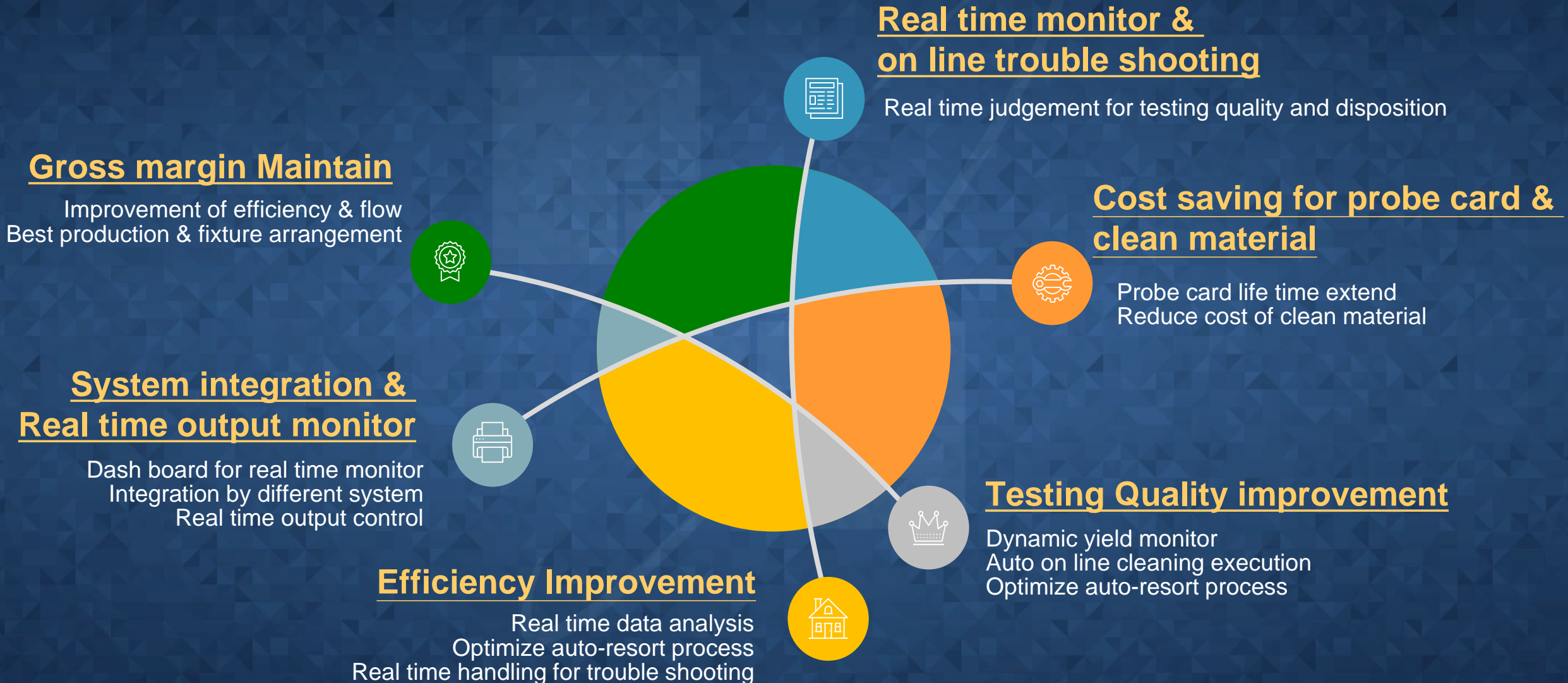
To make good quality for probe card needle & probe mark. More analysis for yield , parameter & probe mark.

# CP Testing Flow After System Integration

CP Testing Flow after system integration



# Benefit for system integration



# Conclusion

**With the shrinking of process and requirement of quality , how to maintain and improve testing efficiency & gross profit is the target of every testing factory. Integration of big data , IoT , AI , automation & unmanned handling technology with creative & reciprocal cooperation model will be the key technology to decide if testing house can put the strengths in the lead and provide the best service to customers.**

# Follow-On Work

- How to control data flow with edge computing
- Big data management & control (testing data, log , AOI & PMI data)
- Affordability of automated function
- More background job & analysis tool development

# Cooperation Partners

## ■ Jetbond Technology Co., LTD. :

Probe card storage & Automated Probe Card Trolley Service,  
AOI integrated solution , AI implement for bump analysis

Contact Window : Roden Hsu ([roden@jetbond.com.tw](mailto:roden@jetbond.com.tw))

## ■ Weilitech Technology Co., LTD. :

EDA system integration service (Testing data & Probe log) ,  
AI Algorithm for PMI support

Automated testing function development

Contact Window : Edward Jiang ([ed@weilitech.com.tw](mailto:ed@weilitech.com.tw))