SWTEST ASIA 2022

TestGeni - An Intelligent Automation Tool for ATE Engineers

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Introduction

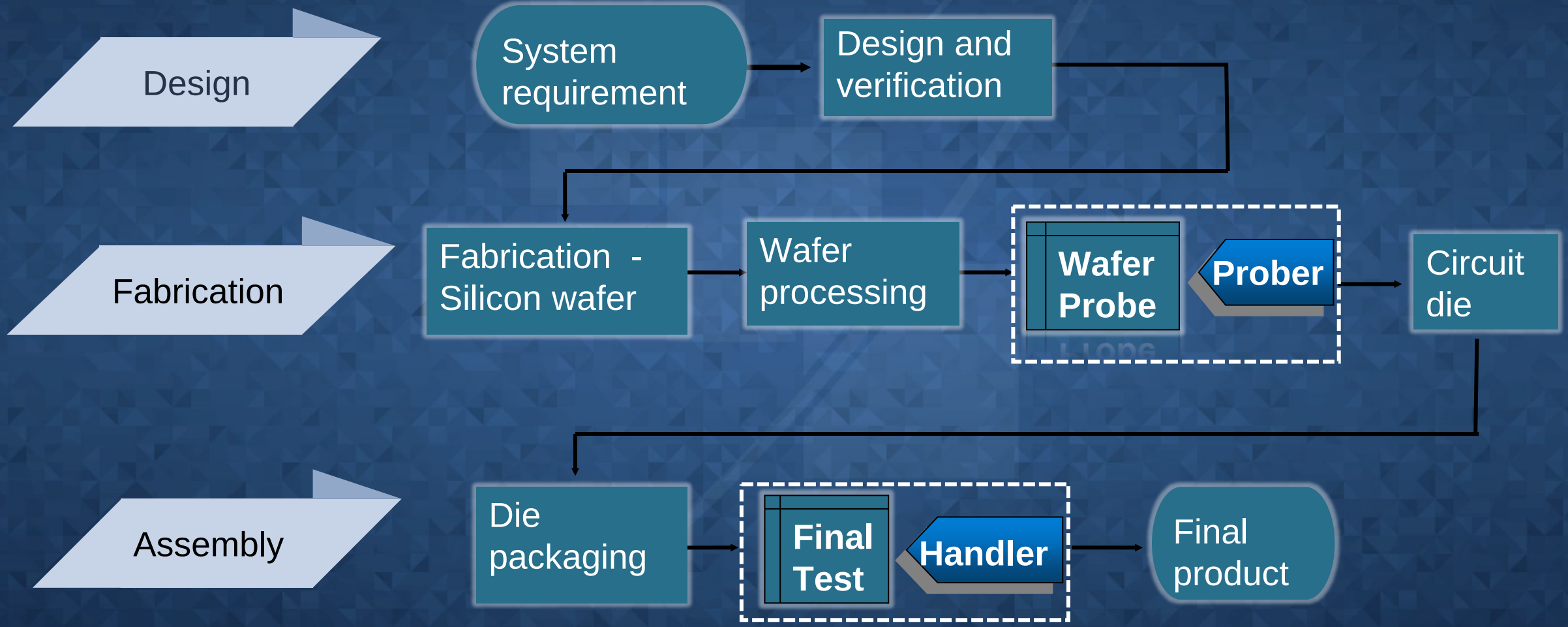
Time is money in semiconductor industry

One of the biggest challenges of post silicon validation is time reduction in program development and testing

Automation: An intelligent solution reducing the manual efforts

Caliber intends to provide the best possible automation in test program generation even in the absence of tester tool

Post silicon validation in IC manufacture cycle



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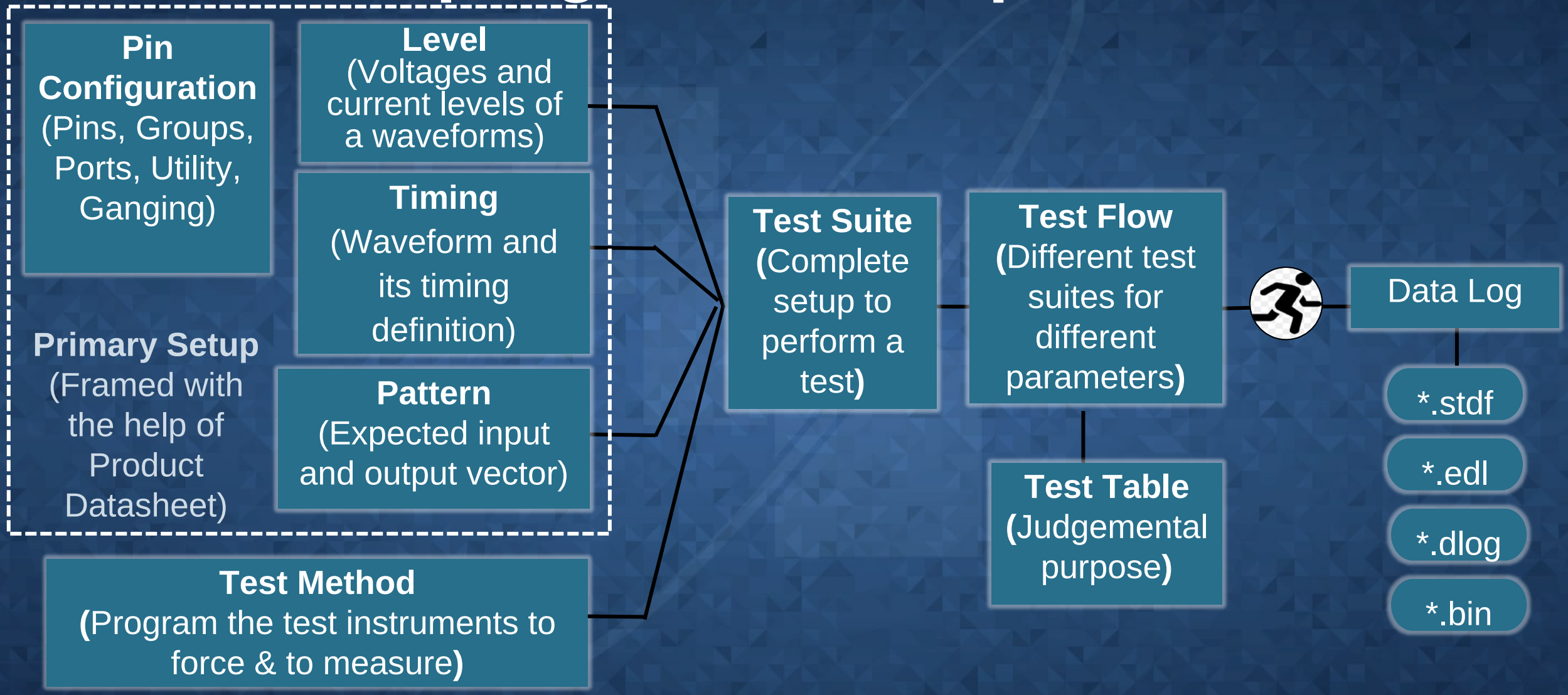
Basic program development flow



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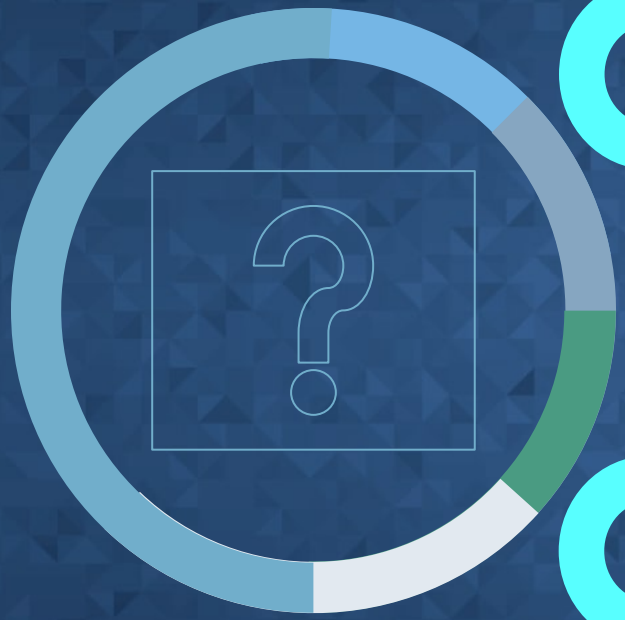
Why TestGeni?



- Quick generation of primary setup files
- Huge vector generation, i.e., fault detecting algorithms for memory chip testing
- Legacy tester pattern conversion to desired tester platform conversion
- Cross portability in production, characterization and debug test flow
- Analysis of data log and generation of user defined(Textual & Visual) formats

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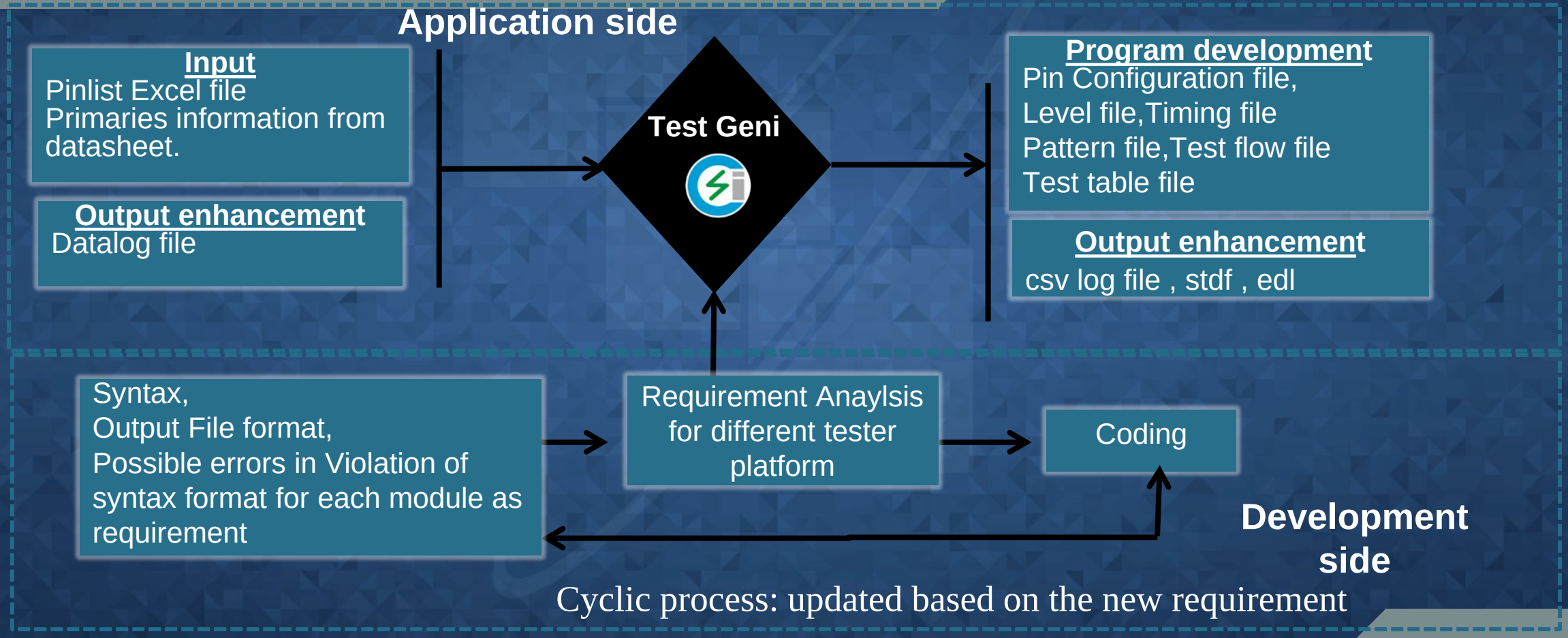
Prototype model of TestGeni

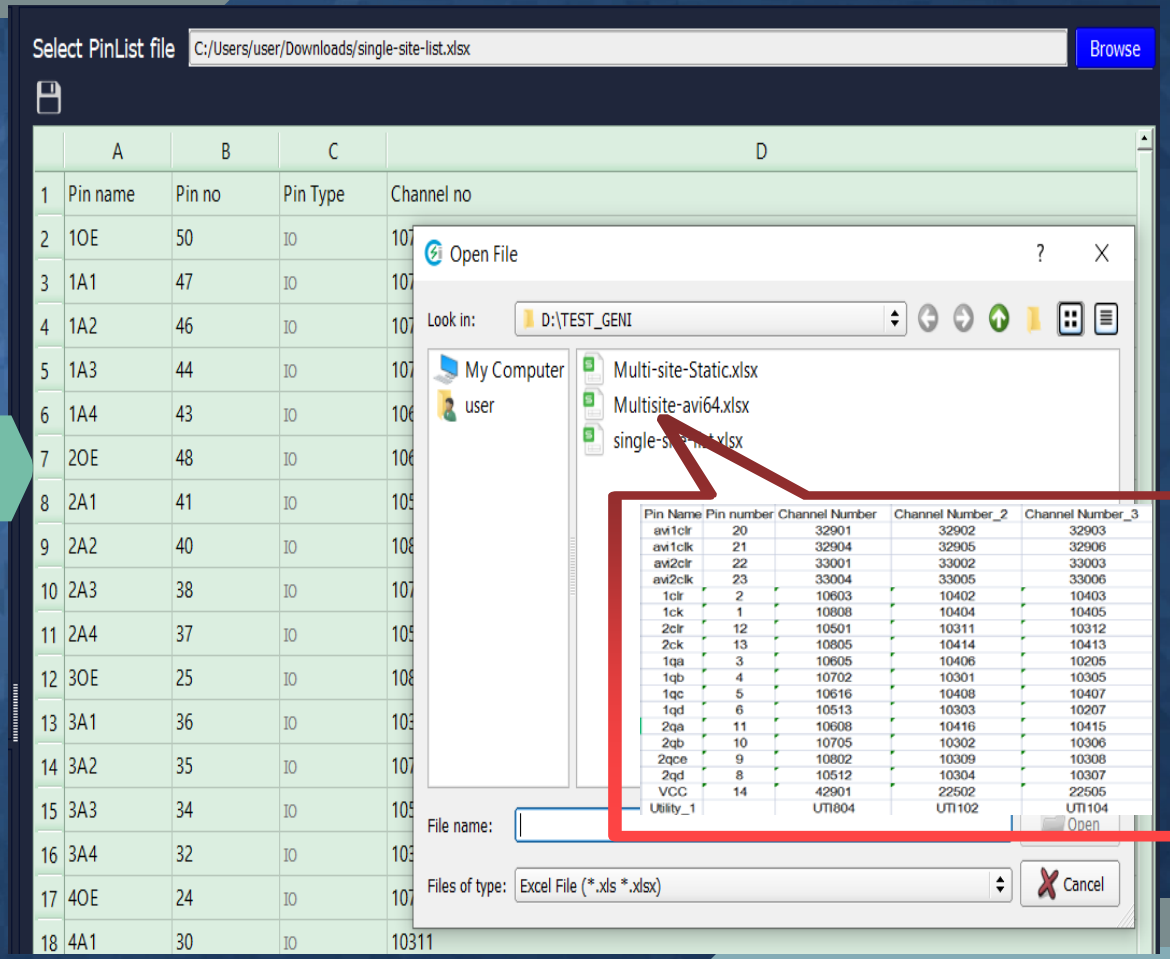


Automation: Primaries development

Converts excel file into a loadable pin config file supported by tester tool

Time reduction in feeding pins for primary setup file

Customizable with any kind of pin-info to tester compatible pin config



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Automation: Primaries development

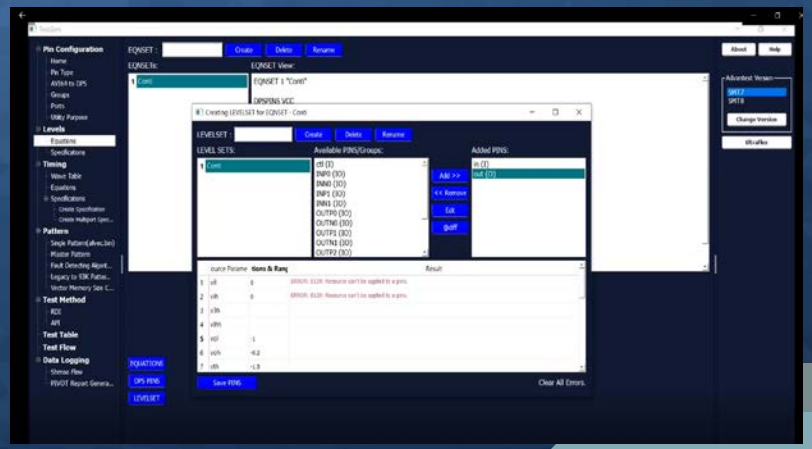
User friendly GUI interface in generating primaries and avoids the manual syntax errors

Reduces time in test program development

Supports multiple tester platform

```
EQNSET 1 "LEV_EQUNSET_CONT_DPSSHORT_01"
SPECS
     VCC [V]
     VIL [V]
     VIH [V]
     VOL [V]
     VOH [V]
     IOL [mA]
     IOH [mA]
     VT [V]
DPSPINS VCC
vout= VCC
vout_frc_rng=7
iout_clamp_rng=500
ilimit=500
t_ms=4
offcurr=act
#connect_state= UNGANG
LEVELSET 1 "LEVSET1_CONT"
PINS cont_pins

vil=VIL
vih=VIH
vol=VOL
voh=VOH
vt=VT
iol=IOL
ioh=IOH
```



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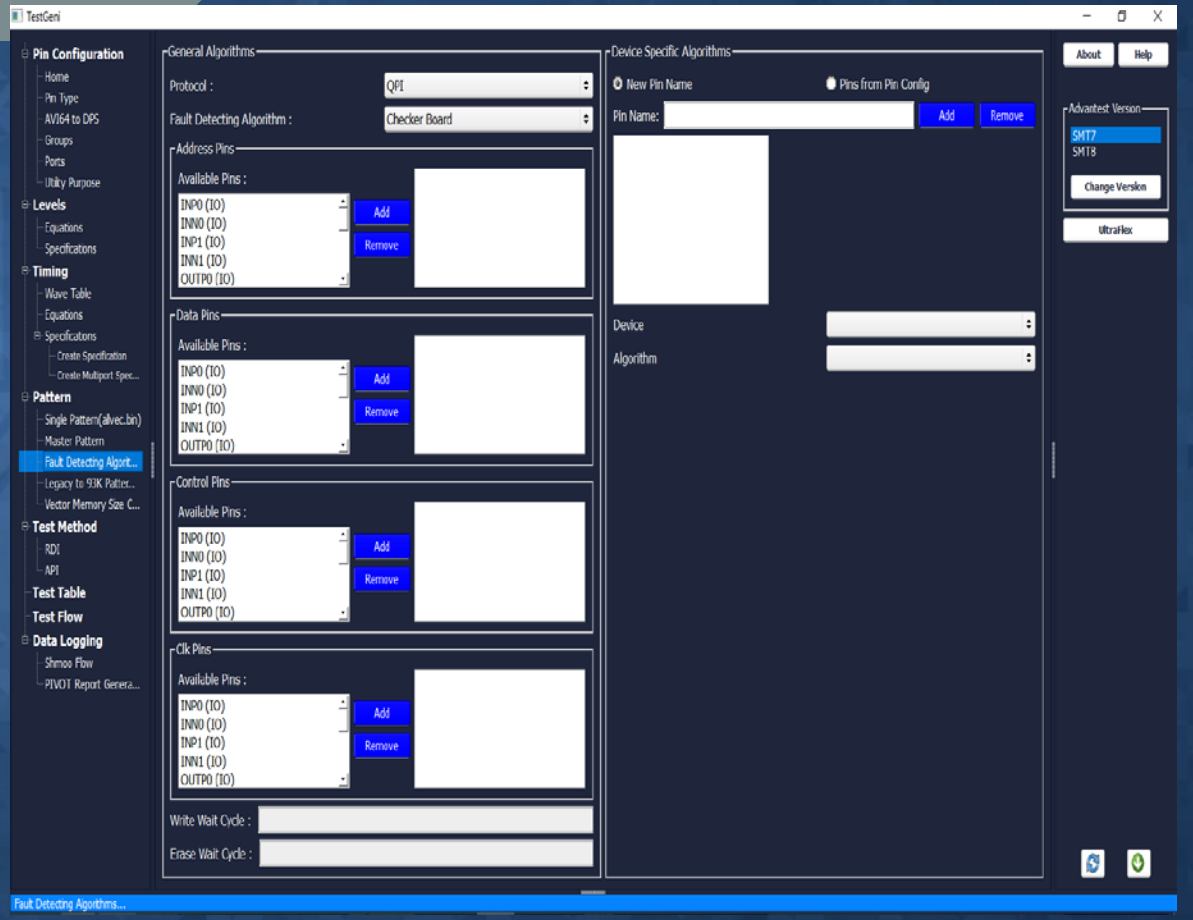
Vector generation

Easy generation of huge vectors with the help of algorithms.

Incorporation of protocol based pre-defined fault coverage algorithms.

Vector generation for NOR, NAND Flash memory device specific algorithms



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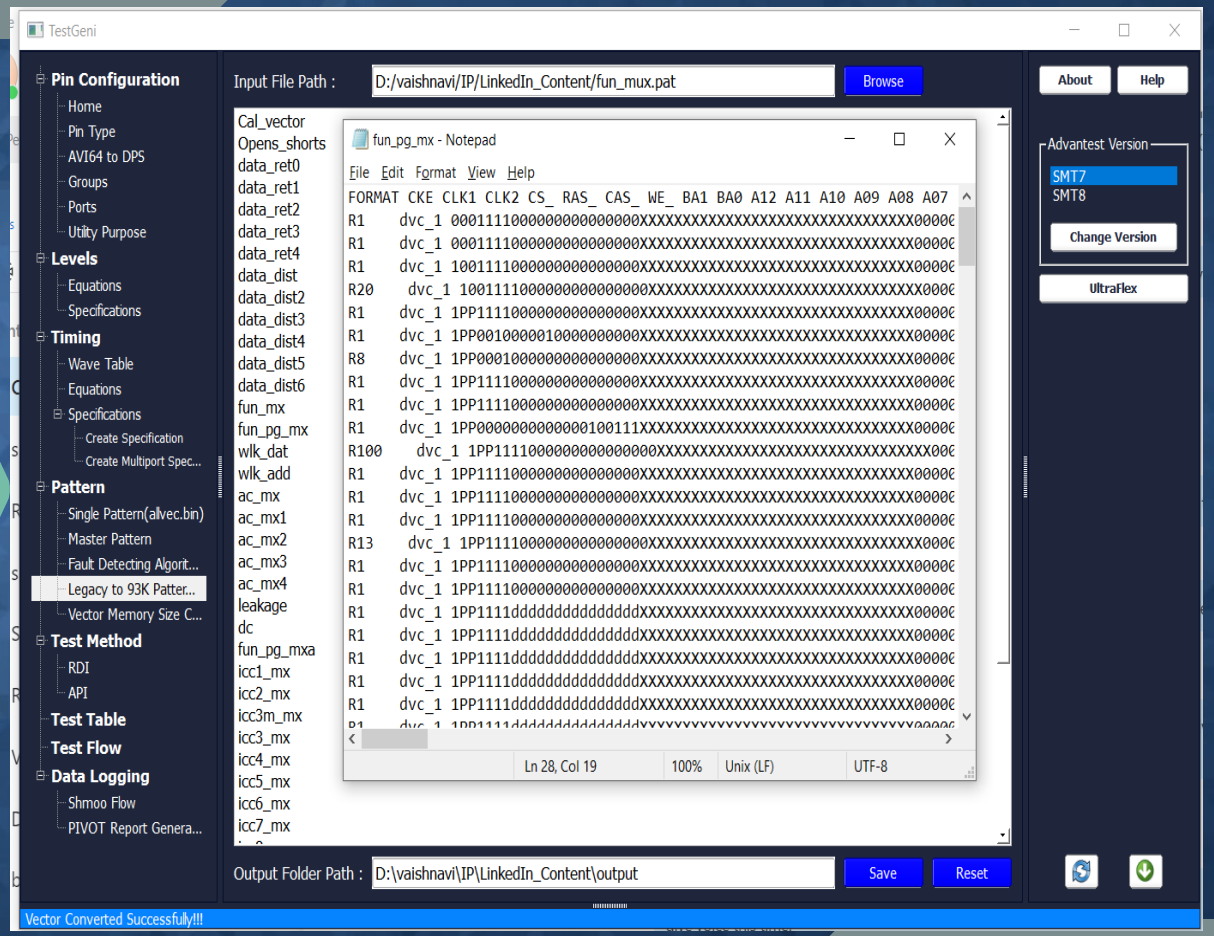
Expeditious pattern conversion

Legacy tester pattern to desired tester pattern conversion

Sample conversion from a legacy tester platform to V93000-SM7 patterns

Swift conversion in a single click



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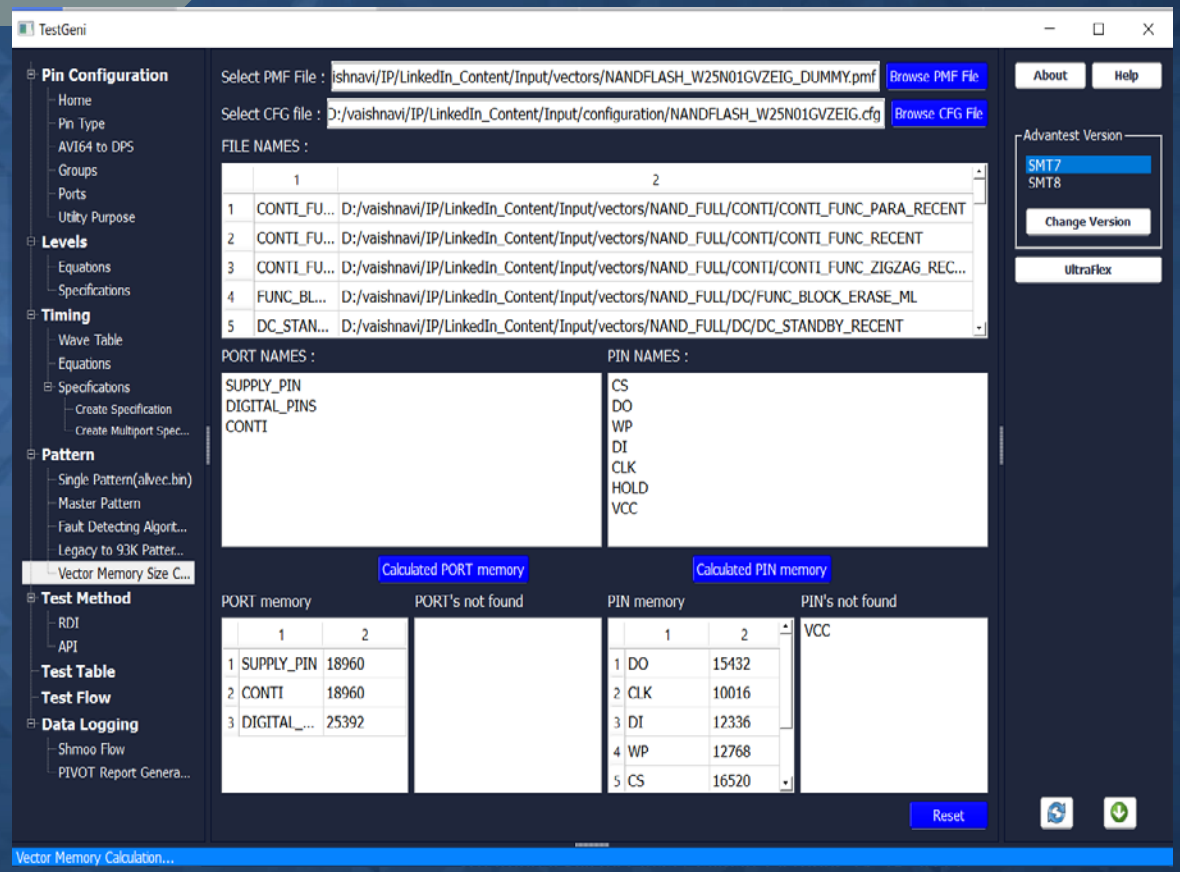
Vector memory size calculator

Firmware commands are essential to find the size of vector memory.

TestGeni facilitates user friendly GUI interface with vector and configuration file

Selected pin, port, vector wise memory size calculation



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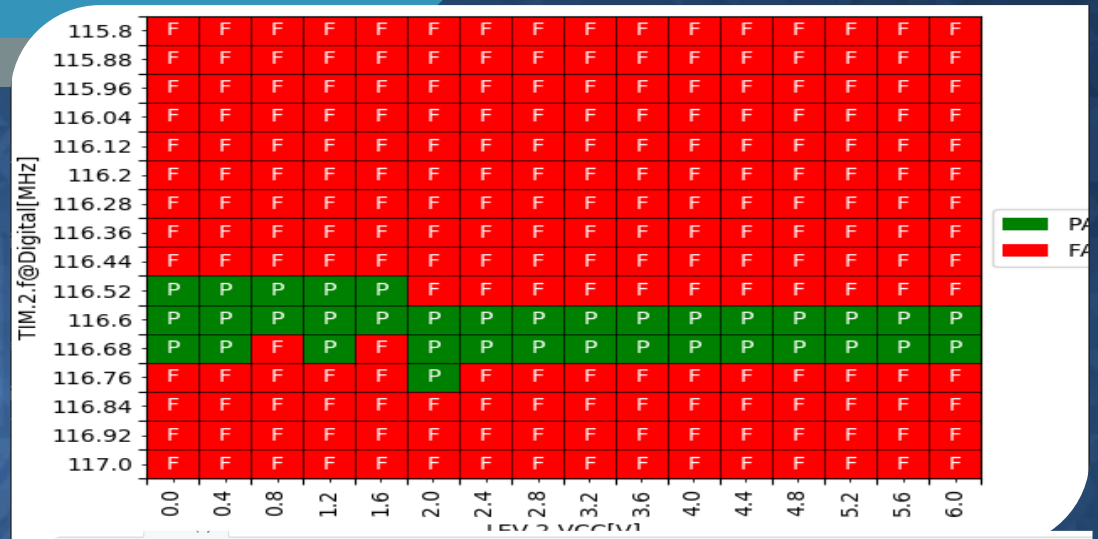
Datalogging

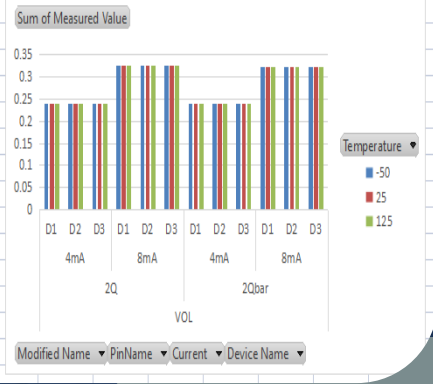
Converting stdf file into an expansive csv file with easily accessible and organised parametrics

Data and test time crunching for quick reporting

Shmoo plot generation from datalog file



	A	B	C	D	E	F	G
1	Sum of Measured Value				Temperature		
2	Modified Nam	PinName	Current	Device Name	-50	25	125
3	VOL	2Q	4mA	D1	0.240437999	0.240723997	0.240495995
4				D2	0.240381002	0.240437999	0.240324005
5				D3	0.240266994	0.240266994	0.240324005
6			8mA	D1	0.324445993	0.324788988	0.324503005
7				D2	0.324445993	0.324503005	0.324503005
8				D3	0.324389011	0.324389011	0.324389011
9		2Qbar	4mA	D1	0.239464998	0.239693999	0.239464998
10				D2	0.239408001	0.239464998	0.239351004
11				D3	0.239408001	0.239294007	0.239351004
12			8mA	D1	0.321184009	0.321298003	0.321240991
13				D2	0.321126997	0.321126997	0.321069986
14				D3	0.321184009	0.321184009	0.321126997



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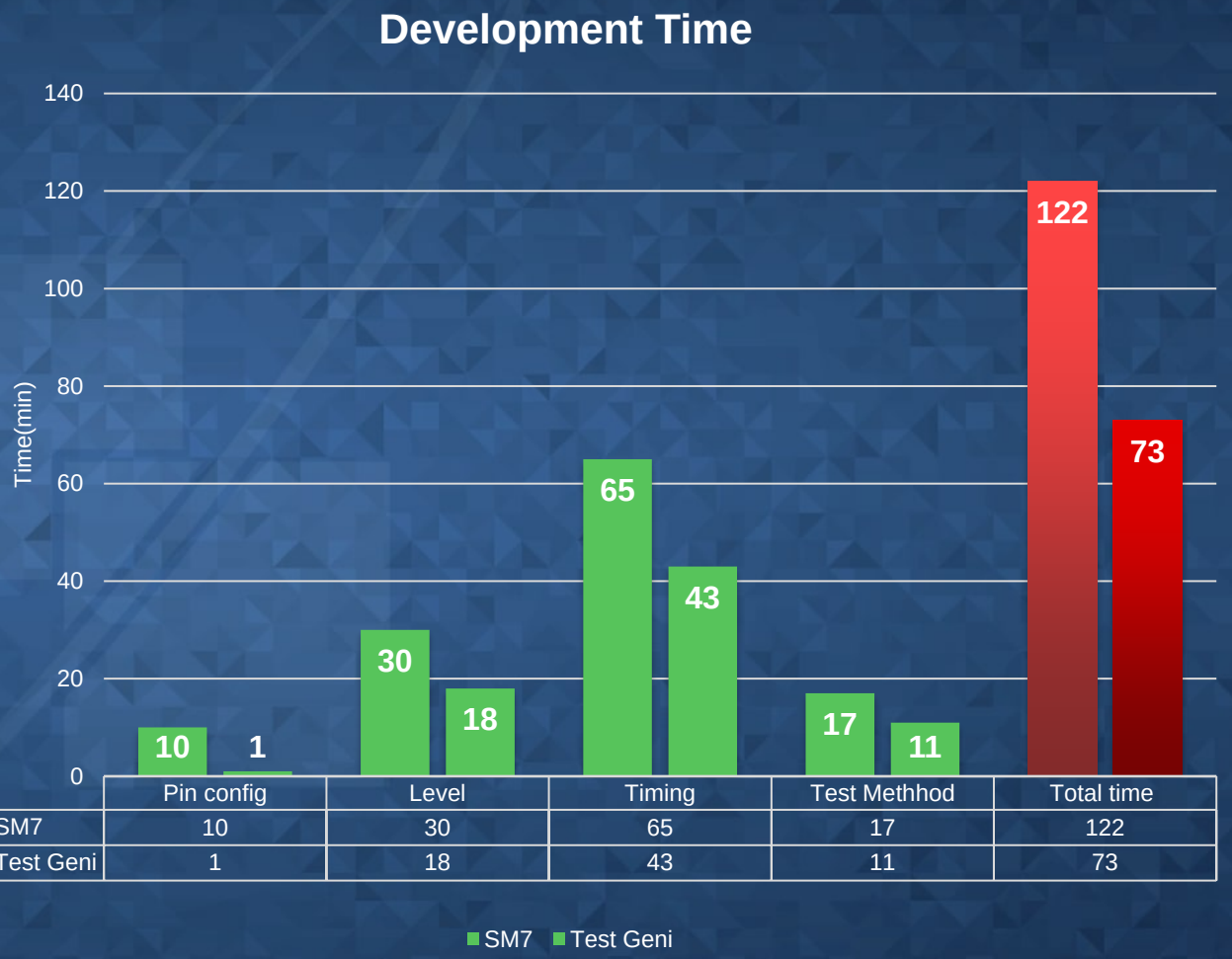
On Target

Use case

- ✓ Real time product: Digital ASIC
- ✓ Tester platform: Advantest 93k
- ✓ Version : SM7
- ✓ Test program development is implemented in both tester tool and TestGeni.
- ✓ Approximately 41.6% of time is saved using TestGeni



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Conclusion and future work

- TestGeni helps in possible automation needed for test program development and analyses the test data which reduces the man hours
- Incorporating new tester platforms for portability and other advanced features is in progress to reduce the development time further

Q & A