SWTEST ASIA 2022

Known Good Die Memory Wafter Test Challenge Beyond DDR5 4GHz/8Gbps Speed

FormFactor™

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Agenda

- **Raising Demand of Testing on Advanced Packaging**
  - Advanced packaging market overview and trends
  - HBM package yield case study
  - KGDS Tester Insertions/Options in HBM manufacturing flow
- **KGDS test requirements challenge probe card design**
  - Probe Card solutions on different KDG test application
  - Recap 3.2GHz probe card solution
  - Simulation vs. Measurement Result for 4.0GHz probe card solution
- **Feature Development Direction and Acknowledgement**
  - Conclusion, feature development and acknowledgement

Advanced Packaging Demand Drive Testing Demand

- **Advanced Packaging Demand Taking-off**
  - Revenue Growth in CAGR 6.6% (2014~2025)
  - Beyond 2025 50% of IC are forecasted to be Advanced Package
- **Advanced Packaging Complexity Trend**
  - From simple SoC + HBM to multiple SoC + multiple HBM
  - HBM DRAM stack increased
  - Package size growing
- **DRAM KGDS Test Help Reduce Risk and Cost on Advanced Packaging/HBM**
  - Higher complexity → lower yield
  - Higher complexity → higher packaging cost
  - Earlier defect detection help save package cost

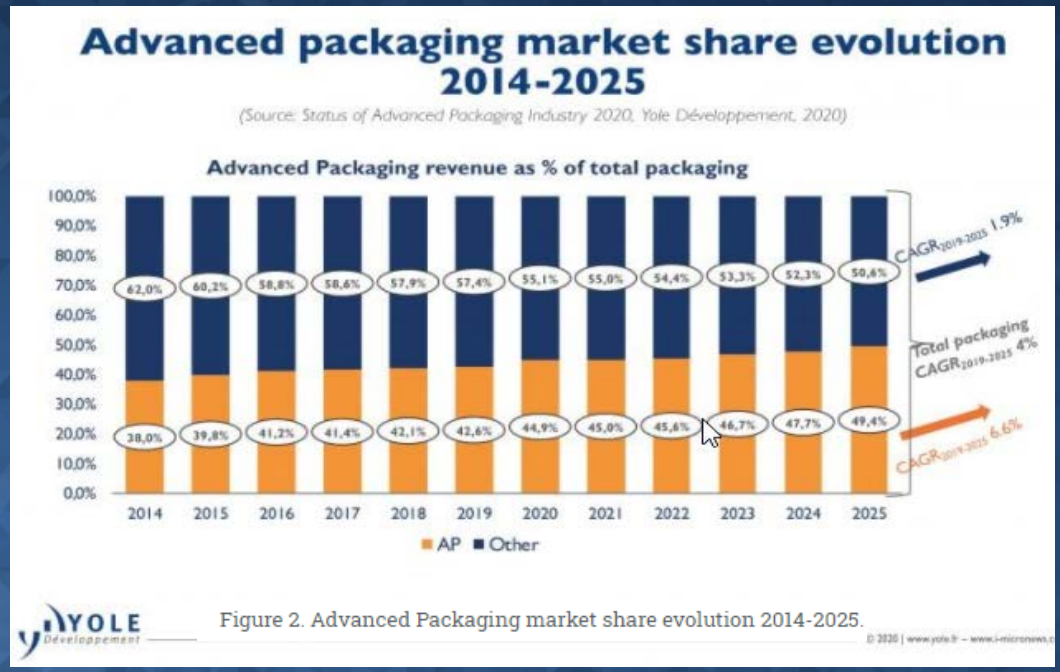
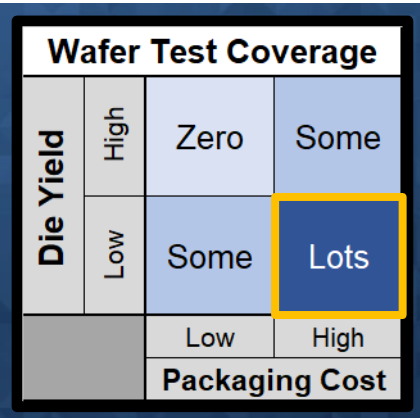


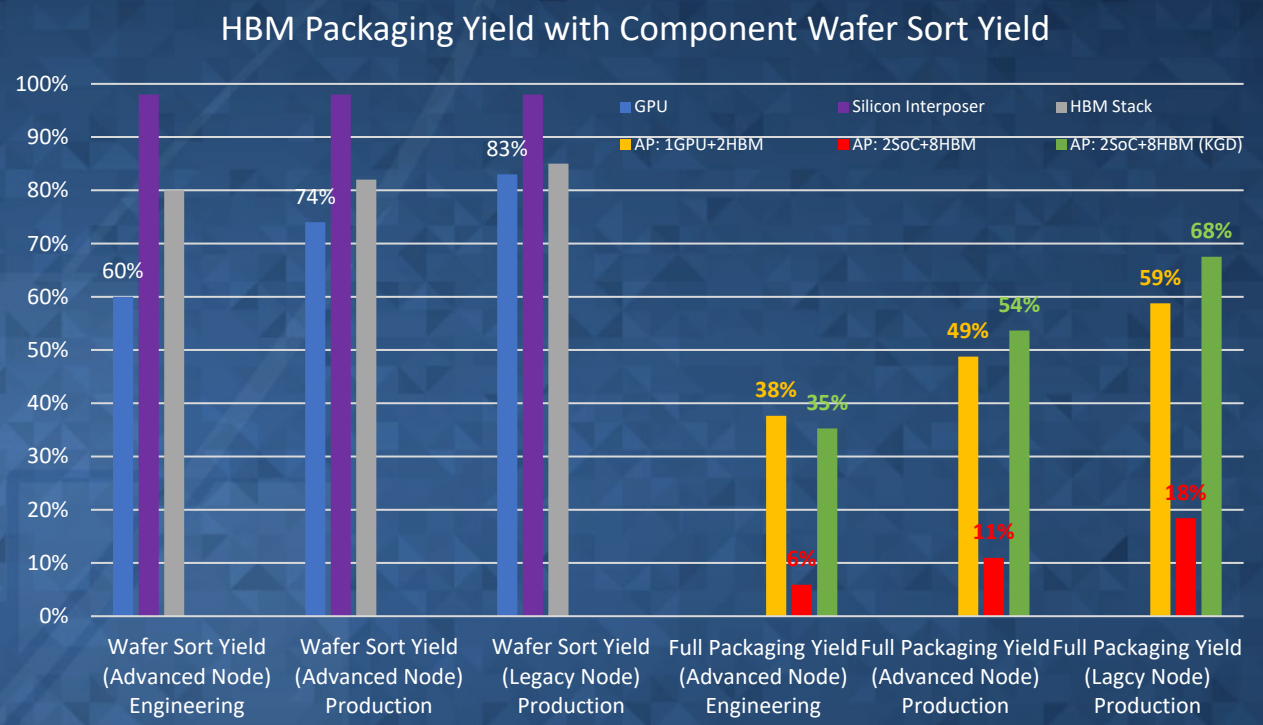
Figure 2. Advanced Packaging market share evolution 2014-2025.

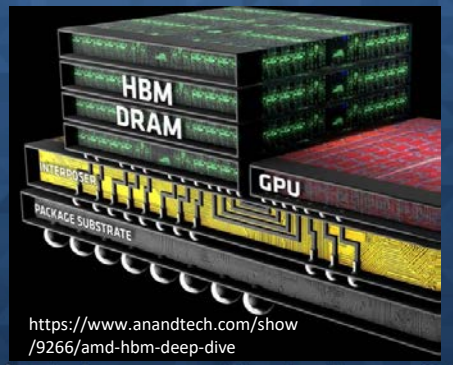


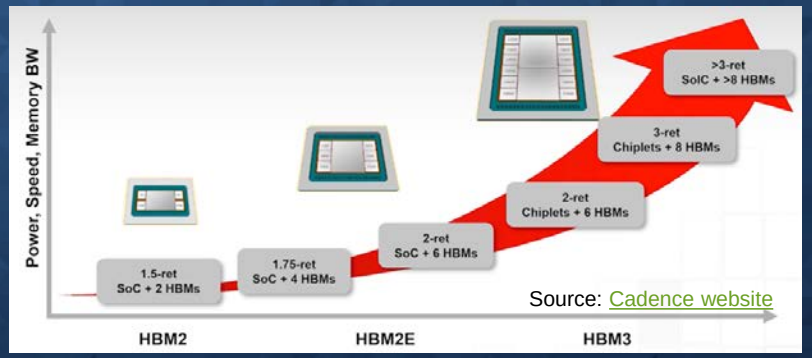
https://www.swtest.org/swtw_library/2020proc/pdf/00pm_SWTest_Untethered_Keynote_Slessor_FormFactor.pdf

Advanced Packaging Yield Case Study

- **Assumptions on High Bandwidth Memory Case:**
  - GPU yield: 60%~85% (depends on device and tech node)
  - Silicon Interposer: ~98% (pretty good)
  - HBM stack yield: 80%~85% (depends on device and tech node)
- **What about 2 SoC + 8 HBM**
  - Yield drop down to >20%
- **What about with KGS HBM**
  - Yield improve dramatically by KGS HBM



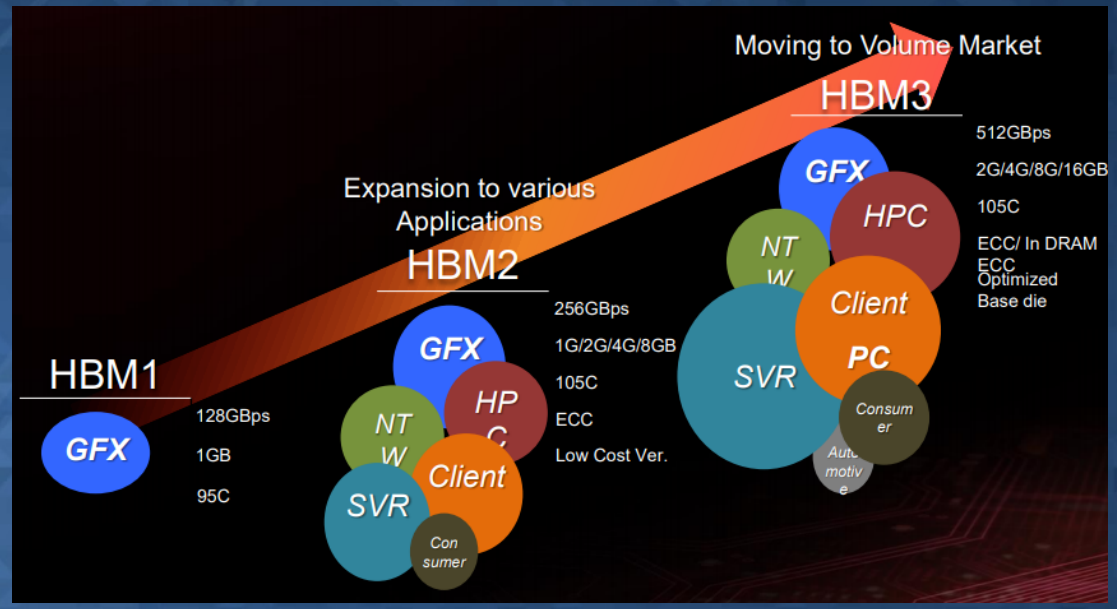




HBM and DRAM Data Rate Spec Drives KGD Test Requirement

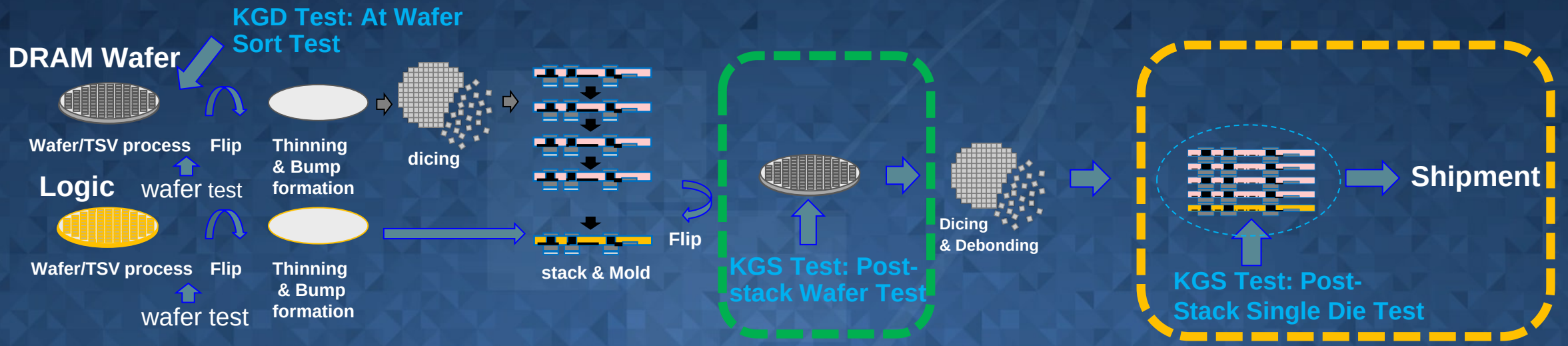
- **HBM Application Expands to Broader Market**
  - From Graphic to Server, AI, Automotive, HPC
- **HBM to HBM3 Performance Enhancement**
  - Faster data rate speed
  - Higher memory bandwidth
  - Wider temperature range
- **KGD Test Requirements, PC Challenges**
  - Probe Card speed requirement from 1.6GHz to >3GHz
  - Temperature range from -40~125C to -40~150C
  - Test efficiency to meet high volume production

	DDR4	LPDDR4(X)	GDDR6	HBM2	HBM2E (JEDEC)	HBM3 (TBD)
Data rate	3200Mbps	3200Mbps (up to 4266 Mbps)	14Gbps (up to 16Gb ps)	2.4Gbps	2.8Gbps	>3.2Gbps (TBD)
Pin count	x4/x8/x16	x16/ch (2ch per die)	x16/x32	x1024	x1024	x1024
Bandwidth	5.4GB/s	12.8(17)GB/s	56GB/s	307GB/s	358GB/s	>500GB/s
Density (per package)	4Gb/8Gb	8Gb/16Gb/2 4Gb/32Gb	8Gb/16Gb	4GB/8GB	8GB/16GB	8GB/16GB/ 24GB (TBD)



Source: SK Hynix Presentation “An In-depth Study of High Bandwidth Memory”

Choices of Known Good Die/Stack Test in HBM Manufacturing Flow



	Option 1 (Known Good Die Test)	Option 2 (Known Good Stack Wafer Test)	Option 3 (Known Good Stack Single Die Test)
Where to Test in the HBM Flow:	DRAM Wafer Sort	DRAM Wafer Post Stacking	DRAM Stack Die Post Dicing
Probing Interface:	Pad on DRAM Die	Sacrifical PAD in HBM Bump Array	HBM Micro-Bumps
Probe Card Technology:	DRAM HFTAP Probe Card	DRAM HFTAP Probe Card	Vertical MEMS Probe Card
Advantage:	Probing recipe and probe card technology similar to wafer sort test. Earliest detection in HBM Mfg flow	Known good stack result Relatively cost effective solution (high test efficiency and good enough coverage)	Full test coverage, truly known good stack
Challenges:	Known good die only, not able to detect defects during wafer stack	Test strategy and DFT build to die design to get good enough coverage Probing recipe optimization for wafer stack and CTE management on composition material	HBM2 bump pitch and signal count challenge space transformer fan out (high cost) Probing recipe develop on single die stack handling

https://www.swtest.org/swtw_library/2021proc/pdf/w04_01_liao_swtest_2021.pdf

https://www.swtest.org/swtw_library/2017proc/PDF/S09_01_Nhin_SWTW2017R2.pdf

Probe Card Solutions: KDS HBM2, KGD LPDDR4, KGD NAND

KGD LPDDR4 Probe Card

Max 128DUTs, 45TD, T11.2P (-40~150°C)

Target Speed 3.2GHz

Advantest T5503 WMB2 HS2

KGD DDR5 Probe Card

Max 80DUTs, 10TD, T11.2P (-40~150°C)

Target Speed **4GHz**

Advantest T5503 HS2

KGS LPDDR4 Probe Card

Max 128DUTs, 45TD, T11.2P (-40~150°C)

Target Speed 3.2GHz

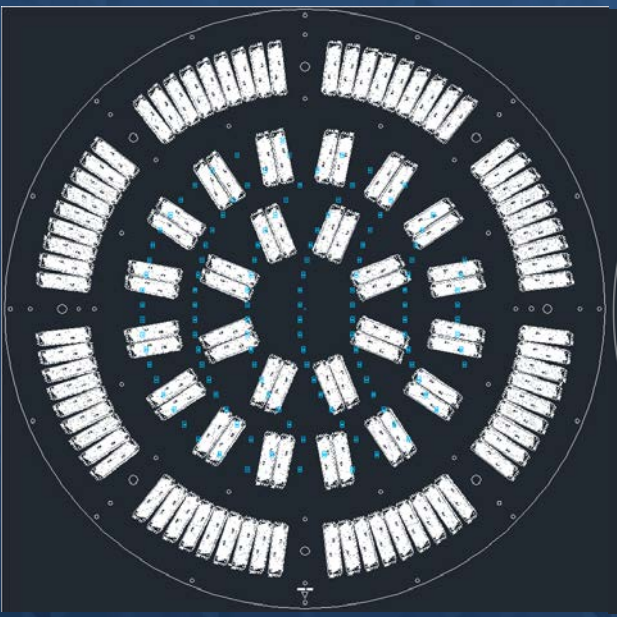
Advantest T5503 HS2

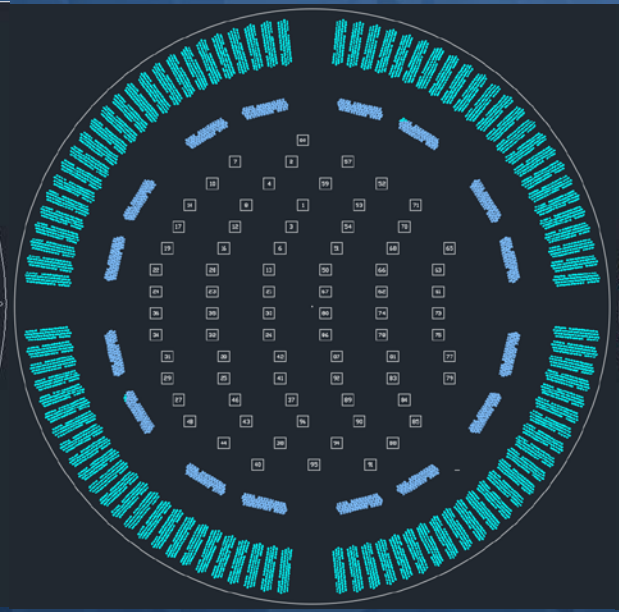
KGD NAND Probe Card

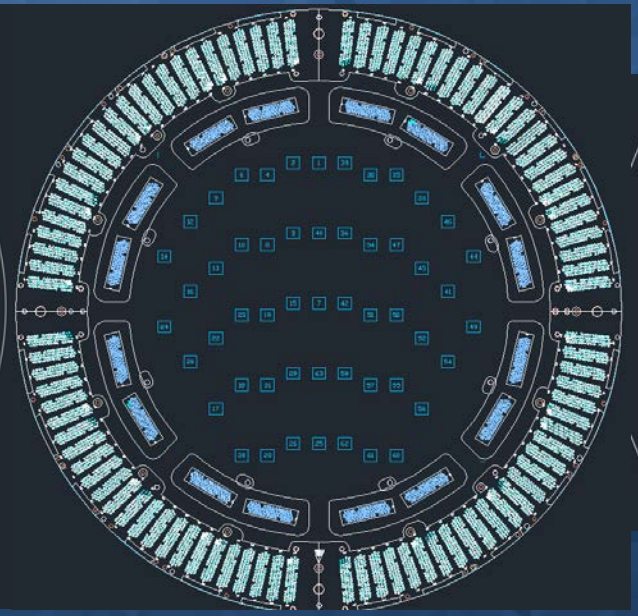
Max 64DUTs, 45TD, T11.2P (-40~150°C)

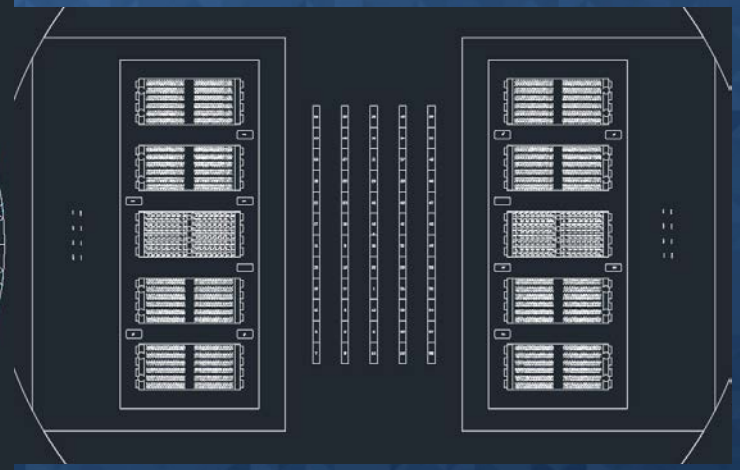
Target Speed **4GHz**

Teradyne Epic









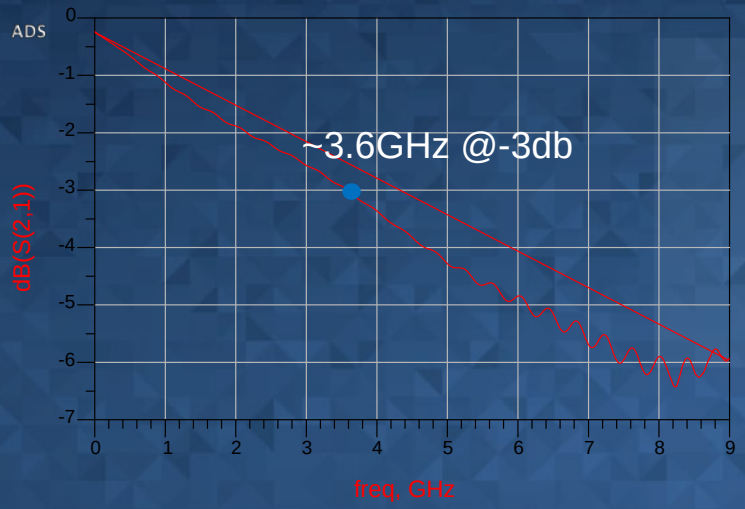
FFI KGDS Probe Card Design Experience: Design & Actual Correlated

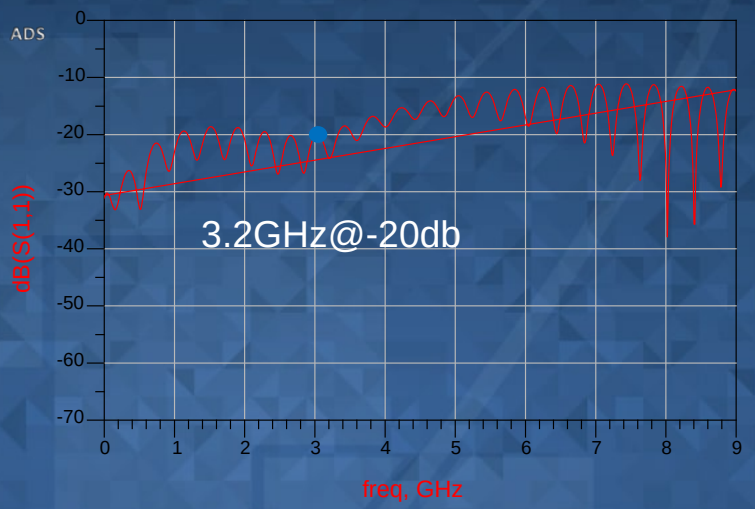
Insertion Loss

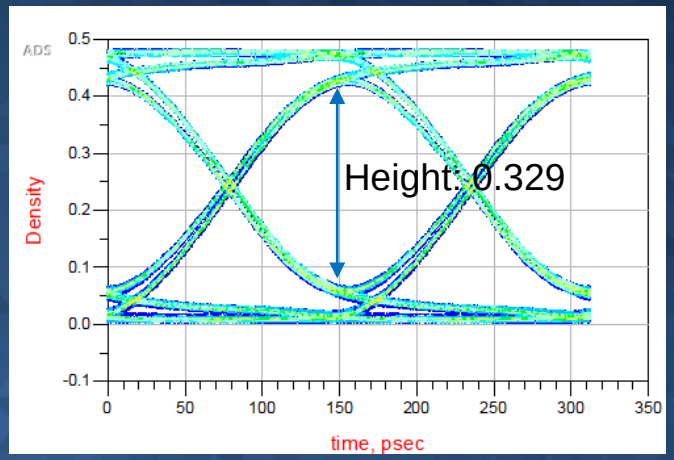
Return Loss

Eye-Diagram
Assume 50ohm on die termination
Prefect Input Signal

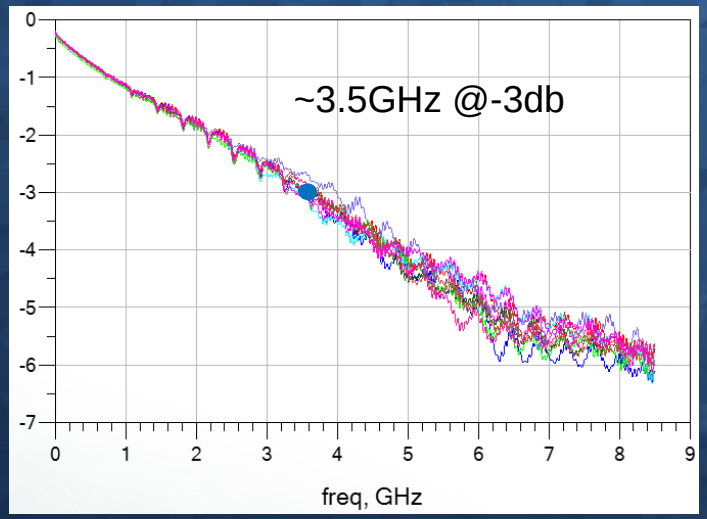
Design Simulation

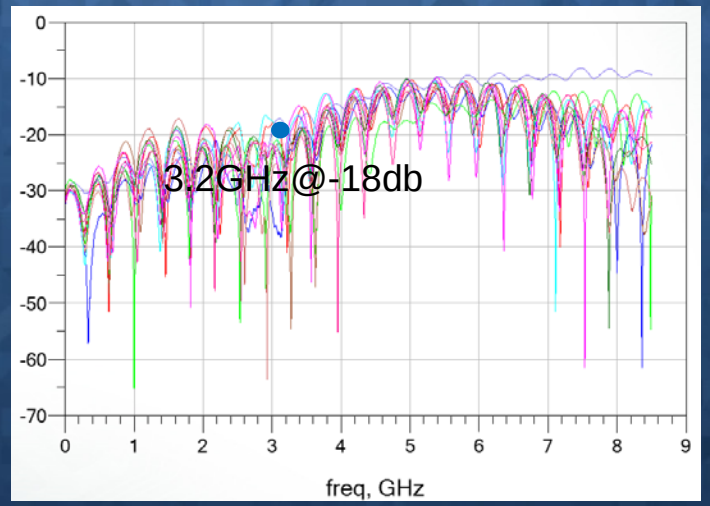


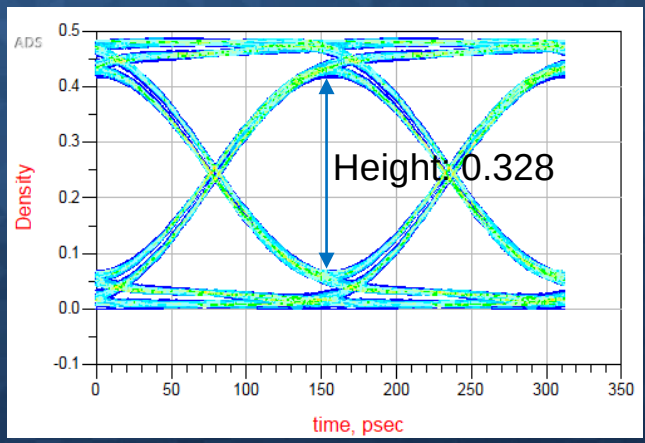




Outgoing Measurement



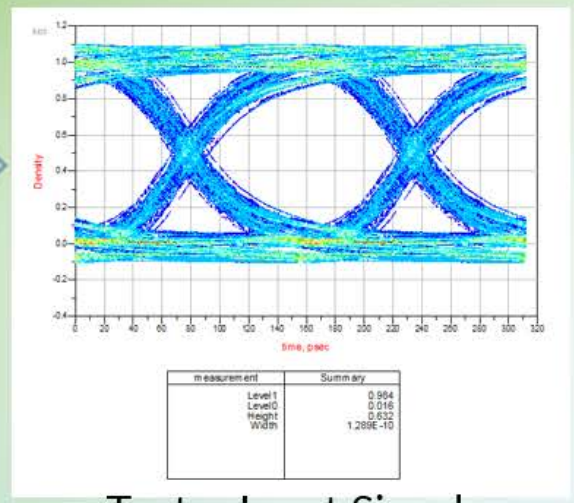




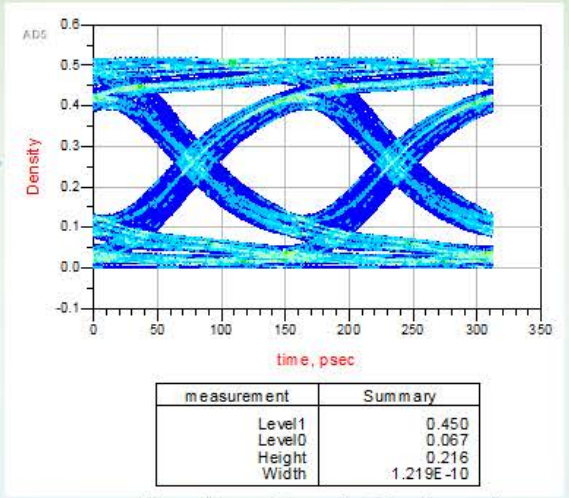
FFI HFTAP K32 (3.2GHz) Performance Presented on SWTW

LPDDR4 Probe Card D-Eye SHMOO Conclusion

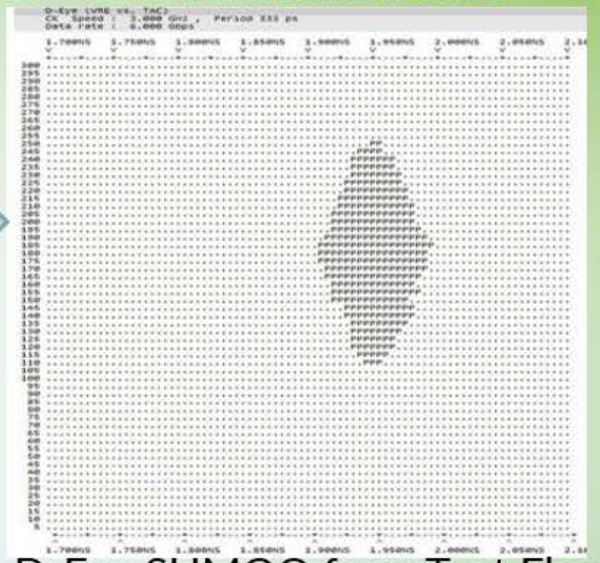
Perfect Input Signal



Tester Input Signal
Simulation 3.2GHz



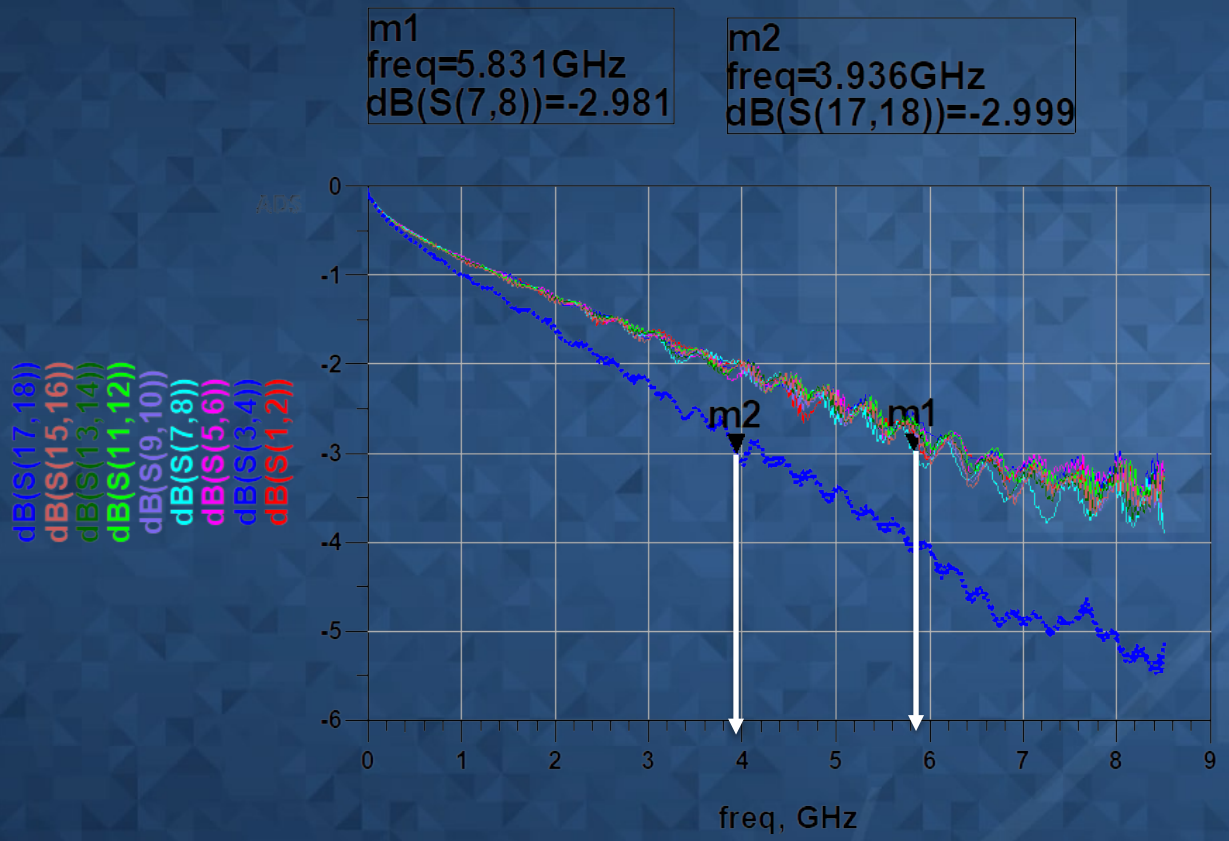
Probe Card Output
Simulation 3.2GHz



D-Eye SHMOO from Test Floor
3.0GHz Data Rate Test Pattern

- FFI simulation considered tester and probe card signal degradation
- Simulation considers ideal case (no crosstalk noise and power/GND noise)
- Simulation shows 43% eye height, confirmed by SHMOO plot and test floor data, performance reach 90~95% to the simulation result.
- Both simulation and actual test result show FFI K32 probe card capable for >3GHz test speed, correlate between design simulation and test result

FFI Improved Probe Card Speed Performance Beyond 4GHz Specification

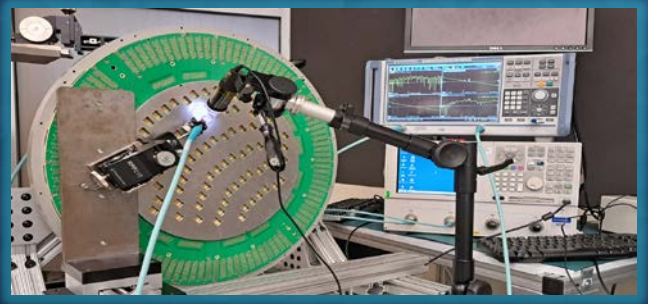


M1: PCB design with Advanced Design Rule
M2: PCB design with HFTAP K32 Design Rule

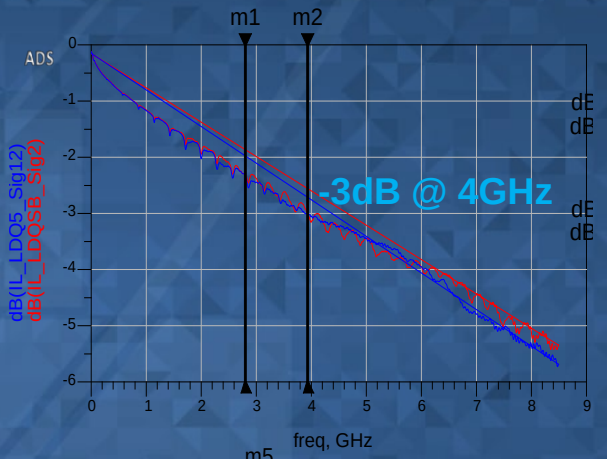
- **FFI PCB Design Measurement Result Show There is Path for Probe Card Support >5GHz KGDS Test Requirement**
  - Multiple signal channel PCB only simulation
  - With advanced design rule (for HFTAP K40 and K50 product)
  - Existing tester configuration
  - With PCB high speed material and manufacturing rule
  - -3dB bandwidth improve by 1.9GHz

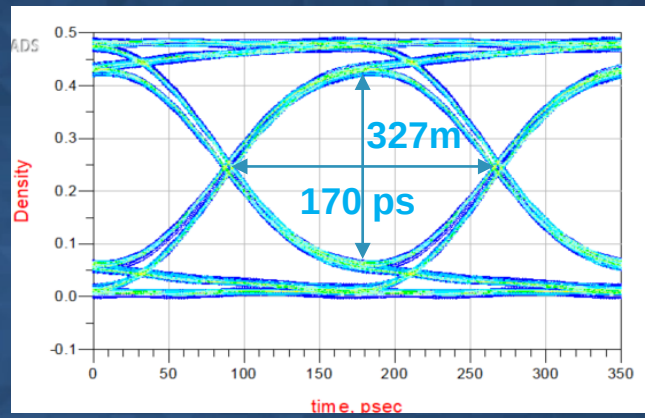
DDR5 KGD 4GHz Probe Card Performance

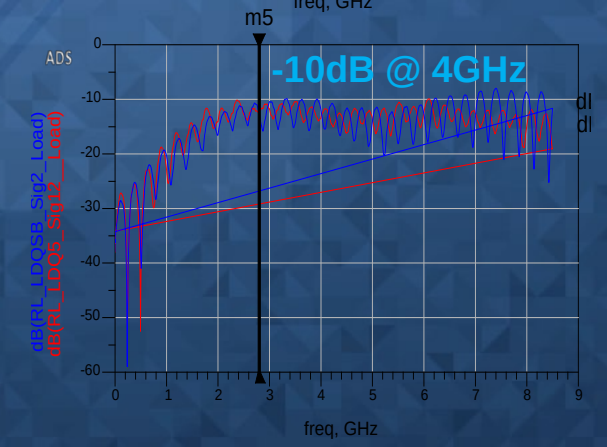
- **Probe Card Parameters:**
  - Total ~80 DUTs, 15K Probe Count
  - Dual temp -40 to 125°C
  - Customer test at 2.8GHz but require 4.0GHz capability
- **Probe Card Performance**
  - K40 advanced PCB routing rule applied
  - Insertion lost: -3dB at 4GHz
  - Eye opening: 170ps, height 327m
  - Voltage Amplitude: >78% of input signal

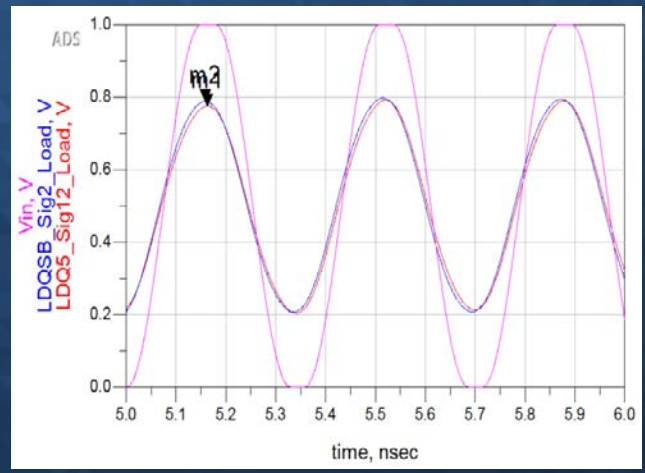


Probe Card Measurement Result (from probe to PCB)





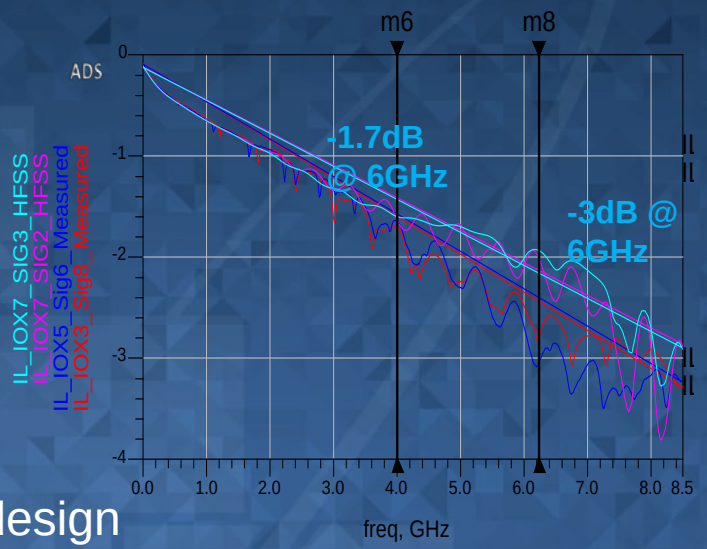


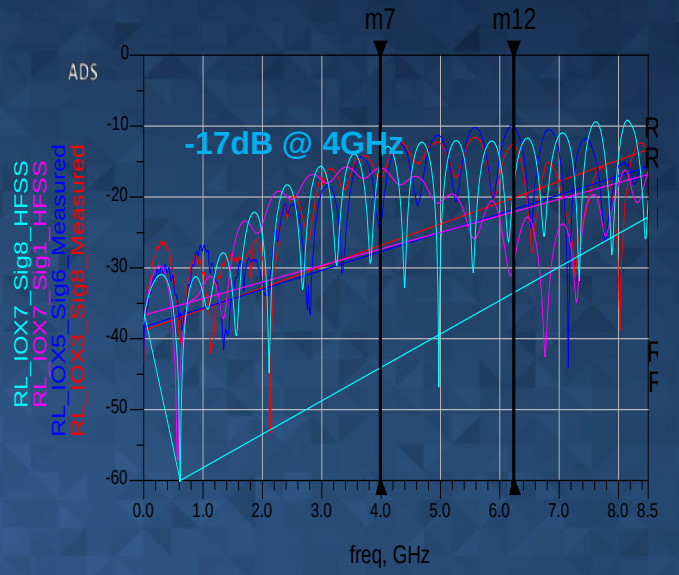


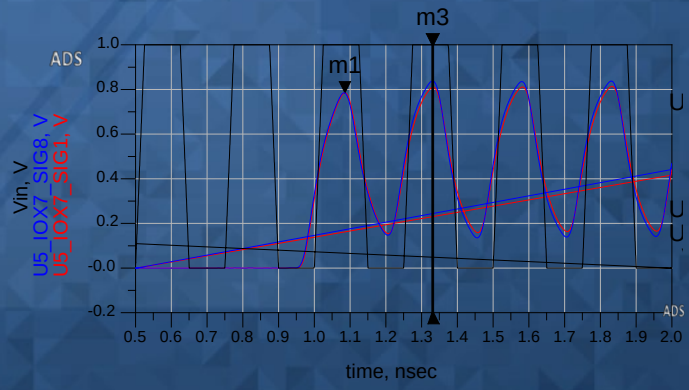
NAND KGD 4GHz Probe Card Performance

- **Probe Card Parameters:**
  - Total ~64 DUTs, 3K Probe Count
  - Dual temp -40 to 125°C
  - Customer require 4.0GHz capability
- **Probe Card Performance**
  - K40 advanced PCB routing rule applied
  - Insertion lost: at 4GHz, simulation during design show -1.6dB vs. Measured -1.6 to -1.7dB

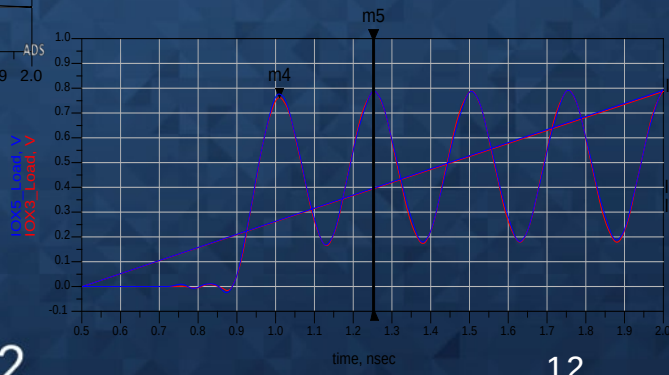
    Measurement shows capability at 6GHz -3dB
  - Return Loss: at 4GHz, simulation during design show -16dB vs. Measured -17dB
  - Voltage Amplitude: >78% of input signal







Simulation during design 80% of input signal



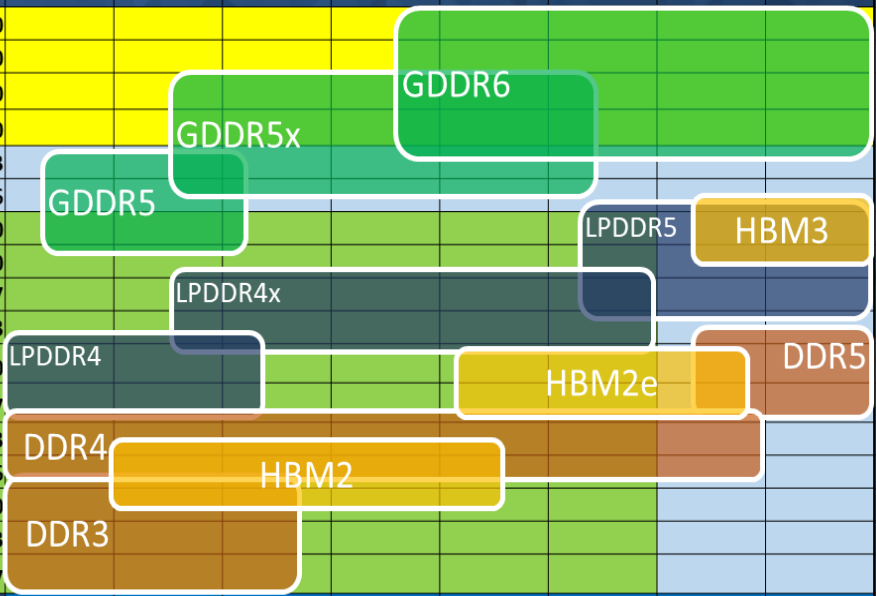
Measured 78% of input signal

Future KGDS Probe Card Development Direction

- **Satisfy for Higher Speed Test Requirements**
  - K32 (3.2GHz) has released to HVM in 2021
  - K40 (4.0GHz) customer evaluation in 2022
  - Probe Card architecture proven for >5.0GHz speed
  - >5.0GHz speed need to co-work with ATE
- **Increase Test Efficiency by Raising Maximum # of DUT on Probe Card**
  - K16 (1.6GHz) has a solution for x2 signal sharing by x2 TTRE technology to double the parallelism
  - Co-working with tester companies for higher density channels for x256 DUT at 3.2GHz ~ 4.0GHz solutions

Memory KGDS Speed Test Requirement vs. FFI Product Line

FFI Product Platform	FFI HFTAP Product Class	Clock (MHz)	Data Rate (Mbps)
		8000	16000
		7000	14000
		6400	12800
		5600	11200
Matrix	K40	4267	8533
		3733	7466
Matrix	K32	3200	6400
		2800	5600
Matrix	K22	2134	4267
		1867	3733
Matrix	K16	1600	3200
Matrix	K12	1339	2677
Matrix	K10	1067	2133
		933	1866
Matrix, PH	K8	800	1600
		667	1333
Matrix, PH	K5	534	1067



HVM | Customer Eval | R&D: Pending ATE

Key Take Aways and Acknowledgments

- **KGDS Test Demand Increase as Advanced Packaging (HBM) Chip demand Increases Dramatically**
  - AP IC revenue continues growing since 2014 forecast at 6.6% CAGR
  - As increasing AP complexity, yield become extremely challenge on Package Cost without KGDS test
  - KGDS test is one way to improve final yield and reduce packaging cost by eliminating bad components at early packaging stages
- **KGDS Test Requirements Continue to Challenge Probe Card Technology**
  - KGDS test speed requirement continues to increase (from 800MHz to 4.0GHz) and expended from DRAM to NAND flash
  - As AP IC demand increases, KGDS test solution requires better test efficiency to reduce cost and support higher volume
  - FFI HFTAP probe card technology has validated on production test passed 3.0GHz speed and achieved max 128 DUT. Performance and measurement data show promising result on Probe Card support higher speed and parallelism
- **Acknowledgment**

  - Mr. Jim Tseng (FFI): provided simulation & measurement data for this presentation