SWTEST ASIA 2022

Next Generation DRAM Temperature Requirements and Impacts to Full Wafer Contactor Probe Card Performance

SAMSUNG

FormFactor™

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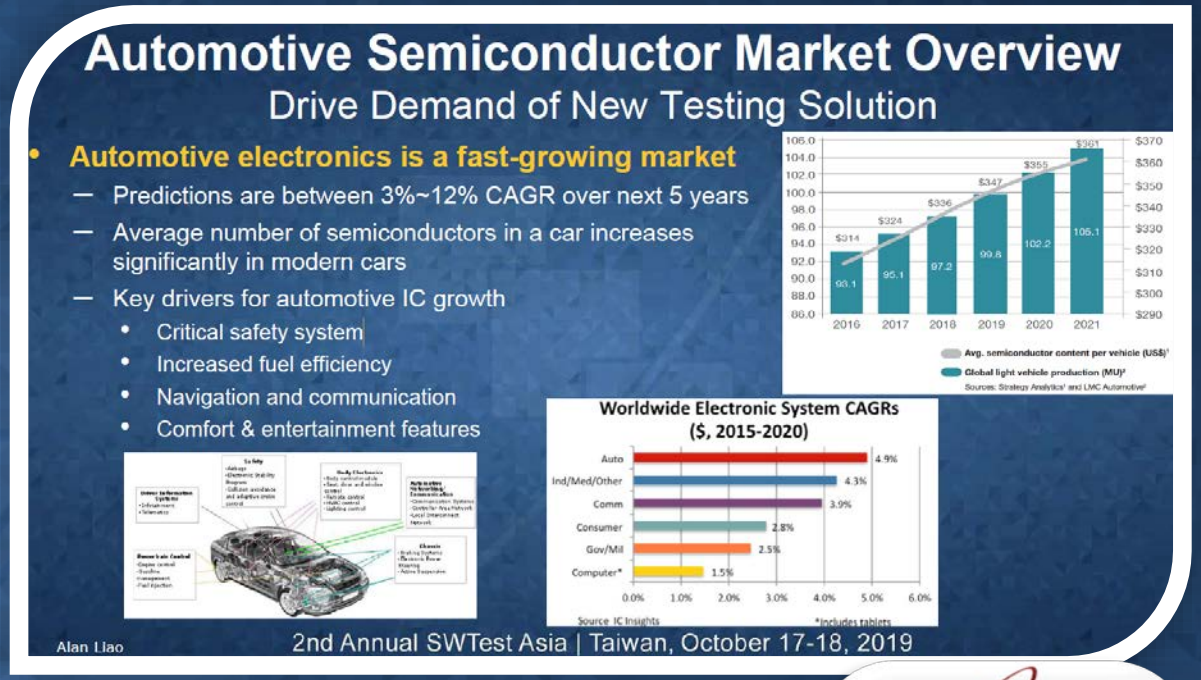
True? or False?
We don’t barbecue the cellphone and laptop.

Overview

- Automotive IC Market Overview
- Automotive IC Test Requirements and Probecard Challenges
- FormFactor High Temperature Probecard Solution
- DRAM wafer level reliability test requirements and Grade-0 test result
- Summary and Acknowledgement

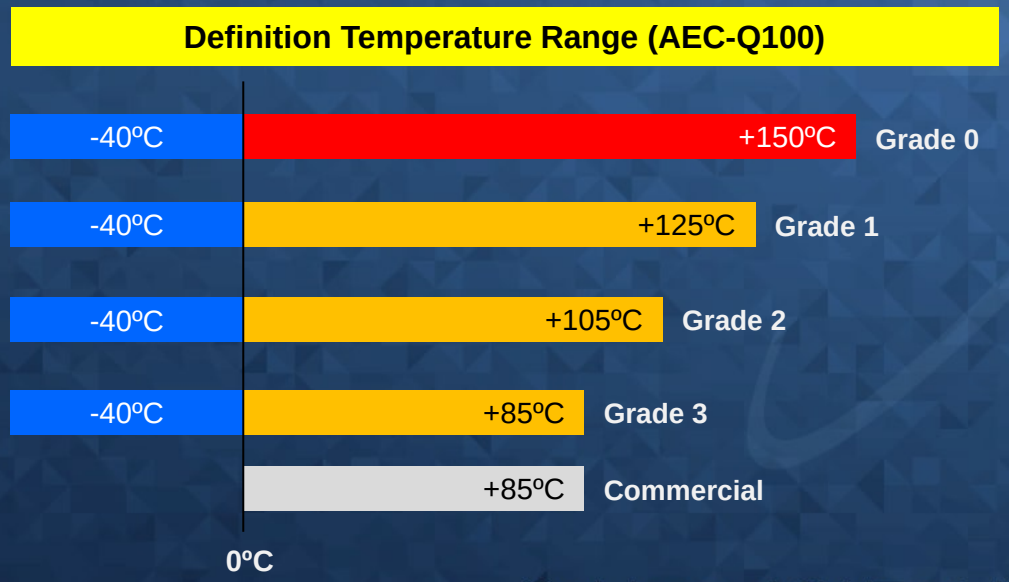
Automotive IC Market Overview

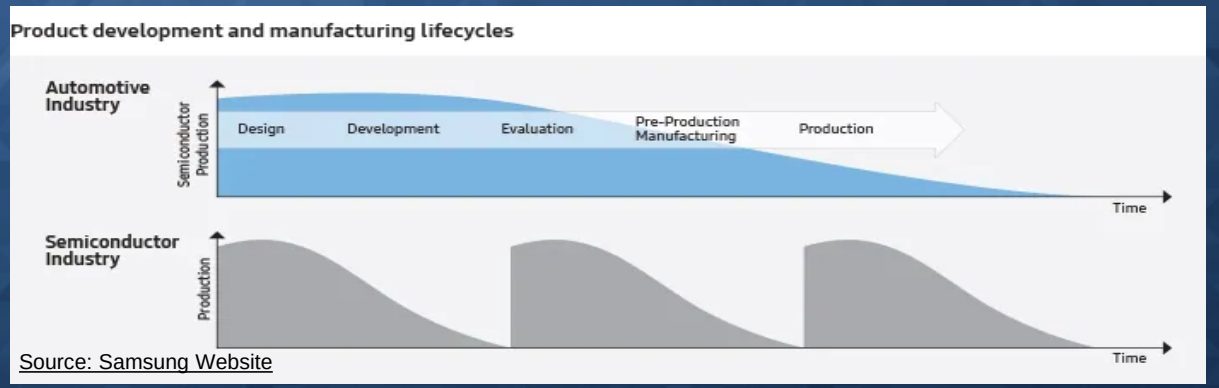
- **Key Drivers**
  - Critical Safety System
  - Increased fuel efficiency
  - Navigation and communication
  - Comfort & Entertainment features



Automotive grades and lifecycles

- **Automotive Temperature Grades**
  - 4 grades by temperature range. - 40ºC to +85ºC, +105ºC, +125ºC, +150ºC
- **Additional process requirement**
  - Additional process steps to ensure the Quality and Reliability.
- **Special BOM consideration**
  - Special BOM to ensure the Performance and Lifecycles





Source: Samsung Website

Hyun Ae Lee, Samsung
Orange Ou, FormFactor Inc.

Reliability Test at Wafer Level

- **Package Sort Test Item is moving to Wafer level Test**
  - WLBI (wafer level burn-in) at Sort Step, Test Items are enforced, Package yield is improved
- **Package Reliability Test Item is moving to Wafer level Reliability Test**
  - Improves memory device quality faster than package reliability step.
- **Reliability Items (Temperature related)**

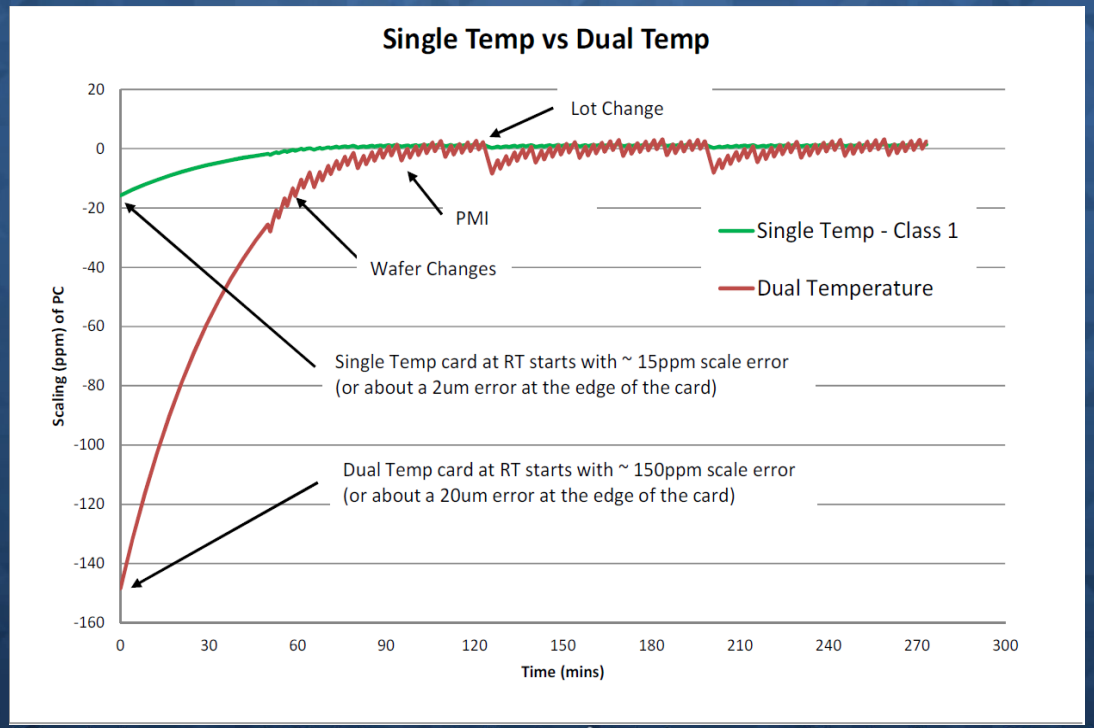
Stress	ABV	Test Method	Additional Requirement
Temperature Cycling	TC	JEDEC JESD22-A104 and Appendix 3	Grade 0: -55ºC to +150ºC for 2000 cycles or equivalent. Grade 1: -55ºC to +150ºC for 1000 cycles or equivalent. Grade 2: -55ºC to +125ºC for 1000 cycles or equivalent. Grade 3: -55ºC to +125ºC for 500 cycles or equivalent
Power Temperature Cycling	PTC	JEDEC JESD22-A105	Grade 0: Ta of -40ºC to +150ºC for 1000 cycles. Grade 1: Ta of -40ºC to +125ºC for 1000 cycles. Grades 2 and 3: Ta -40ºC to +105ºC for 1000 cycles.
High Temperature Operating Life	HTOL	JEDEC JESD22-A108	Grade 0: +150ºC Ta for 1000 hours. Grade 1: +125ºC Ta for 1000 hours. Grade 2: +105ºC Ta for 1000 hours. Grade 3: +85ºC Ta for 1000 hours.

Key Considerations for high temperature probecard design and manufacturing

- **Spring thermal stability**
  - Higher temperature capable spring material vs. current spring material
  - Spring repair process development
- **Interposer thermal stability**
  - IP temperatures from 125ºC to 155ºC depending on spring count
- **PCBA thermal stability and functionality**
  - PCBA temperatures from 110ºC to 150ºC depending on probe count
    - Material stability - Higher Temperature grade material needed
    - Component operating temperatures – Capacitor, ADG, EEPROM, FPGA, Relay
- **DUTlet component**
  - DUTlet temperatures from 130ºC to 160ºC depending on probe count
    - Caps on DUTlets rated to 105ºC/125ºC typically

FormFactor High Temperature Solution

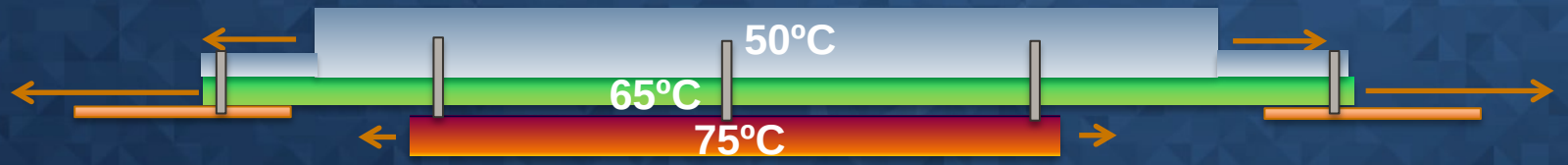
- Formfactor provides Dual Temp & Single Temp Probecards for high temperature demand
- Two types Spring – T11.2P for up to 130ºC, T11.4P for >130ºC
- Sophisticated Component selection considering high temperature on PCB



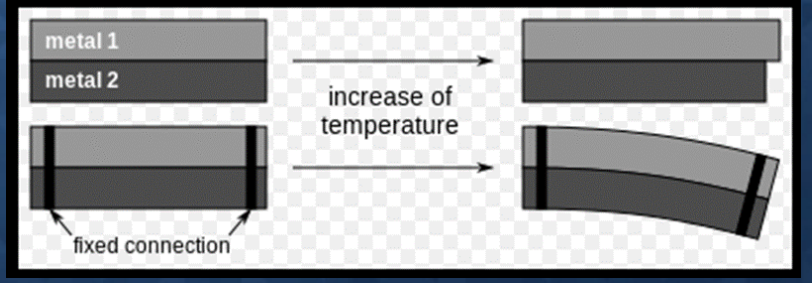
Wide Temp / Ultra High Temp Challenges

- **Thermal Z Behavior – to avoid thermal deflections**
  - Probe card Z movement is a function of many factors
    - Materials, Probe count, Cardholder material, Tester head interface, etc.
  - **Different CTE** values – $TSS_{(tester\ side\ stiffener)}$, PCBA, $WSS_{(wafer\ side\ stiffener)}$.
  - **Temperature** difference by the location
  - **WSS CTE** is selected to match the wafer expansion (dual temp), or to minimize expansion (single temp)
  - **TSS CTE** required to minimize Z movement at Hot/Cold.
  - The FormFactor Matrix card architecture has been extensively characterized and refined over hundreds of designs for many tester/prober combinations and has been optimized to provide industry leading thermal stability.

Example of Different Temperature, Different Expansion



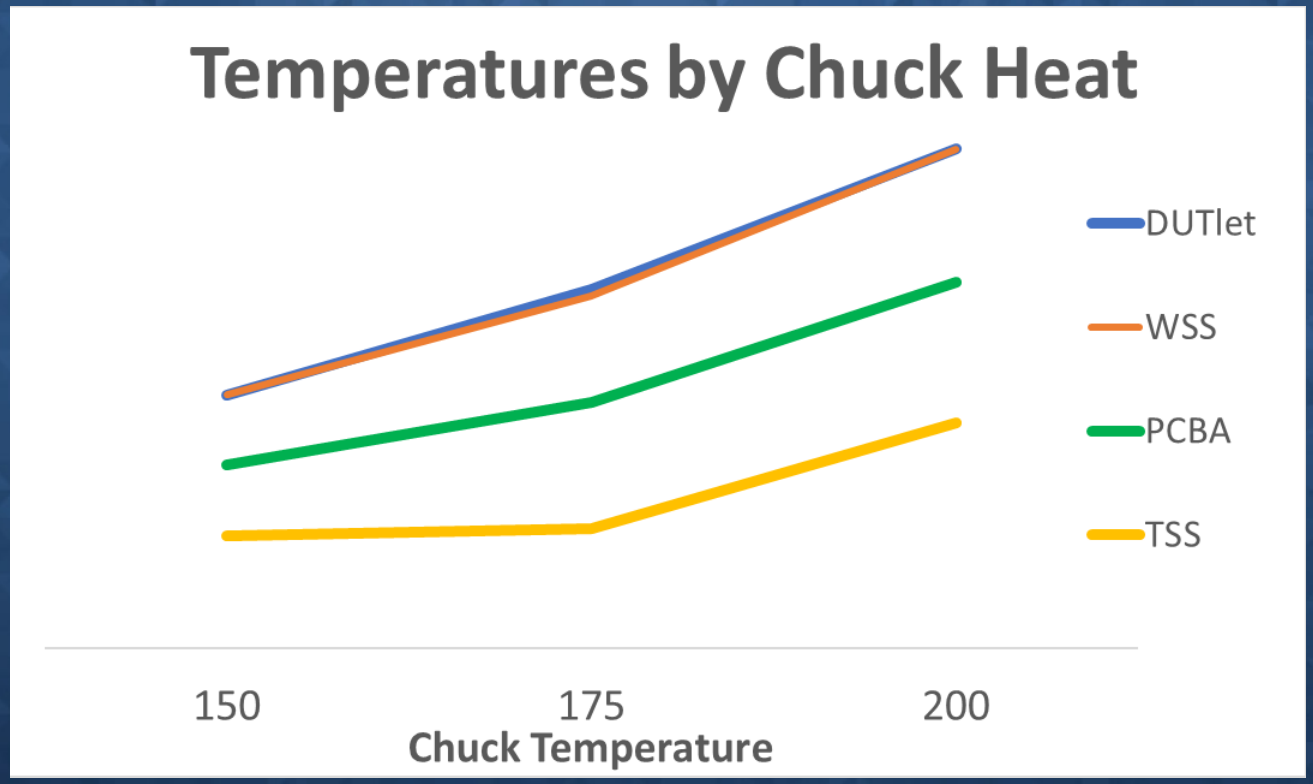
Thermal Deflection – vertically



Bimetallic strips curls when heated – different expansion ratio

Ultra High Temperature

- Thermal Characterization at 150/175/200ºC
- Implemented measurements of card temperatures at different chuck temperatures (15K spring Matrix probe card)



Grade-0 high parallel probecard development

- **Objective**
  - To verify automotive **grade-0** (-40ºC~+150ºC) probecard **in main memory** device
  - To verify the probecard running **at Reliability test condition** (>3 days wafer chip test condition)

- **Card Test condition and check points**
  - To verify **stable contact mark** at +150ºC wafer test condition
  - To check **thermal movement for 72-hour** (3-day) contact test condition

Grade-0 high parallel probecard development

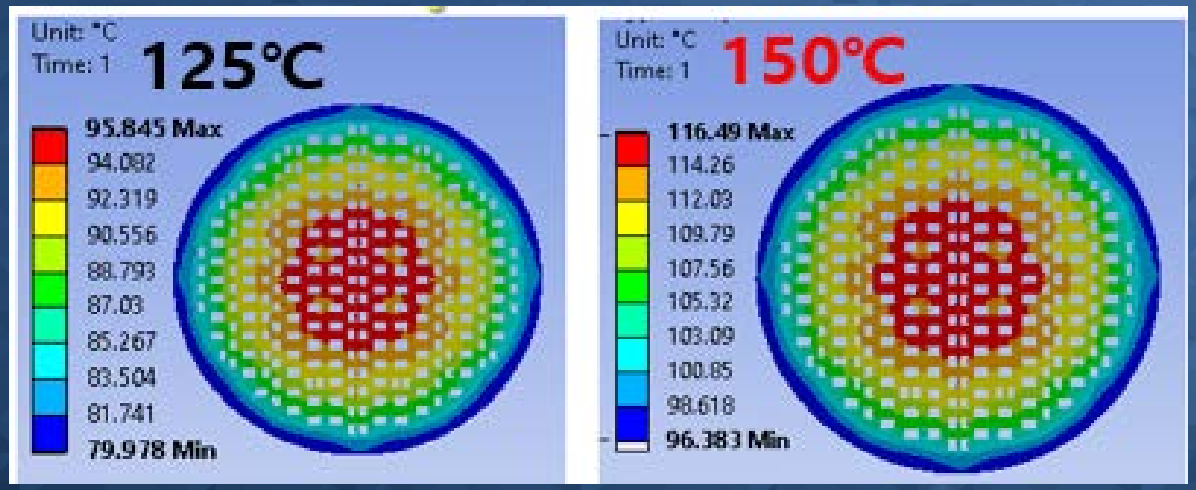
5 key considerations for 150ºC memory wafer level test

1. To decide **probing condition (soaking condition)** with different thermal uptake between probecard extraction and memory wafer at 150ºC
2. Data error possibility at high voltage, high current test condition – probecard **component** burn-out or **degradation** check
3. Probe **contact stability at long test time (>72hours)** contact- Stable contact with >30% Pad edge margin (X, Y) and Z-direction stabilization within 1-hour.
4. To verify any system error or probecard damage possibility in **thermal cycling** (-40ºC to 150ºC or 150ºC to -40ºC)
5. To verify **probe life cycle at high stress** condition (high voltage/current) in long contact time condition for stable reliability data and probecard quality.

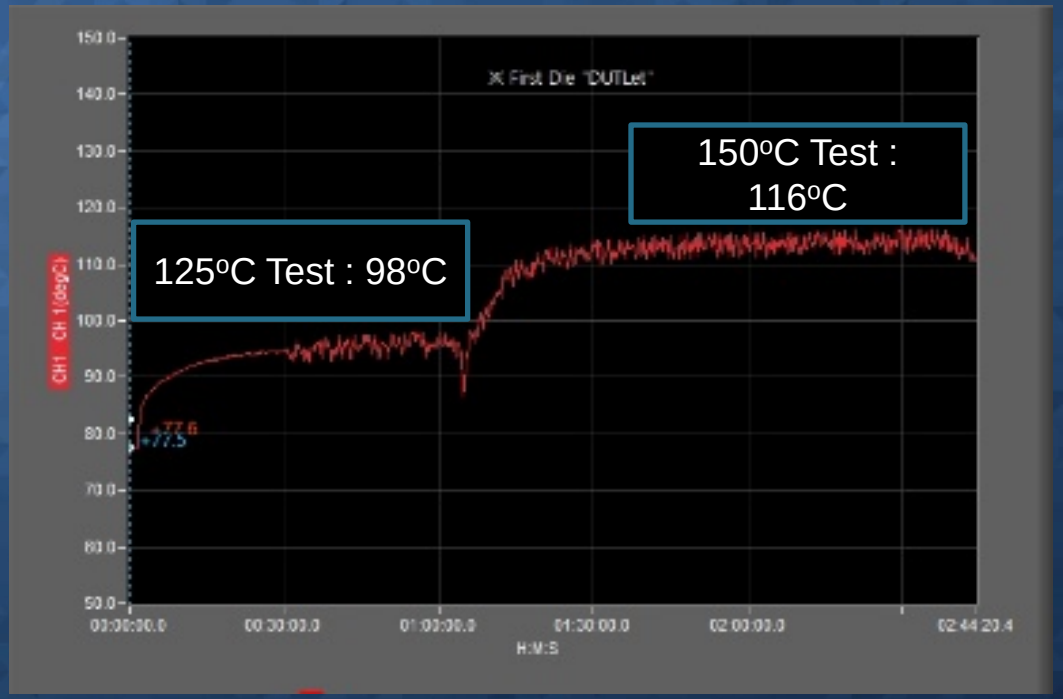
Memory Wafer Level Test Measurement -1

- **Temperatures with non-operating condition**
  - Dutlet (Contactor) temperatures at Chuck temperature 125ºC and 150ºC
  - FFI simulation is matched with Samsung measurement

- Simulation at 125ºC and 150ºC - FormFactor



- Measurements at 125ºC and 150ºC - Samsung



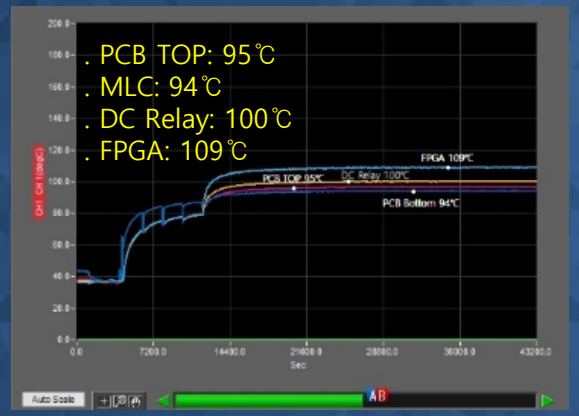
Memory Wafer Level Test Measurement -2

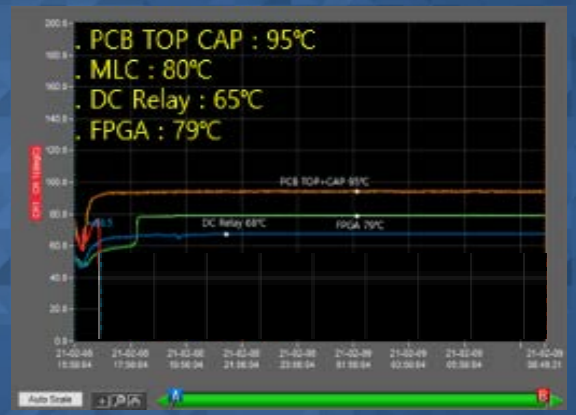
- **Temperature measurement at memory device operating condition – with normal temp probecard**
  - Considering over-heat, component should be placed outside chuck area
  - Heating components such as FPGA/Regulator/DC Relays are located outside chuck center – stable operation when wafer chip level test

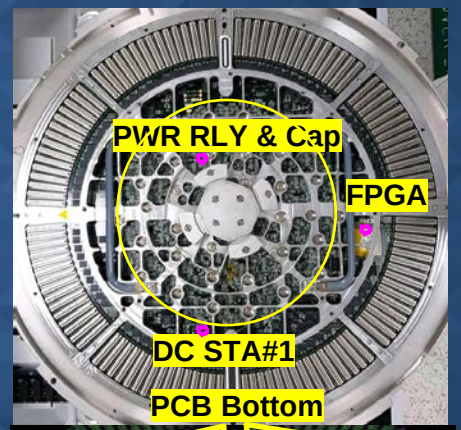
Standard Probecard

Grade-0 Probecard

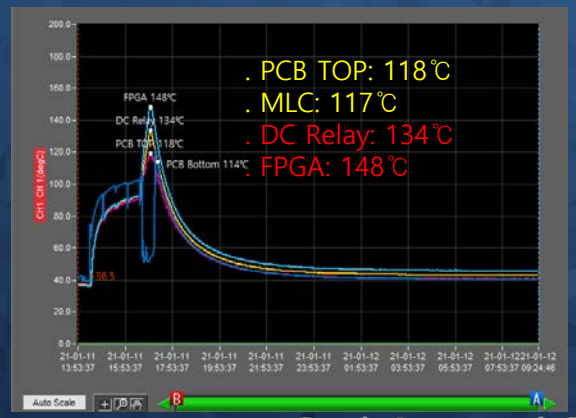
125°C Test

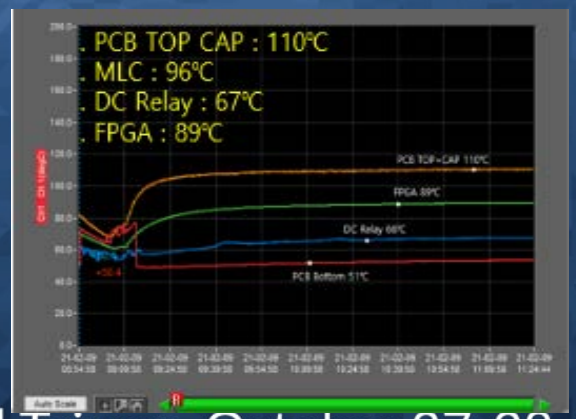


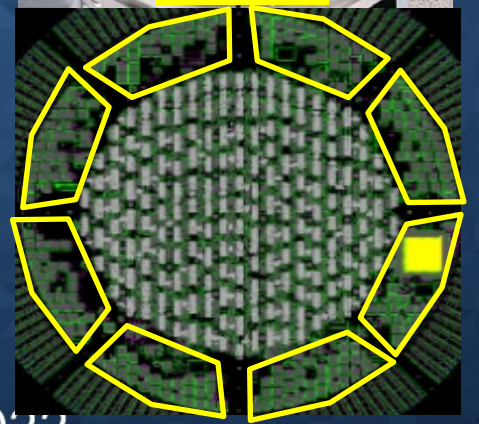




150°C Test

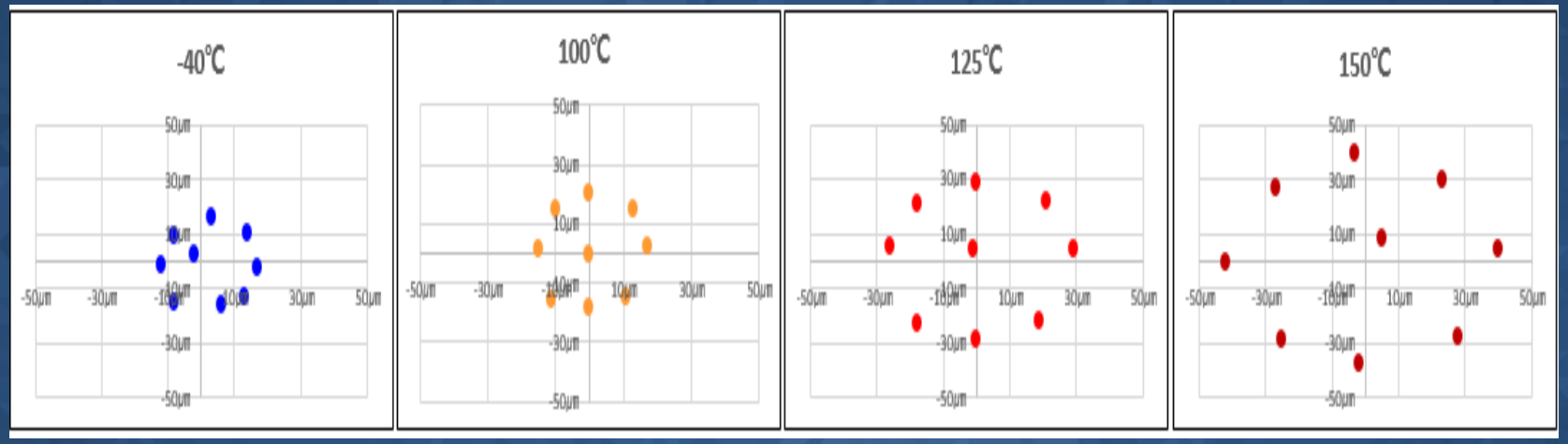






Memory Wafer Level Test Measurement -3

- **Contact Mark thermal movement**

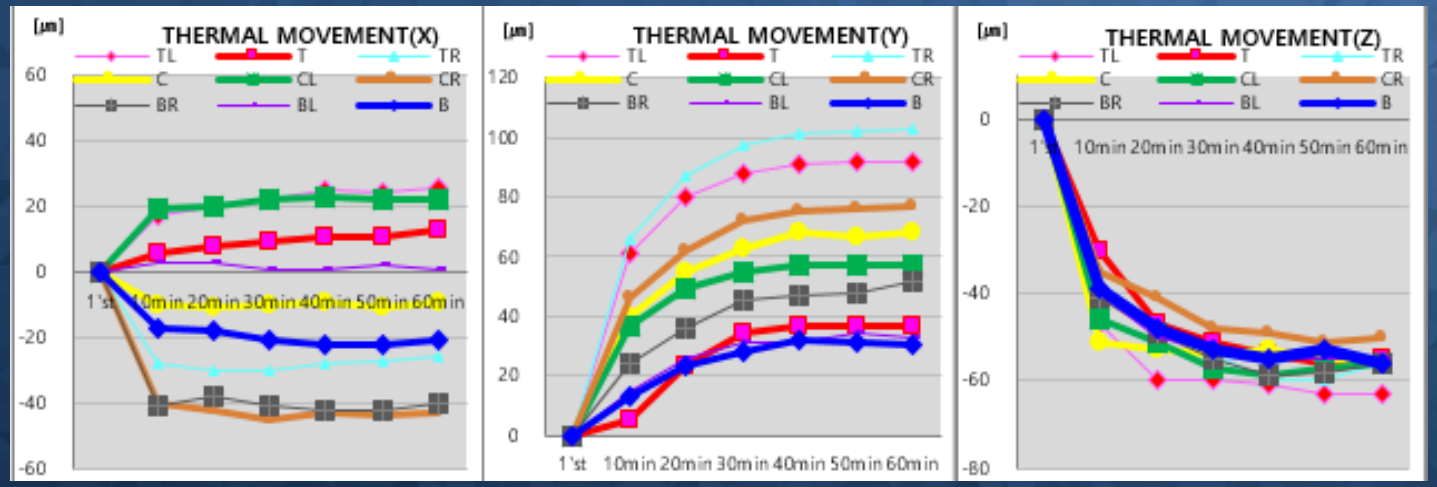


- Wafer PAD contact mark ±14㎛ shrunken at -40°C and ±40㎛ extracted at +150°C
- These contact marks track the Silicon Wafer movement through this temperature range
- Proper probe offset and prober each cold and hot temp soak time. To make stable contact mark on PAD.

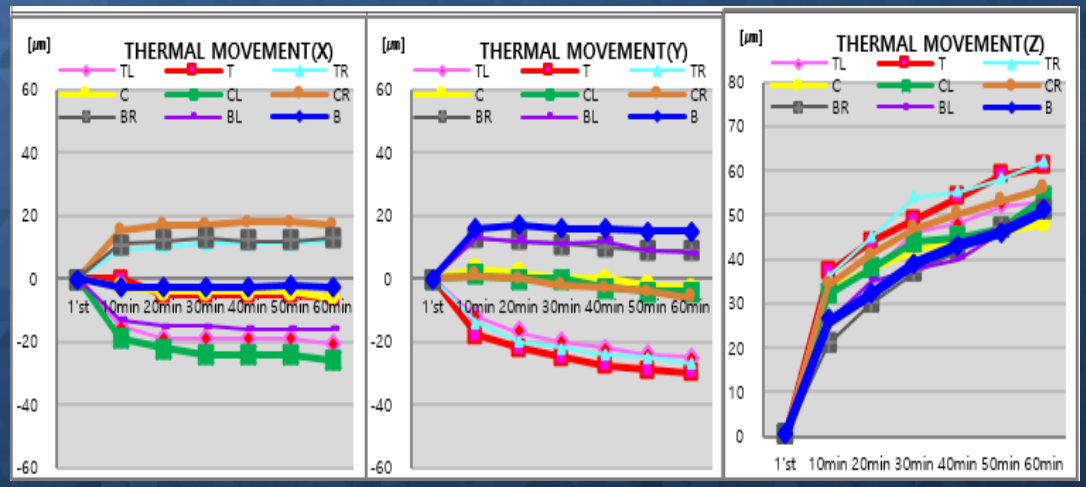
Memory Wafer Level Test Measurement -4

- **XYZ thermal movements at Cold and Hot Test**
  - Achieved stabilized contacts within an hour
- **Result after 150ºC 72 hours contact**
  - Contacts are in 58% of PAD size, Achieved Pad edge margin >40%

HOT (150ºC) THERMAL MOVEMENT (OD:180 ㎛)



COLD (-25ºC) THERMAL MOVEMENT (OD:180 ㎛)



Achievement High Parallelism Memory Wafer Test Solution for High Temperature

	2015	2019	2021
FF Temperature	130°C	130°C	175°C
Samsung R&D	-25°C ~ 125°C	-25°C ~ 125°C	-25°C ~ 150°C
Probe card Parallel	HDT(X6TRE) 5TD @ 480mm	XDT(X16TRE) 2TD @ 520mm	HDT(X6TRE) 2TD @ 480mm
Probe Type	T11.2	T11.2	T11.4
Tip Force (gram force/mil)	0.8gf/mil	0.8gf/mil	0.8gf/mil
Probing Margin(%)	>±15%	>±15%	>±15%
Soak Time	60 min	20 min	20 min
Thermal offset	-2.4um / 0.3um	2.4um / 2.4um	-3um / 3um
Result of 1TD Probing	Qualified	Qualified	Qualified

Summary and Acknowledgements

- **Summary**
  - Automotive Grade-0 Memory Wafer Level Test is feasible with High Parallel Probecard
  - Memory Wafer Level Reliability Test (>72 hours contact test) at Grade-0 condition is feasible in PAD size with >40% PAD Edge margin.
  - Maintain stable reliability data and probecard quality under probe lifecycle at high stress condition (high voltage/current) in long contact time condition.
- **Customer Acknowledgements**
  - Hyun Ae Lee, Samsung Memory EDS Team
- **FormFactor Acknowledgements**
  - Joe Ceremuga, Kalyanjit Ghosh, FormFactor R&D Team

Questions?

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Probe makes the world different and advanced probe makes the world better!

THANK YOU

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