SWTEST ASIA 2022

Wafer Level Magnetic Testing of STT-MRAM for Process Control and Chip Sorting in Volume Manufacturing

Hermes Testing Solutions Inc.

Hprobe

Antoine CHAVENT, Gilles ZAHND, Nedved SIMAO, Anthony BUSSIERE, Steven LEQUEUX, Brice BLANC, Marco MANSUETO, Matthieu ODE, Eric MONTREDON, Quentin STAINER, Thierry BRUNO, Kevin LIU, Laurent LEBRUN, Henry CHUNG, Siamak SALIMY

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Outline

- Baseline Test Flow for High Volume Manufacturing
- STT-MRAM introduction and Parametric (WAT) Test
- Proposed Automated Test Equipment for MRAM Chip Probing and Wafer Sort
- Magnetic Test on 1Mb STT-MRAM Chip
  - Single Bit Magnetic Parameter Extraction within 1Mb MRAM chip
  - 1Mb Magnetic Field Immunity
- Summary

Baseline Test Flow for STT-MRAM in HVM

Wafer Fab (front-end)

Test & Assembly (back-end)

Fab & In-line monitoring → **Wafer Acceptance Test** → **Wafer Sort Test** → Assembly → **Final Test**

Wafer Acceptance Test

- Wafer Level
- Test Key of Single MTJ
- Extraction of Specified Parameters
- Test Coverage:10 to 200 per wafer
- Pass/Fail Test

IBEX-WAT

Wafer Sort (Chip Probing)

- Wafer Level
- Chip with array of MTJs
- Extraction of Magnetic Parameters
- Immunity to external magnetic field
- Test Coverage: > 50%
- Binning Test

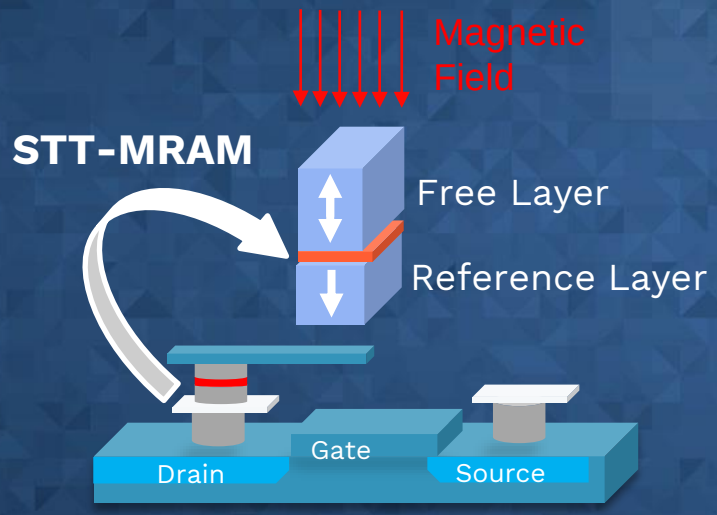
IBEX-WS

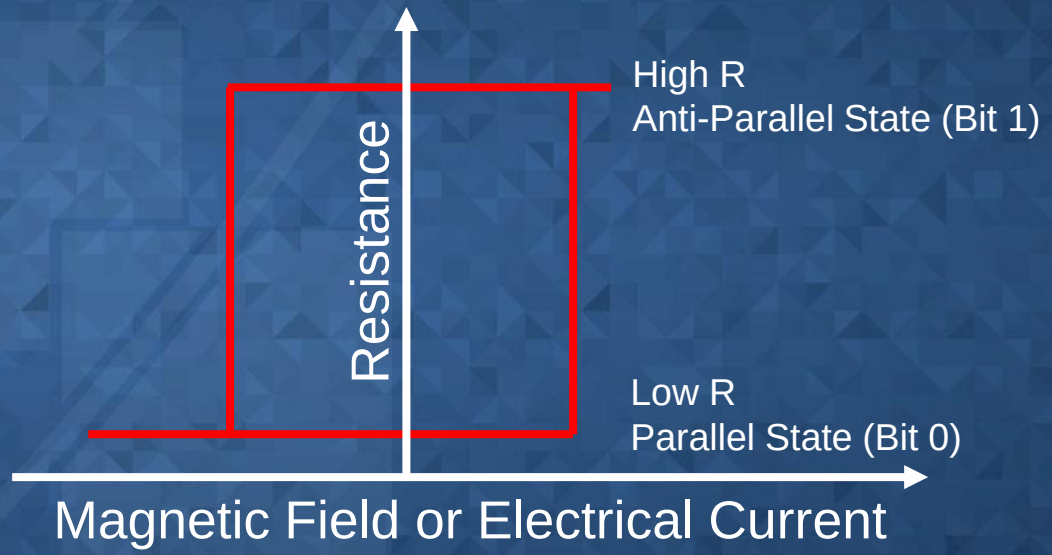
Final Test

- Packaged Level
- Chip with array of MTJs
- Extraction of Magnetic Parameters
- Immunity to external magnetic field
- Test Coverage: 10-100%
- Chip Sorting

STT-MRAM Introduction

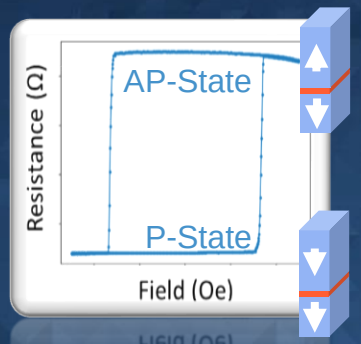
- Key cell is the Magnetic Tunnel Junction
- Integrated in the BEOL of 'CMOS like' manufacturing processes
- Two states determined by the orientation of two ferromagnetic layers separated by a tunnel barrier



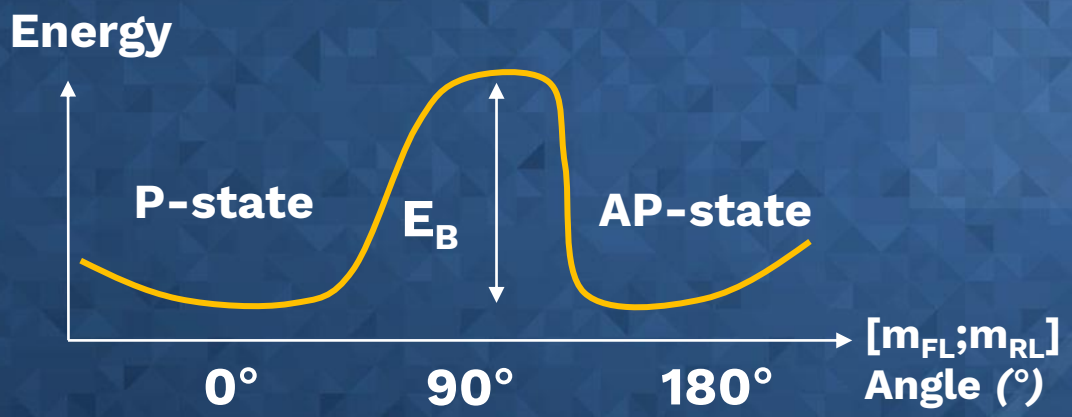


- Non-Volatile, Low Power, Fast, Scalable and Endurant
- eFlash and eSRAM replacement at sub-20nm Logic Processes
- End Application: Automotive, IoT, Wearable, AI, VR/AR

Switching Mechanism of STT-MRAM MTJs



- Switching is triggered when enough energy is provided
- To overpass the energy barrier E_B between 2 states
- Flip magnetization of Free Layer by 180°



Stability Factor of the MTJ

$$\Delta(T, I, H_{offset}) = \frac{E_B}{k_B T}\left(1 - \frac{I}{I_{c0}}\right)\left(1 - \frac{H_{offset}}{H_k}\right)^2$$

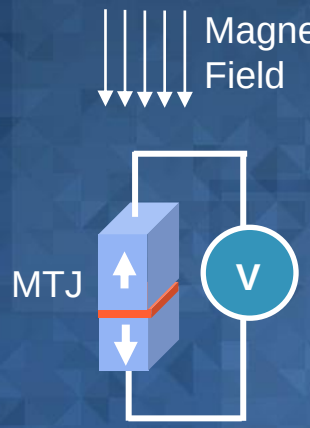
Temperature | Current | Magnetic Field

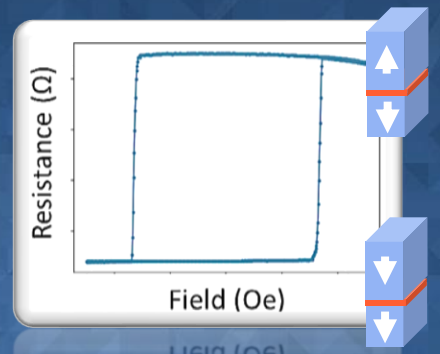
- **Switching can be triggered by Temperature, Current and Magnetic Field**

Extracted Parameters at WAT

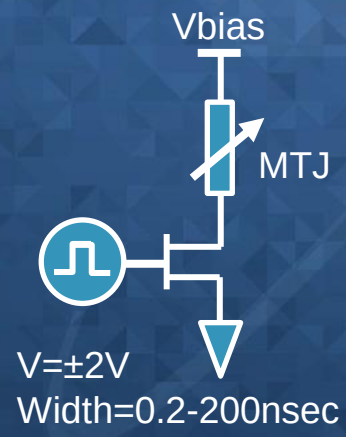
Wafer Acceptance Test

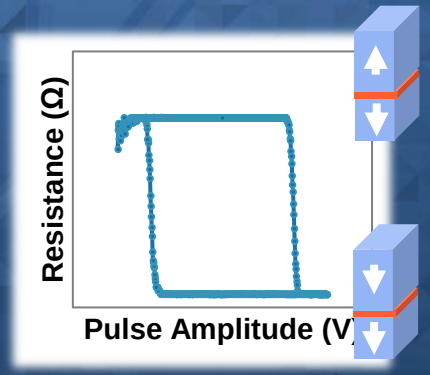
- Wafer Level
- Test Key of Single MTjs
- Extraction of Specified Parameters
- Test Coverage:10 to 200 per wafer
- Pass/Fail Test





- Tunnel Magneto Resistance (TMR)
- Probability of Switching Field
- Coercive Field → Ability to Switch
- Stability Factor → Data retention





- Probability of Switching Voltage
- Bit Error Rate (Write/Read Error Rate)

→ On individual MTJ

How to go beyond magnetic test of single MTJ ?

- STT-MRAM chips are integrating memory arrays composed of Millions to Billions of MTJs
- It is difficult to predict the magnetic parameters over a MB or GB arrays
- STT-MRAM is sensitive to a certain level of magnetic field : Chip resilience to external Field ?

→ **Process/Magnetic distributions within STT-MRAM array cannot be seen at WAT**

We propose new tool to sort MRAM chips at WS under magnetic field & temperature by:

- Extracting the switching field (Hc, Δ) per each bit of MRAM array → **to analyze distribution tails & weak bits**
- Quantifying the field immunity of the chip → **Chip resilience to external magnetic field (active/stand-by)**

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Speed-Up Magnetic Test

Proposed Test Equipment for MRAM

Chip Probing and Wafer Sort

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Proposed System for MRAM Chip Probing

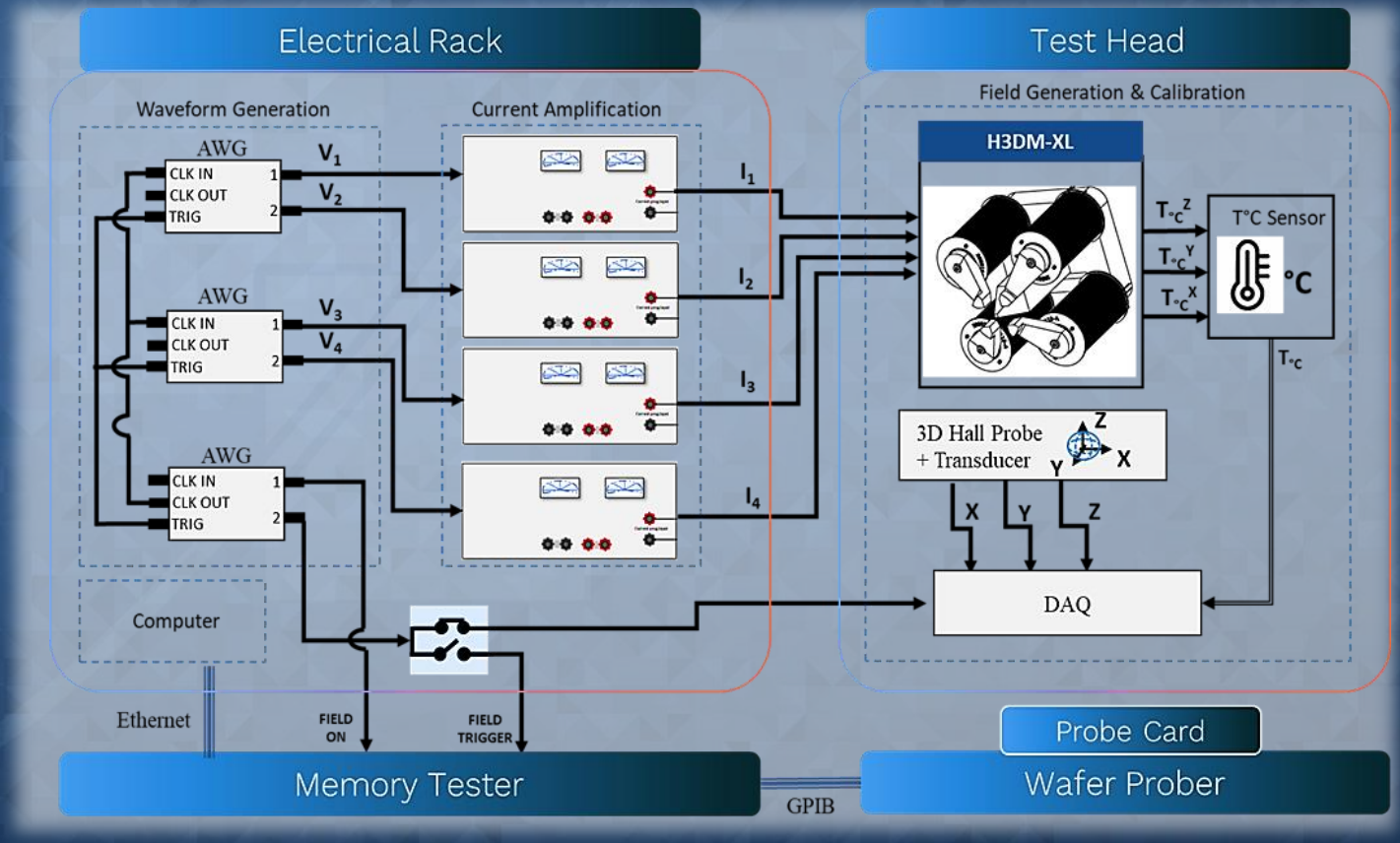
Wafer Level Test System for probing under external magnetic field

Generating Magnetic Field on wafer while probing the chip electrically

→ With Perpendicular field → switching field

→ With 3D fields → magnetic immunity tests

IBEX-WS



TEST HEAD DESIGN

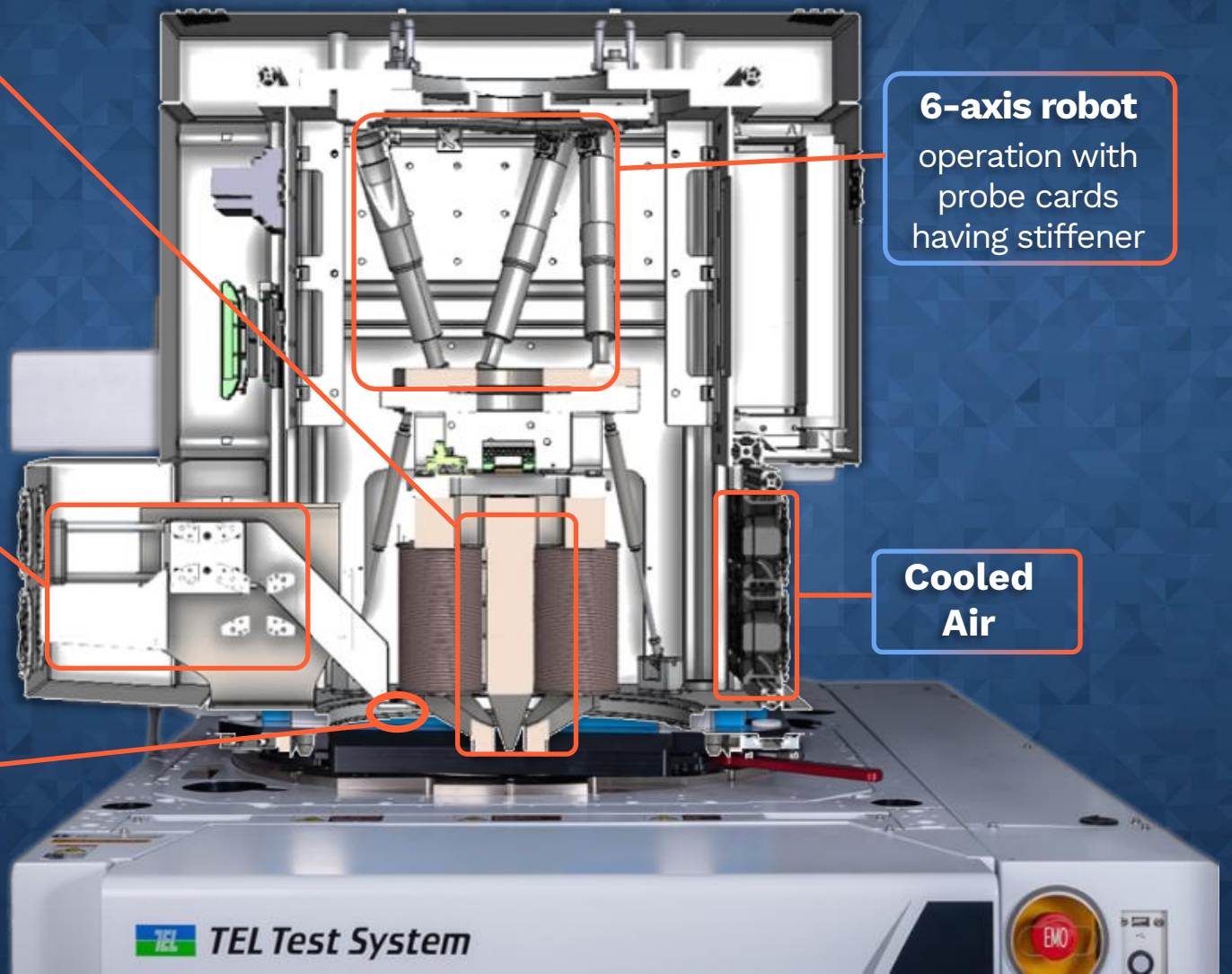
TEST HEAD DESIGN

3D Magnetic Generator
Auto-alignment of magnet to probes

Robotized FCU*
3D mapping of projected field

**Field Calibration Unit*

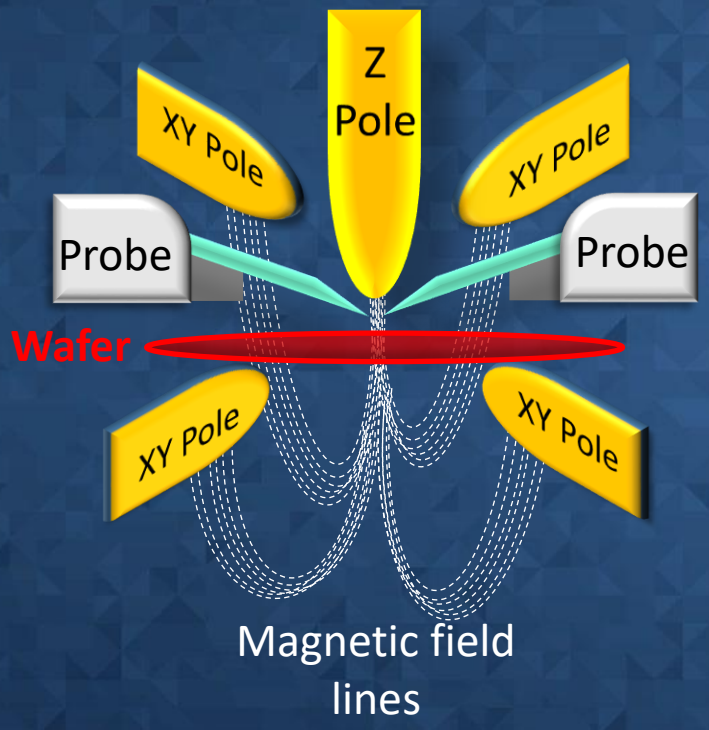
3D Hall Sensor



6-axis robot
operation with probe cards having stiffener

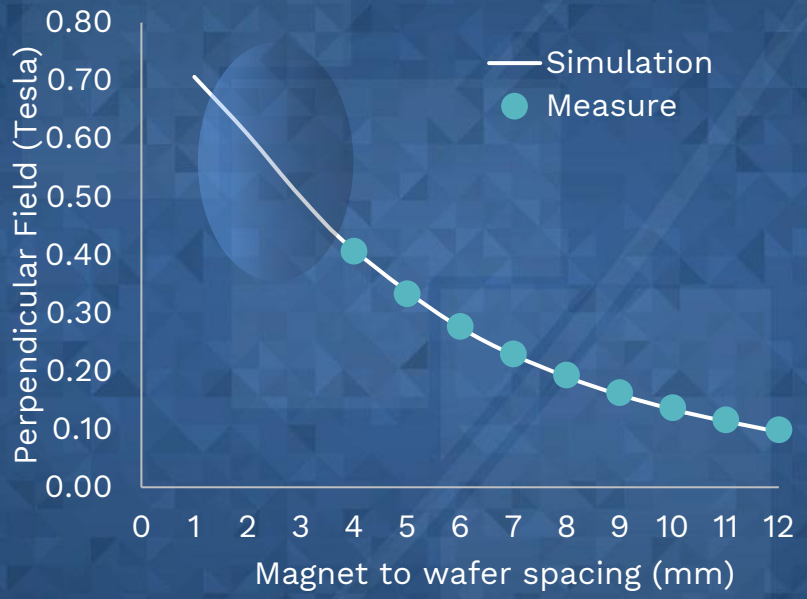
Cooled Air

3D MAGNETIC FIELD GENERATOR



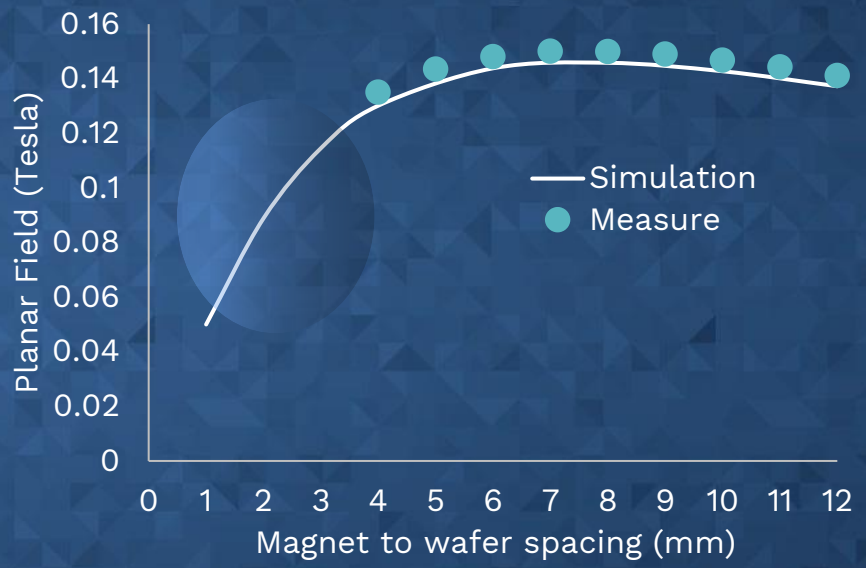
Magnetic field lines

Perpendicular



- Stability Factor per Bit Extraction
- Magnetic Immunity Test

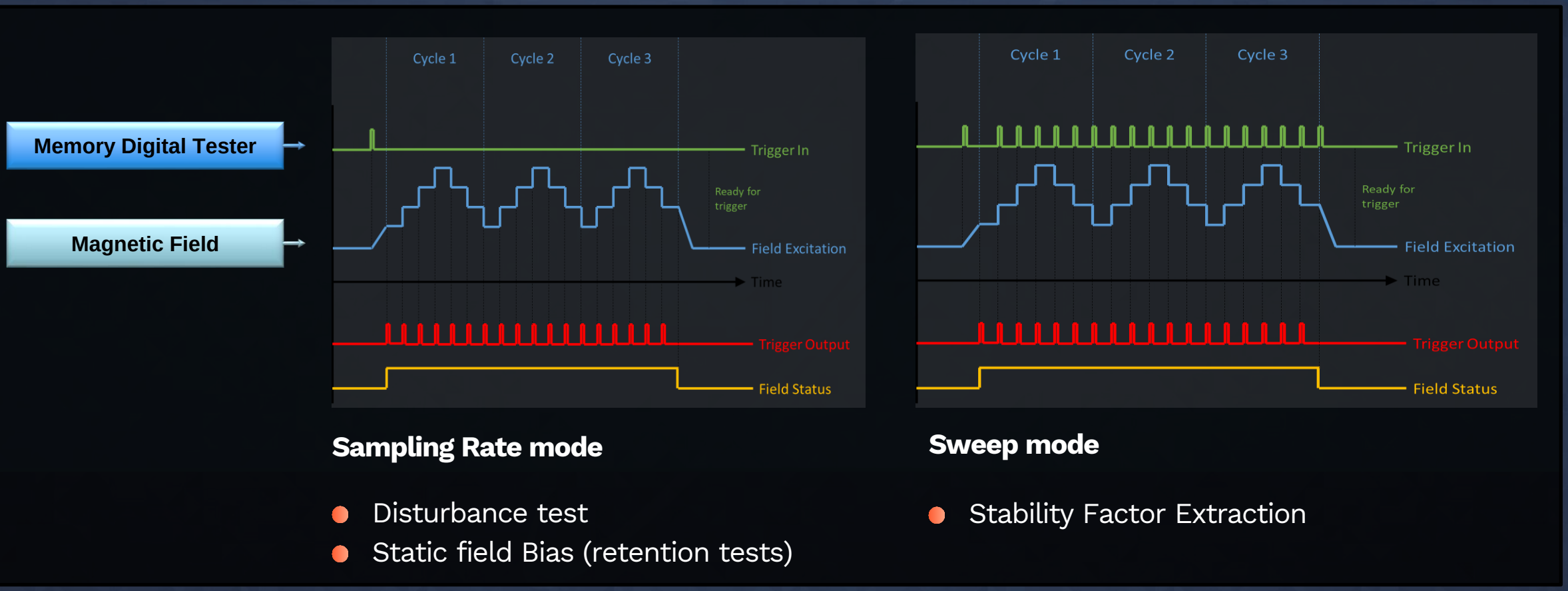
Planar



- Enable 3D field control over the test area
- Retention & field immunity testing

FIELD GENERATION SYNCH WITH MEMORY TESTER

- Designed to operate with memory tester or Memory BIST



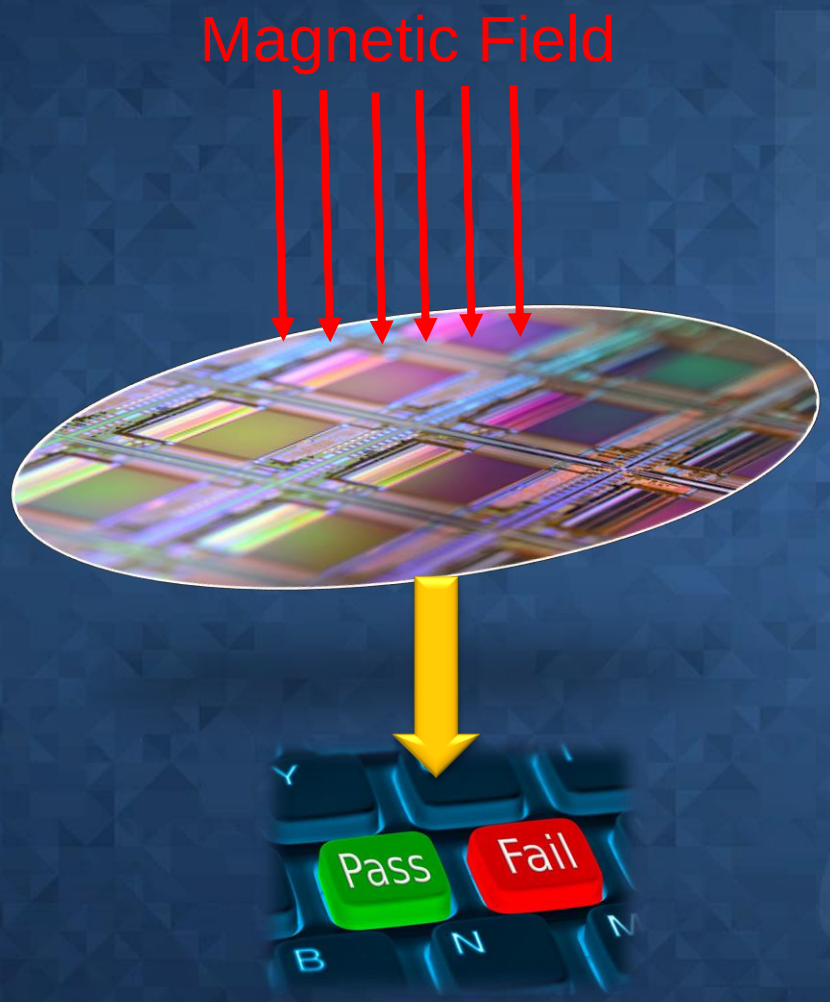
Sampling Rate mode

- Disturbance test
- Static field Bias (retention tests)

Sweep mode

- Stability Factor Extraction

MAGNETIC TEST ON STT-MRAM CHIP



- Commercial STT-MRAM 1Mb chip
- Digital Testing
- Error Correction Code Activated
- No shielding for external magnetic field

→ **Extraction of magnetic parameter per each bit in 1Mb array**

→ Switching Field to enable extraction of Hc and Δ

→ **Evaluation of Magnetic Field immunity**

→ Under 3D fields, in Stand-by and Active mode

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Speed-Up Magnetic Test

STT-MRAM Chip Array - Magnetic Parameter Extraction

Extraction of magnetic parameter per each bit in 1Mb array

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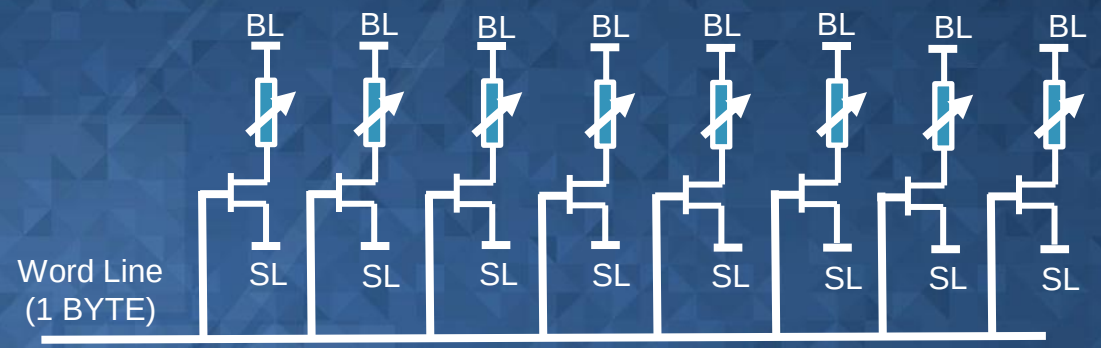
STT-MRAM CHIP - MAGNETIC PARAMETER EXTRACTION

- **1MBit STT-MRAM chip illuminated by magnetic field perpendicular to the chip**

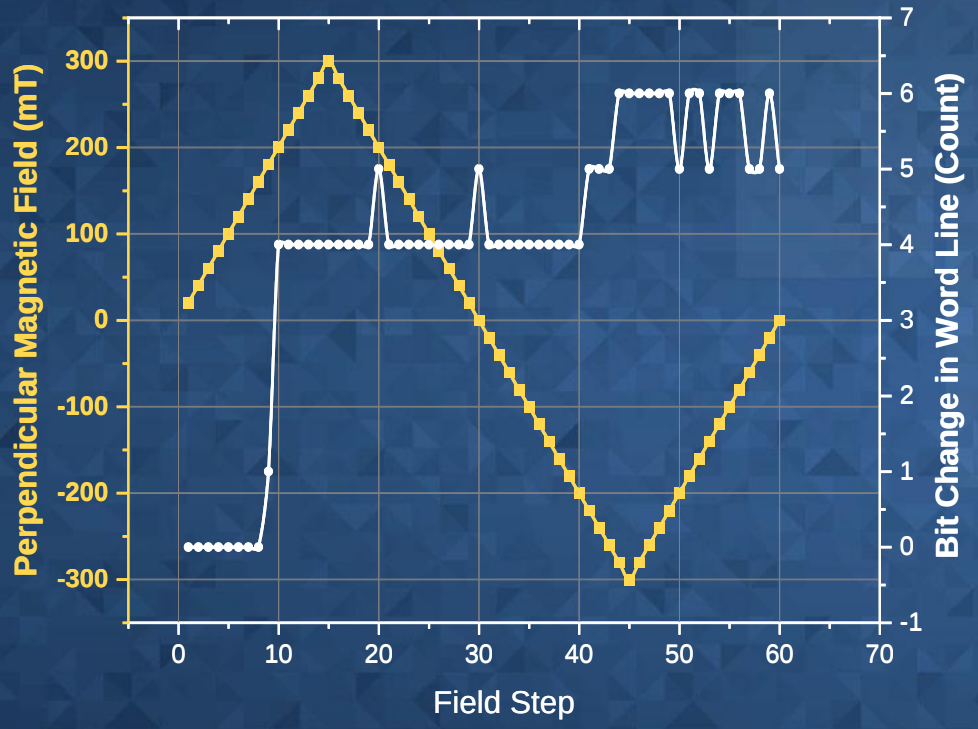
Test Protocol

1) WRITE ’00 00 00 00’ in all Word Lines
2) APPLY Field Pulse
3) READ 125kByte (1Mbit)
4) Analyze the switching per each word/bit

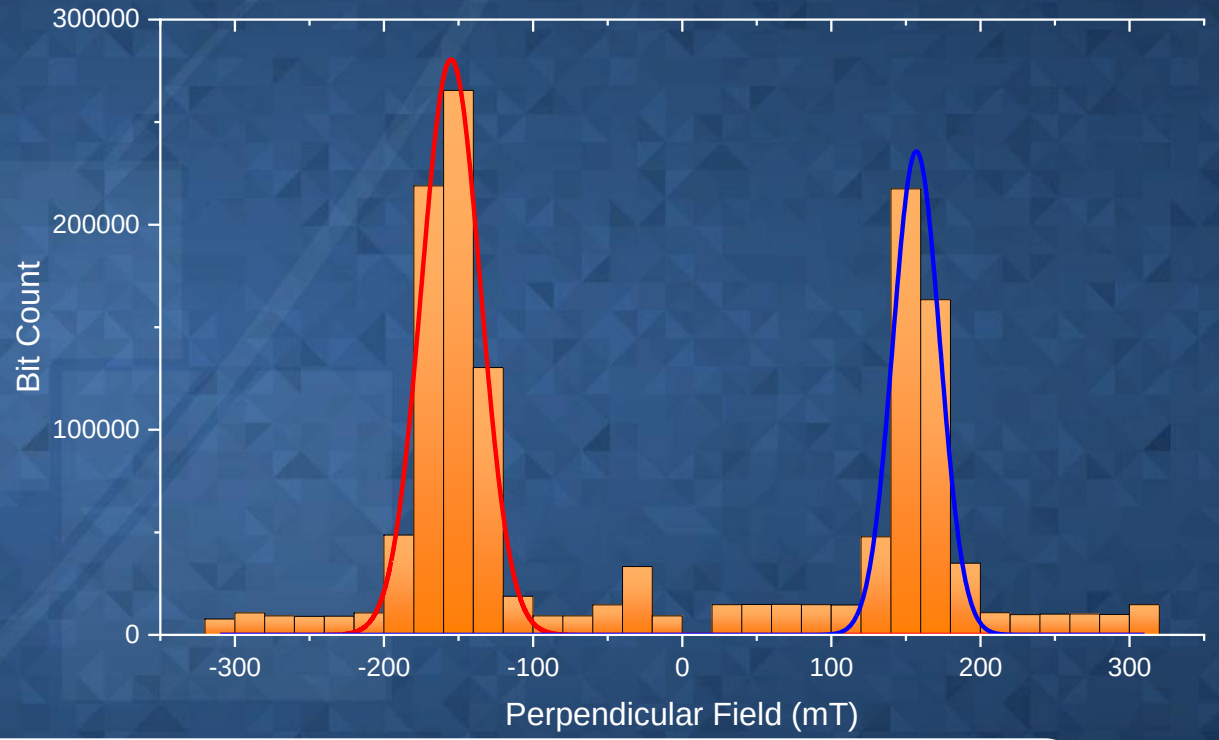


STT-MRAM CHIP - MAGNETIC PARAMETER EXTRACTION

Bit Change in Word Line by sweeping magnetic field perpendicular to the wafer



Switching Field Distribution over the 1Mb STT-MRAM chip



- Extraction of each bit switching field → Hc and Δ is now possible within digital chip (w/ ECC OFF)
- Enable identification of weak bit, tails distribution → to correlate with non-persistent failures

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Speed-Up Magnetic Test

STT-MRAM Chip Array - Magnetic Immunity

Evaluation of Magnetic Field immunity

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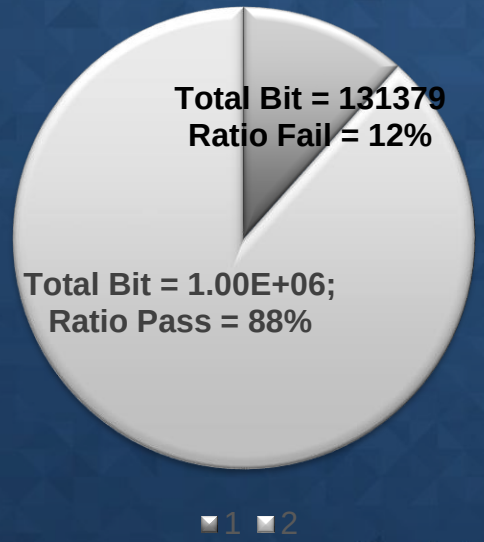
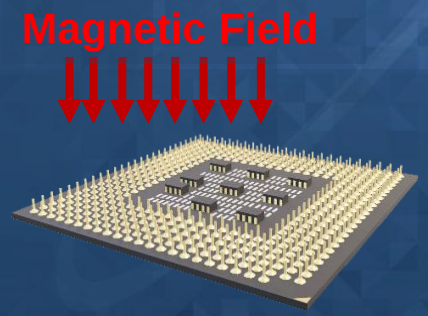
Magnetic Field Immunity – Stand-By Mode

- > 1 Hour static field at 100mT with only Read-Out at the end

Perpendicular Field constant at 100mT during 1 Hour

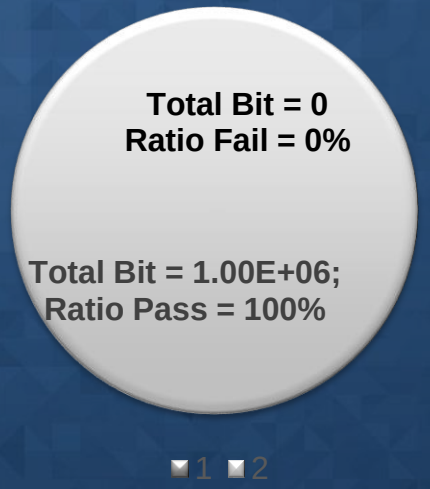
Ratio of Pass/Fail Bits

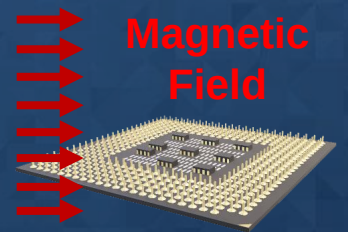




Planar Field constant at 100mT during 1 Hour

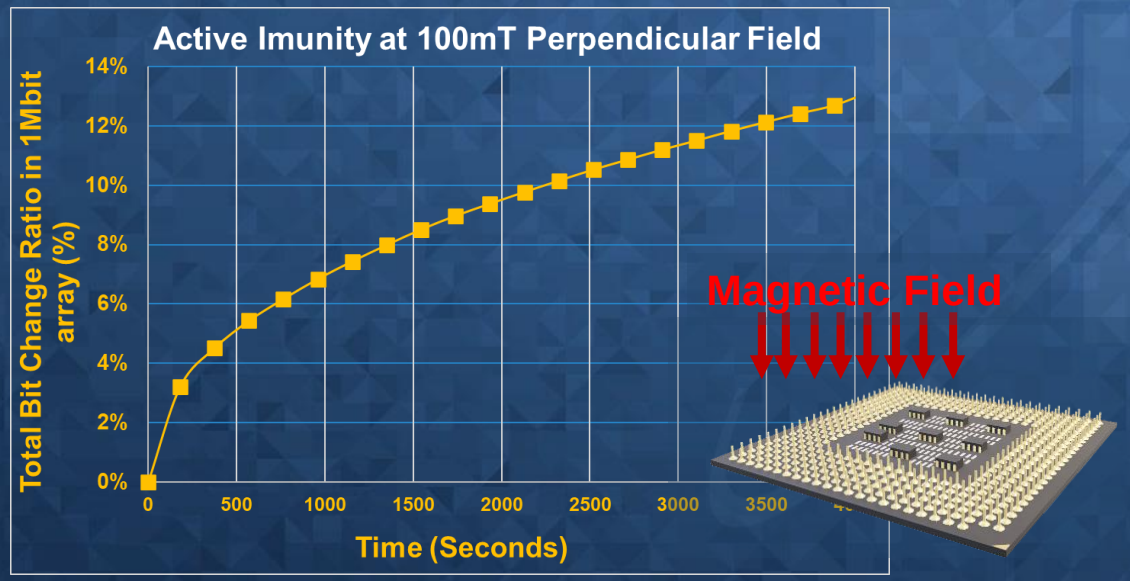
Ratio of Pass/Fail Bits

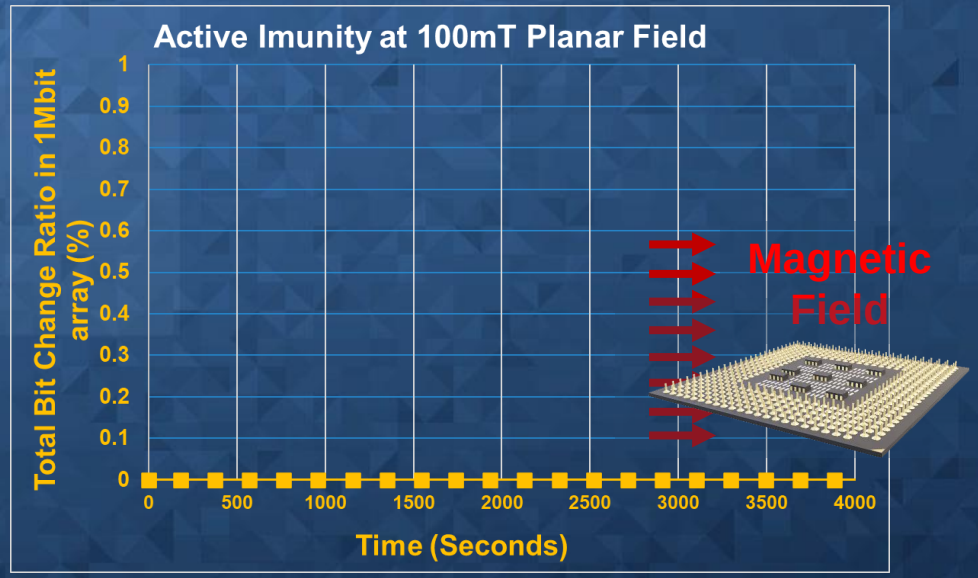




Magnetic Field Immunity – Active Mode

- > 1 Hour static field at 1kOe (perpendicular & parallel) to the DUT with Read every 3minutes





Summary

- For STT-MRAM Chip Probing and Wafer in HVM:
- We proposed to test at Wafer Sort under magnetic field to control the magnetic properties of each MTJ within the array
- We demonstrated magnetic testing capability with memory digital test:
  - To extract bits switching field distribution within the STT-MRAM array
  - To control the chip immunity to 3D external magnetic field

→ with metrics compatible with production requirements

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Speed-Up Magnetic Test

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Thank You

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PROBE TODAY, FOR TOMORROW