SWTEST ASIA 2022

HIGH PARALLELISM PROBE CARD ON V93K DIRECT-PROBE SYSTEM TO INCREASE TESTING THROUGHPUT ON AUTOMOTIVE IC

FormFactor™

John Kao (Presenter)
FSE Manager, Formfactor

Pouya Dastmalchi
Application Eng. Manager, Formfactor

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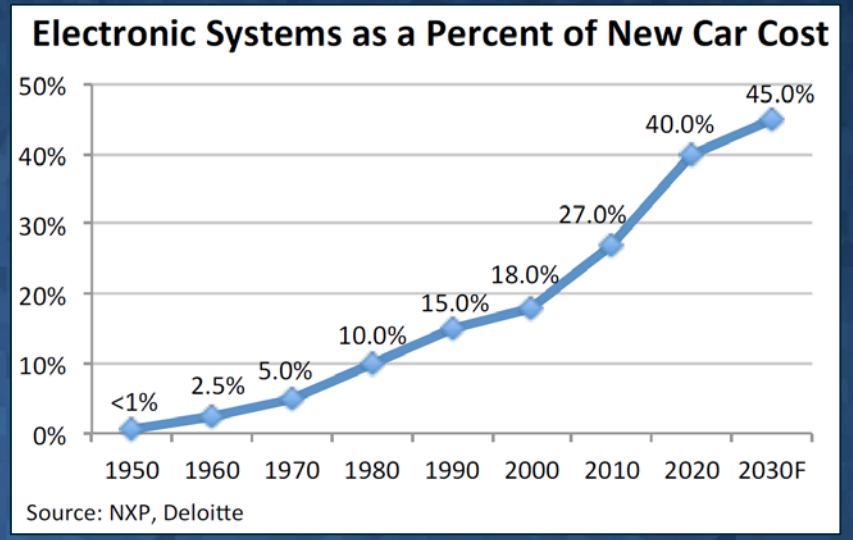
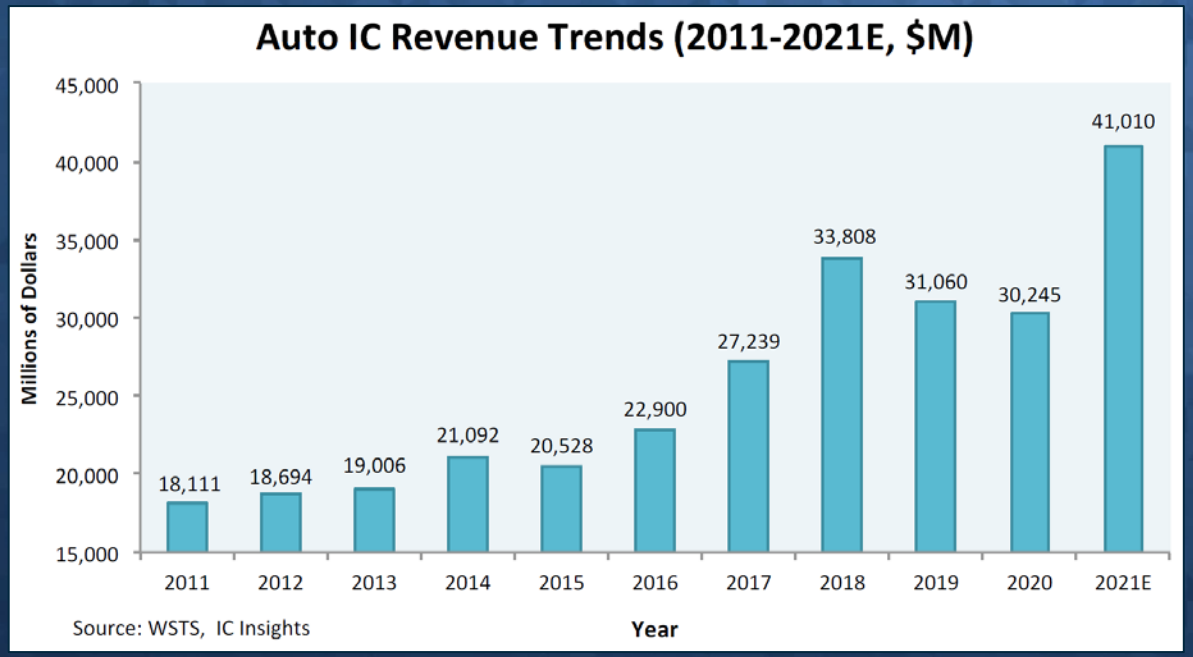
Overview

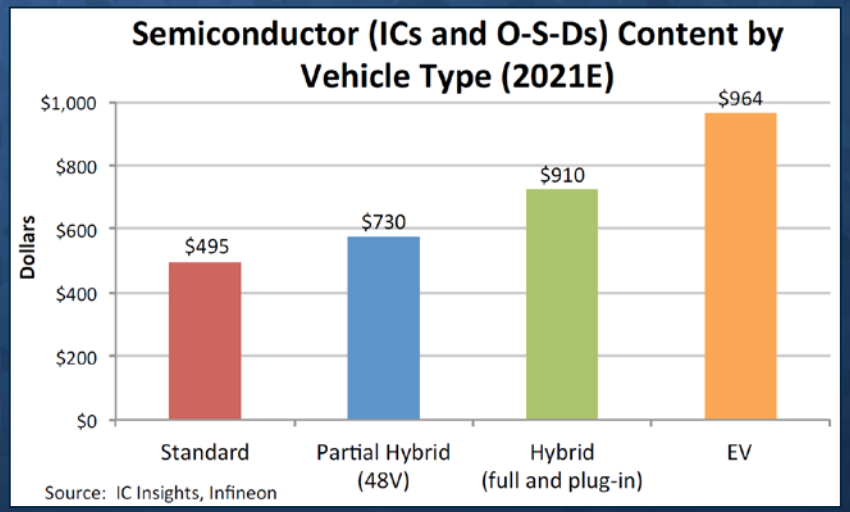
- **Automotive Semiconductor Market Overview**
- **Project Motivation**
- **A Solution to Enable High Parallelism Test on V93K Direct-Probe System**
  - Automotive high parallelism test P/C requirements and challenges.
  - Touch down – Efficiency Analysis
  - Probe card thermal planarity challenges
  - True Scale Matrix Overview
- **Final Result in Production Test Environment**
- **Summary**

Automotive Semiconductor Market Overview

- **Automotive electronic is a fast-growing market**
  - Semiconductor-built electronics is expected to approach nearly half the cost of a new car early next decade.
  - In 2021 Automotive IC Market size increased to ~$41B
  - Expanding at a CAGR of **6.2%** from 2021 to 2028.

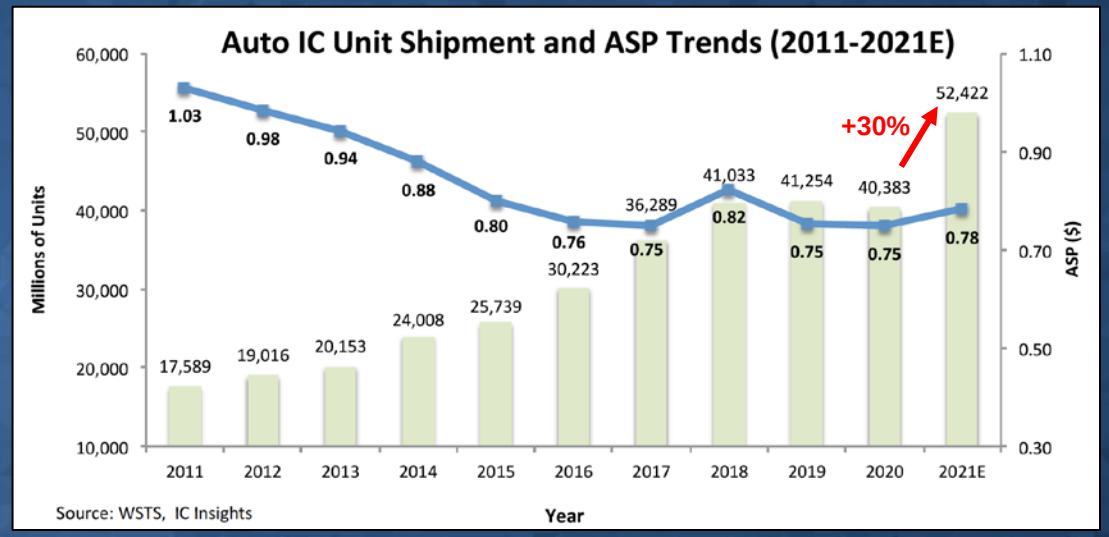






Project Motivation

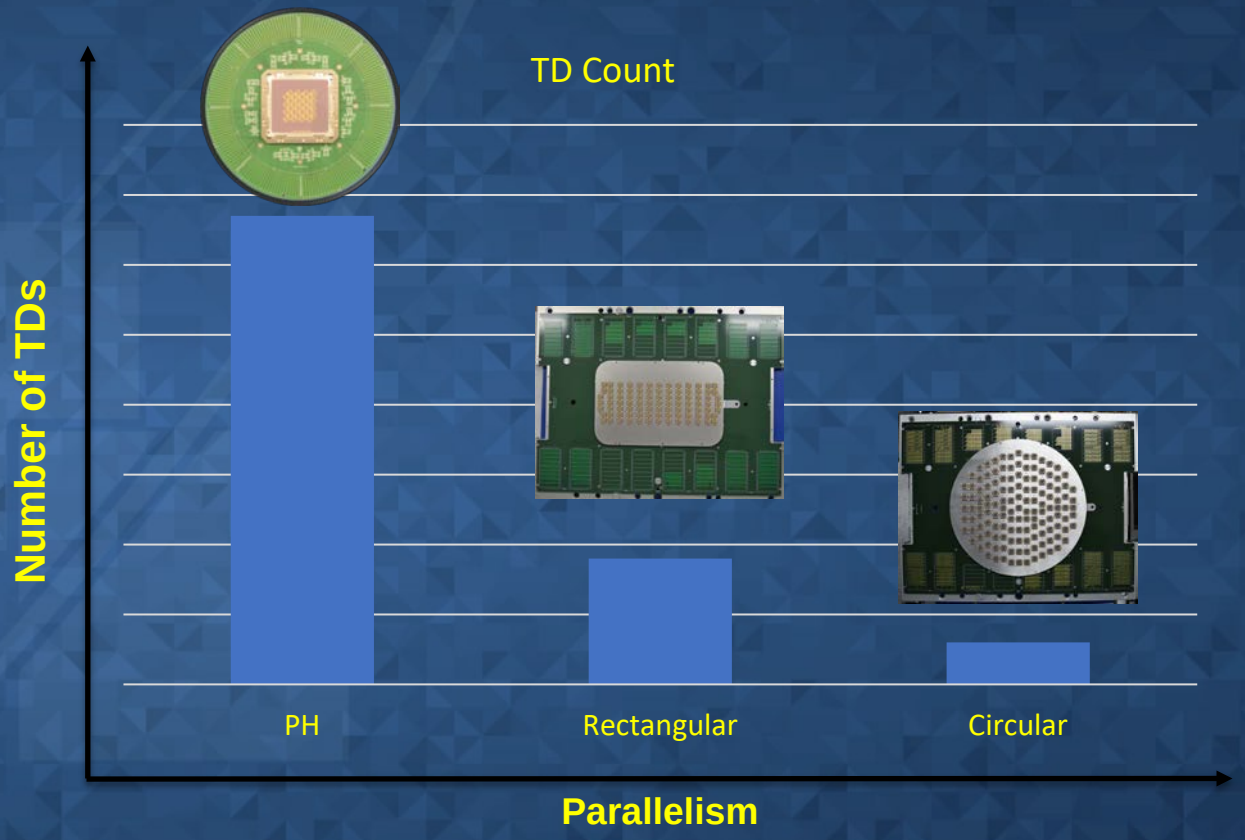
- World-wide demand of semiconductor is driving significant growth, specifically due to decarbonization and digitalization
  - Semiconductor suppliers shipped **30% more automotive IC units** in 2021 compared to 2020, compared to overall IC unit shipment increase of 22%
- **Key project goals:**
  - Increase **throughput** in wafer test with limited tester
  - Decrease **test costs per die**



- Challenges:
  - Hourly rate for test cost is increasing
  - Allocation of further test capacity blocked by global supply chain issues
- Consequence for wafer test:
  - Increase the parallelism at wafer test without increase of tester resources by:
    - Optimizing test strategy (modular test insertions)
    - Optimizing the usage of available tester resources (DPS, channels)

Higher Parallelism Enables Lower TD Count

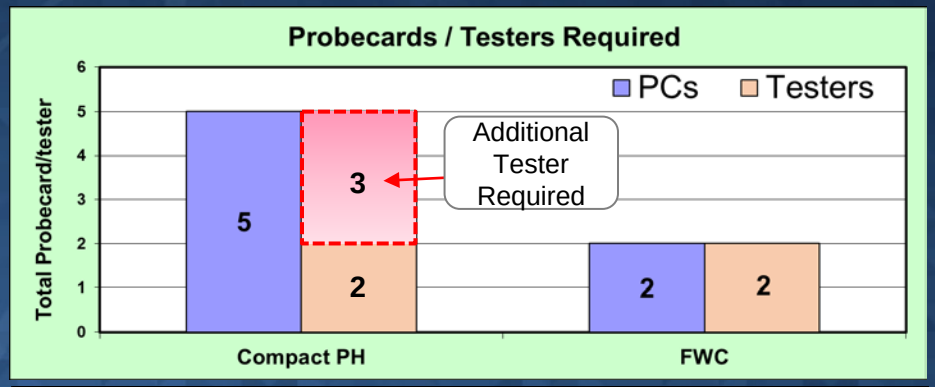
- Increased tester resources introduces the opportunity to raise the parallelism.
- Raising the parallelism would help to reduce the number of required TDs in order to test an entire wafer.
- Number of required TDs for each wafer directly impacts the test time/cost.

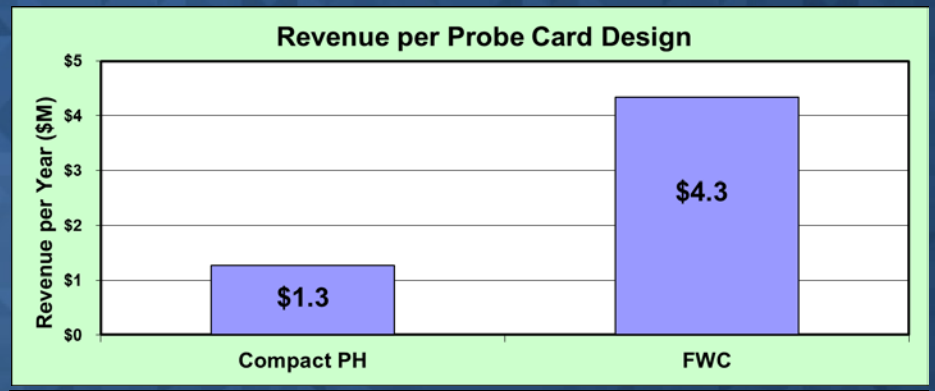


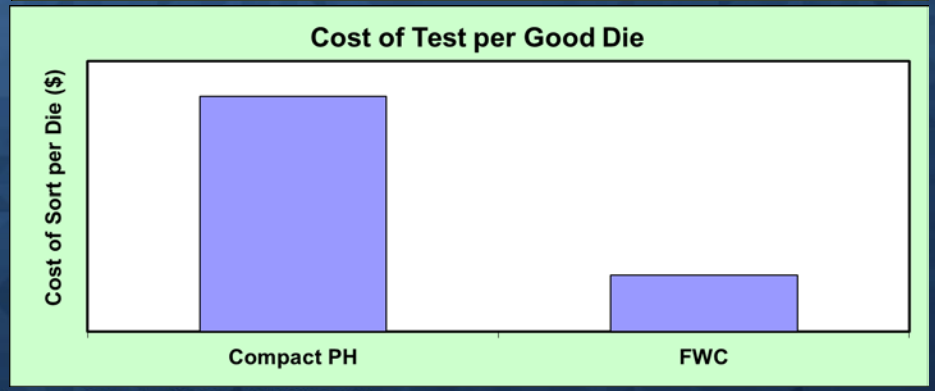
As number of sites tested on each TD increases, the test time per wafer significantly decreases

Cost of Test Model

- **Major motivation was to maximize throughput with limited tester availability**
  - Evaluated throughput increase
    - x64 solid array → 24 TD
    - x192 FWC → 7 TD
- **Model assumptions**
  - 1184 die per wafer
  - 180 sec TD for each PC option
  - 2500 wafer starts per month
  - Only 2 test cells available – not able to increase
  - Wafer and Package yield, maintenance and other parameters are assumed similar on both scenarios for model simplicity
- **Conclusion:**
  - Model confirms the FWC supports project goals to increase test cell throughput without additional capital expenditures and reduce overall cost of tested die

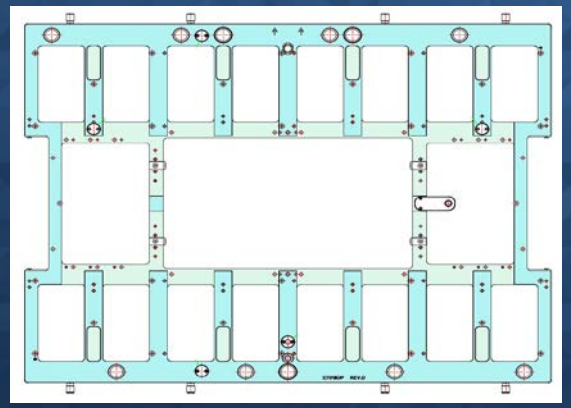


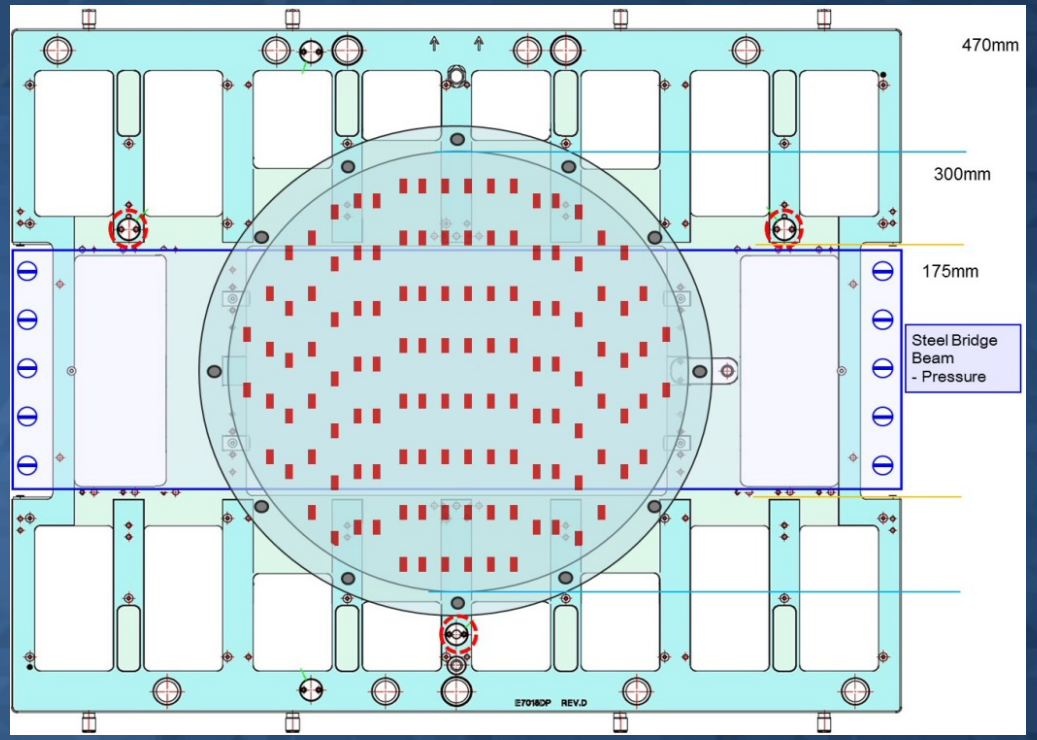


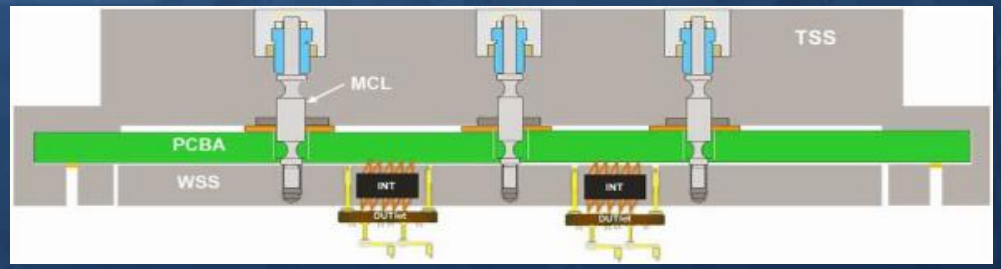


Probe Card Requirements and Challenges

- **High parallel probe card on V93K Direct-Dock**
  - Probe Card active area limit to V93K standard stiffener
    - Tester side stiffener re-design is needed
  - Largest probing area on V93K platform
    - Robust mechanical design is requested to prevent Z direction deflection force when probing.
  - Wide Range Temp Test (-40ºC to 150ºC)
    - Special WSS material can be chosen for desired thermal expansion properties. For dual temp applications, can be matched to that of Silicon – probe tips more accurately track pads across temperature range

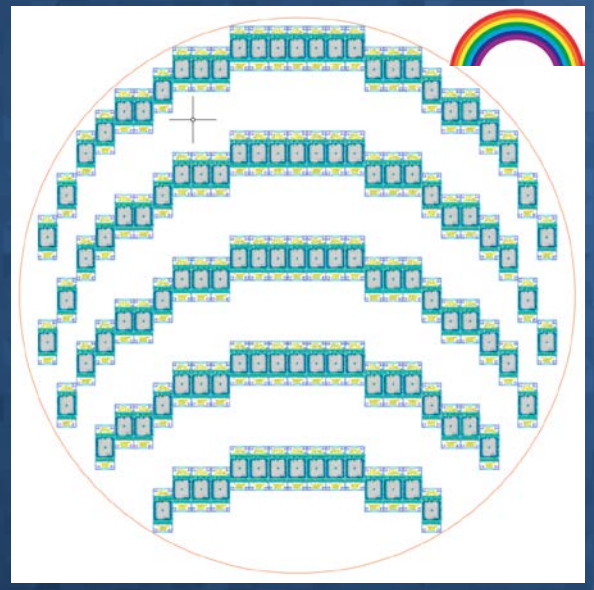






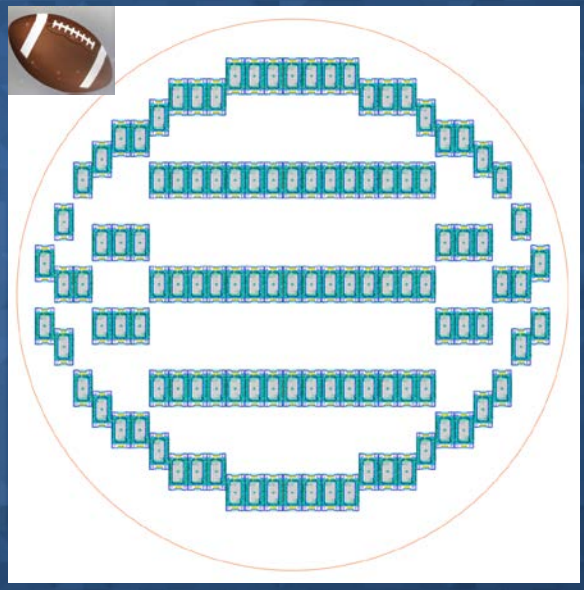
FWC Array – Optimized Site Arrangement

- **Benefits of full contact site arrangement:**
  - Allows the placement of a very high number of site
  - The array can be optimized based on priorities
  - Keeps stable thermal condition, because of low rate of stepping out of wafer
  - No chuck deflection at high pin count probecards, because of well distributed contact force



Rainbow vs Football

(Both are experts in TDs)

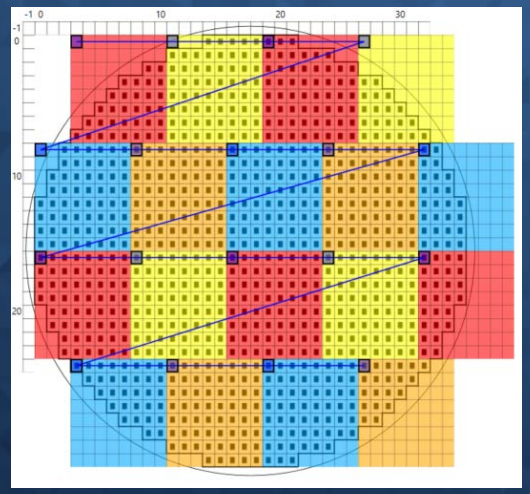


✓ No overlapping of TDs
? Larger tip boundary, less space for cleaning TDs

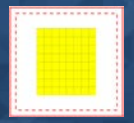
✓ Smaller tip boundary, more space for cleaning TDs
✓ Better contact force distribution
✓ Less stepping outside of the wafer
? Overlapping TDs is required in most cases

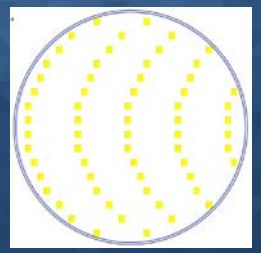
Thermal Condition Improvement During TDs

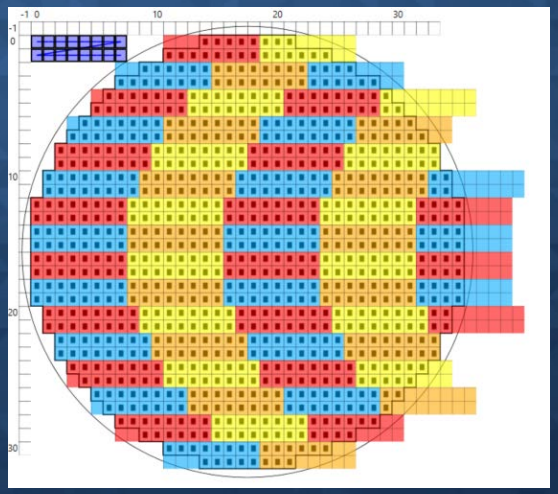
- **The thermal behavior of a probe card with any array is very critical for TDs at the wafer edge**
- **The partial touchdowns on edge can impact the performance of the card depending on:**
  - Temperature of the test
  - Test time for each TD
  - Number of consecutive partial TD
- **Full wafer array has improved stable thermal condition due to lower rate of stepping out of wafer compared to a compact array**
  - Rainbow: Up to 90% of the needle are touching the wafer
  - Football: Up to 98% of the needle are touching the wafer



Compact PH vs Full Wafer



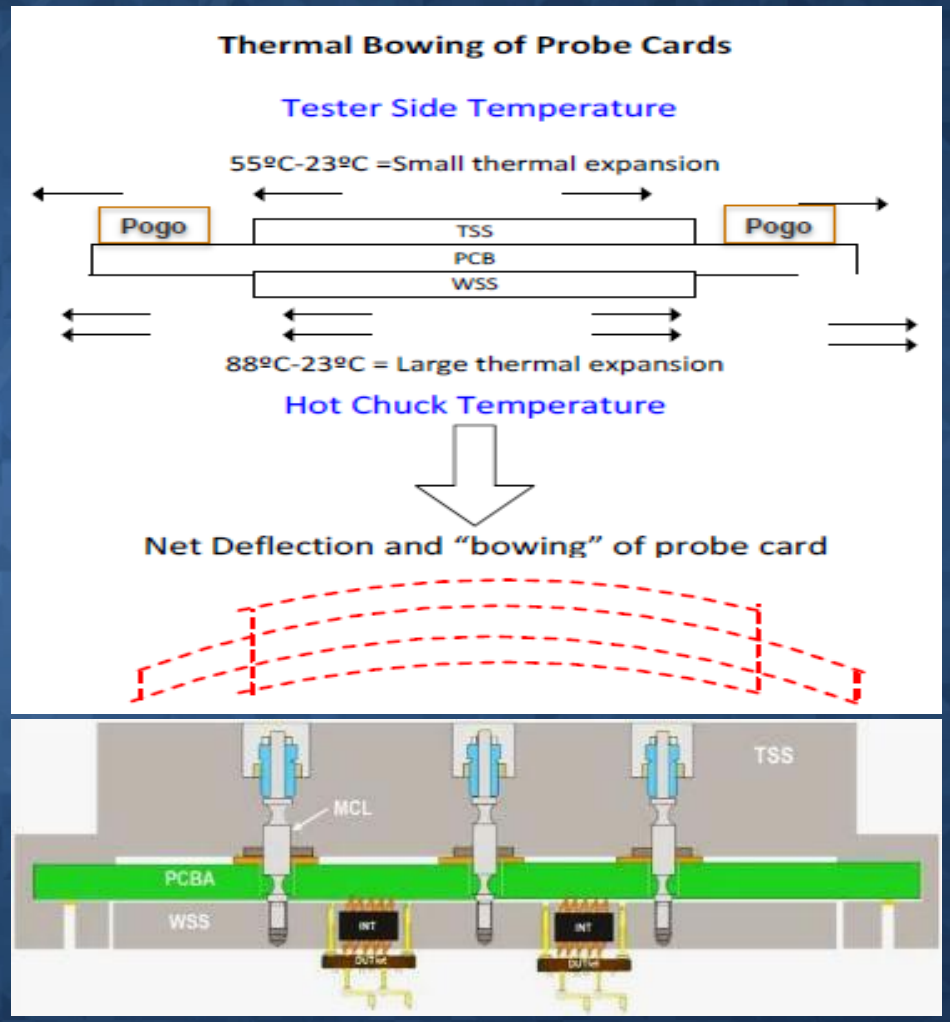




Probe Card Thermal Planarity Control

- **Thermal gradients in probe card produce differential expansion across probe card components and can produce probe card bow**

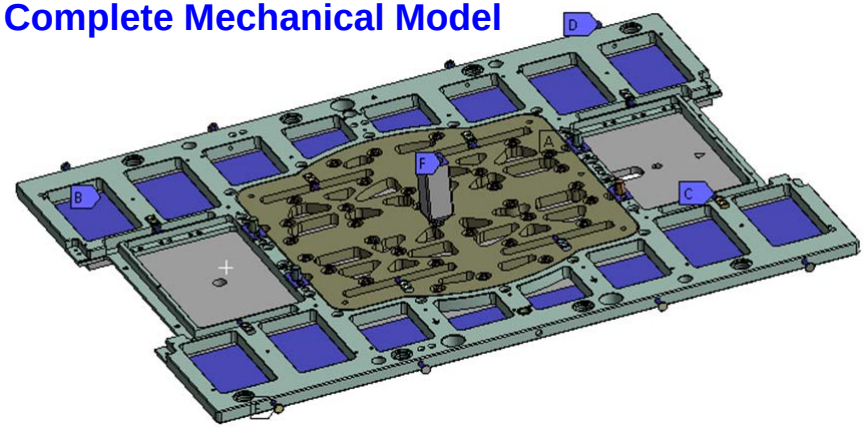
- **Design and build the probe card for better thermal planarity control**
  - Mechanical simulation to understand thermal behavior
  - Design automation (real-time probe card deformation simulation) to optimize **M**echanical **C**oupling **L**ink location for planarity control
  - Added flexible shim kit design on inner tester side stiffener to enhance engagement with V93K DD bridge beam reduce deflection.



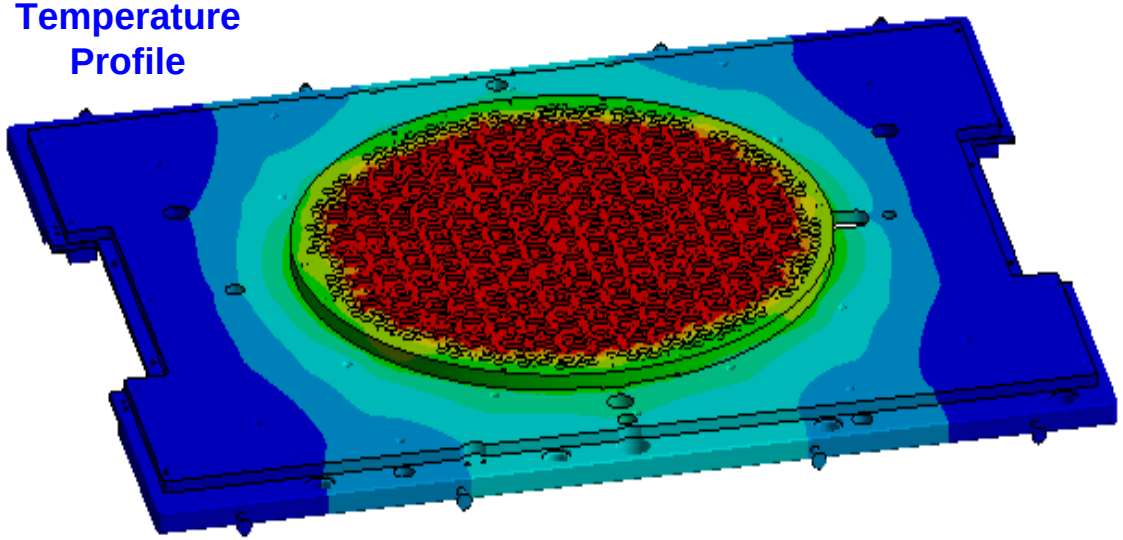
Thermal FEA to Control Card Deflection

- Different thermal FEA simulations were needed to characterize and improve the PC performance by optimizing both:
  - Temperature Profile
  - Deflection due to temperature change on a full stack up PC

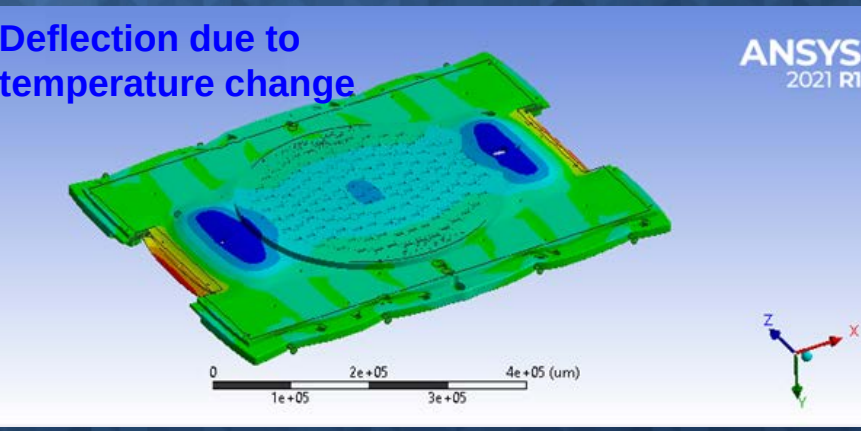
Complete Mechanical Model



Temperature Profile



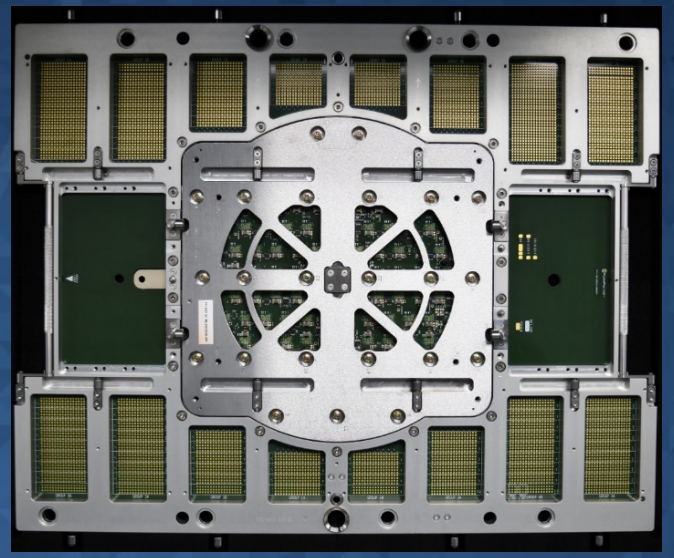
Deflection due to temperature change

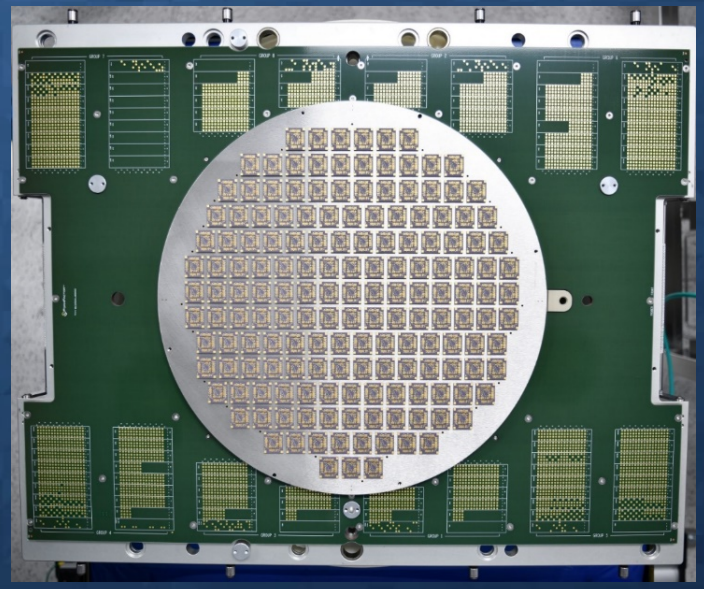


Utilizing thermal FEA probecard deflection is minimized.

FFI TrueScaleMatrix – Full Wafer Contactor Probing

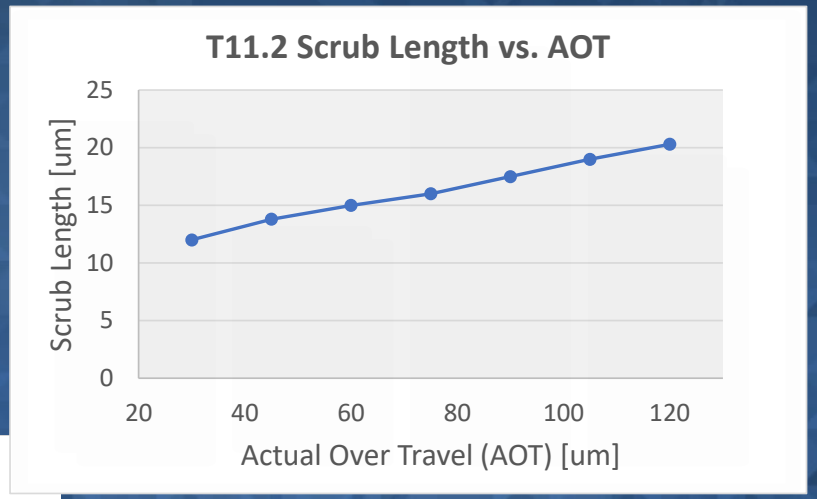
- **FormFactor has developed a FWC solution for DD tester configurations**
  - Based on FFI production proven Matrix full wafer contactor platform
  - Design modifications to both inner TSS and outer TSS
  - Depopulated pogo bank configuration in the test head
- **Features:**
  - Utilizing production proven Matrix architecture
  - 50K+ probe count capability
  - Increased parallelism to > 200 sites
  - Very wide temperature range (meets -40ºC to 150ºC testing requirements)
- **Benefits:**
  - Maximize parallelism, minimize TD count with improved TD efficiency
  - Excellent planarity control ~25um across 300mm array size
  - Keeps stable thermal condition, because of low rate of stepping out of wafer
  - Achieved small super bond pad 30um x 37um at temp range of -40ºC to 150ºC

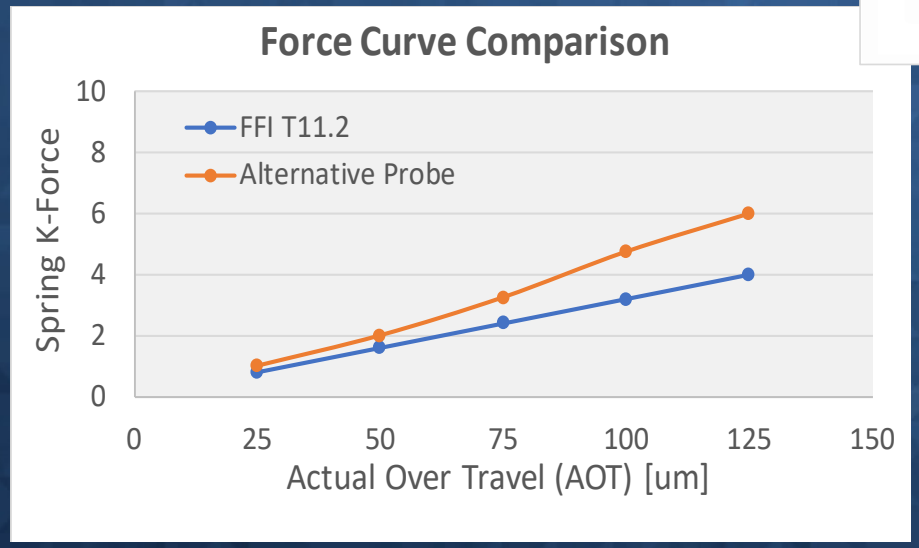


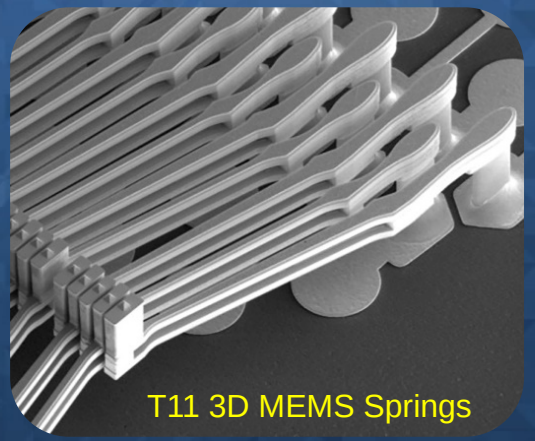


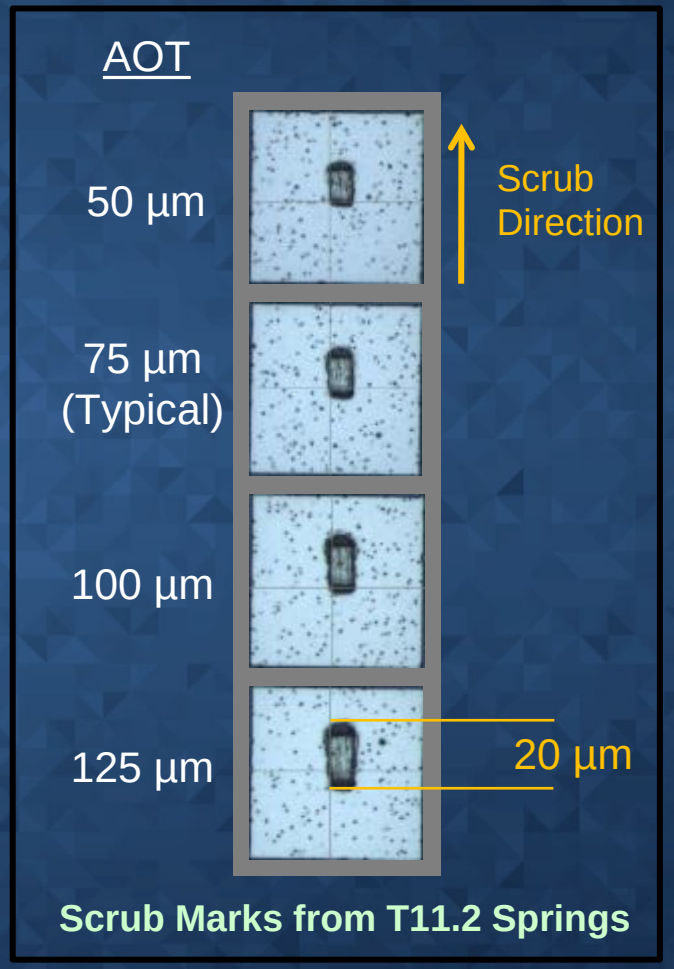
FFI T11.2 3D MEMS Springs

- Low force springs
- Small scrub marks
- Minimized pad impact





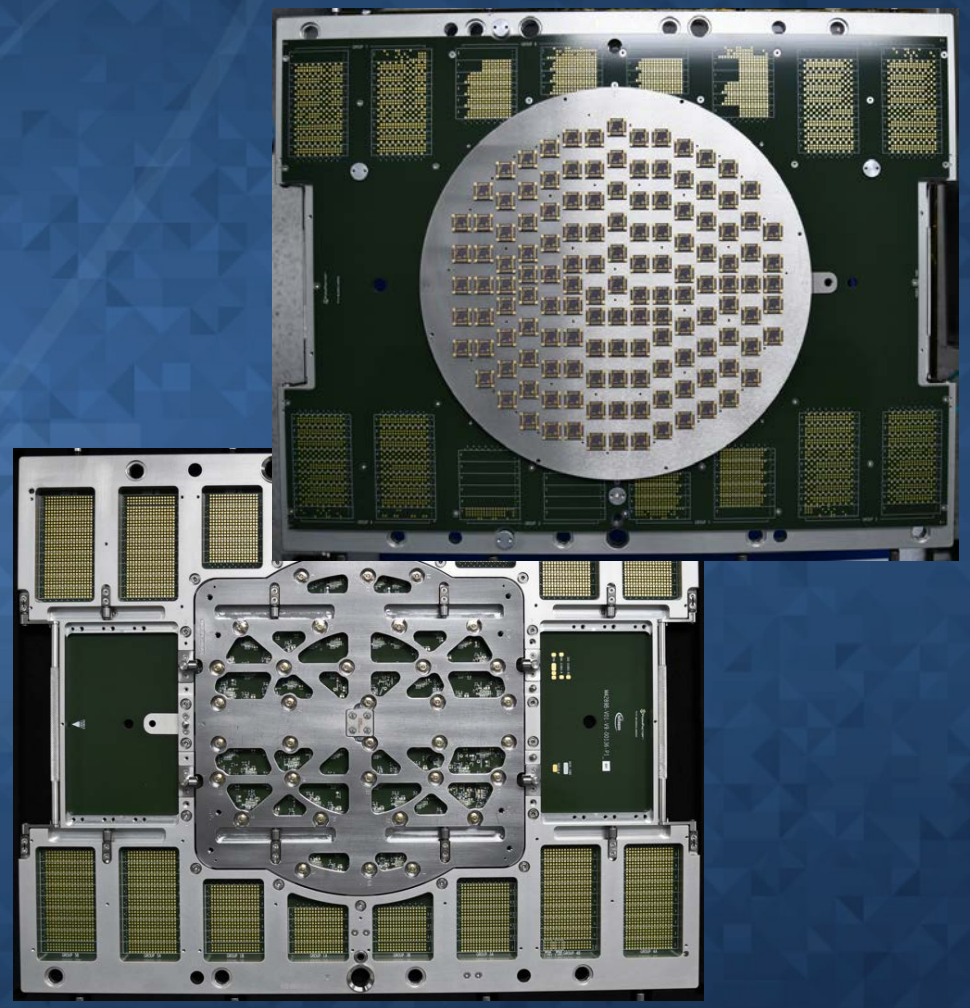




Final Result in Production Test Environment

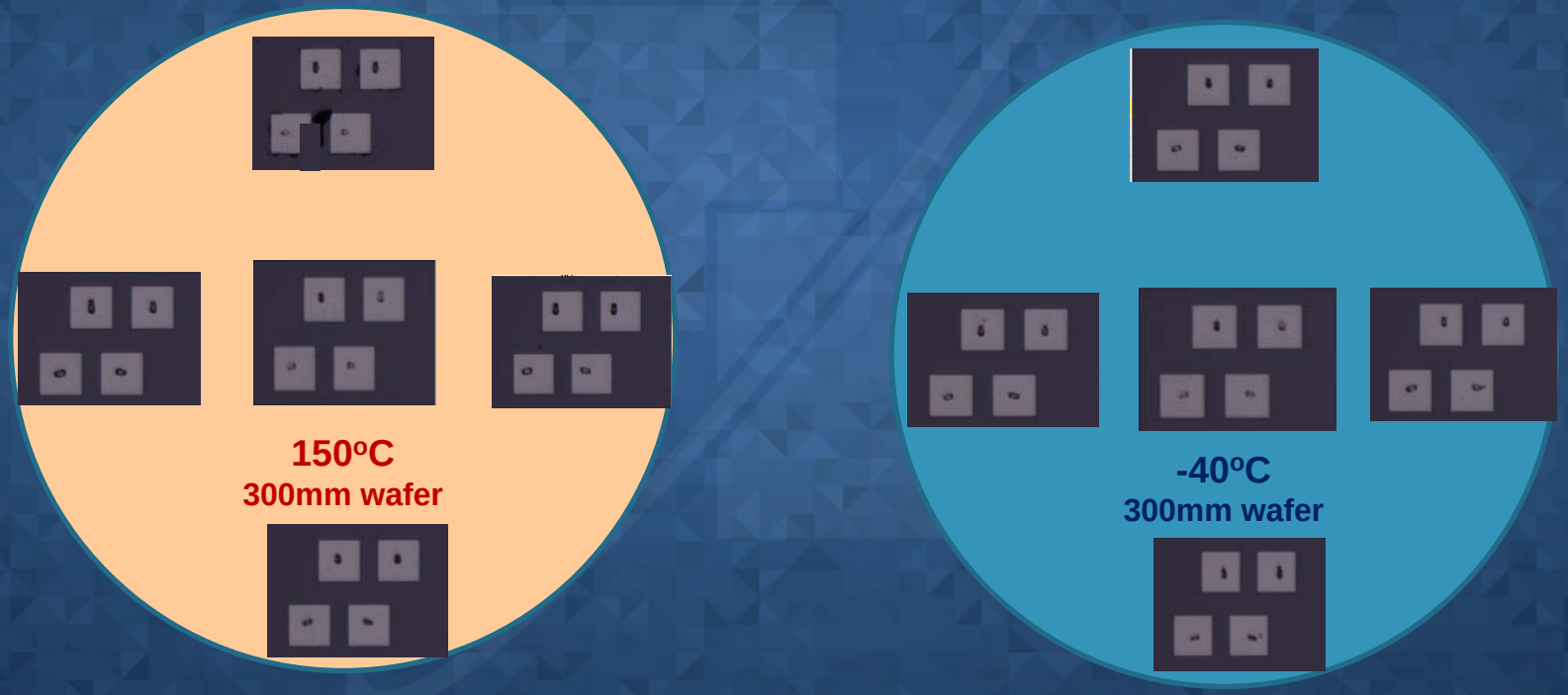
Validation Device Parameters

Test and Probe Card Parameters	
Total Probe Counts	> 20k
Minimum Wafer Pad Pitch	< 100um
Minimum Pad size	75um x 70um
Test Temperature Range	LT:-40°C & HT:150°C
Tester	Advantest V93K DD
Probe Technology	T11.2P
Parallelism	136
TD achieved	6



TrueScaleMatrix Scrub Mark Capability

- **Scrub mark results across full wafer array**
  - Pad size: 70um x 75um
  - Scrub mark data collected on 300mm wafer at 150ºC and -40ºC
  - Ave. scrub mark size: 18um x 10um

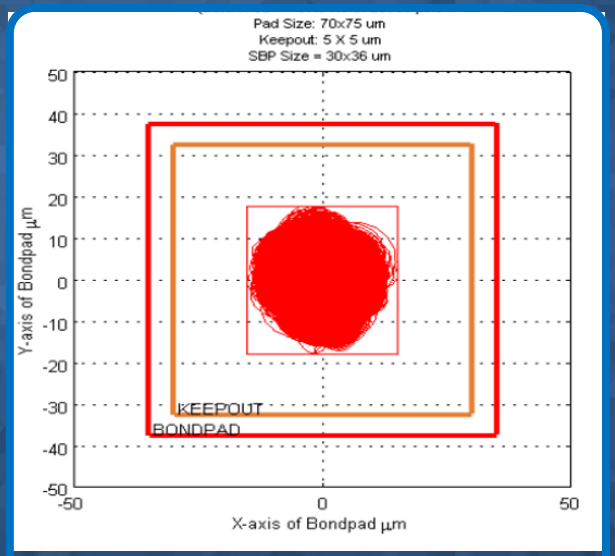


Location of scrub marks at the edge of wafer demonstrates the excellent thermal mechanical performance

Super Bond Pad Capability at Full Temp Range

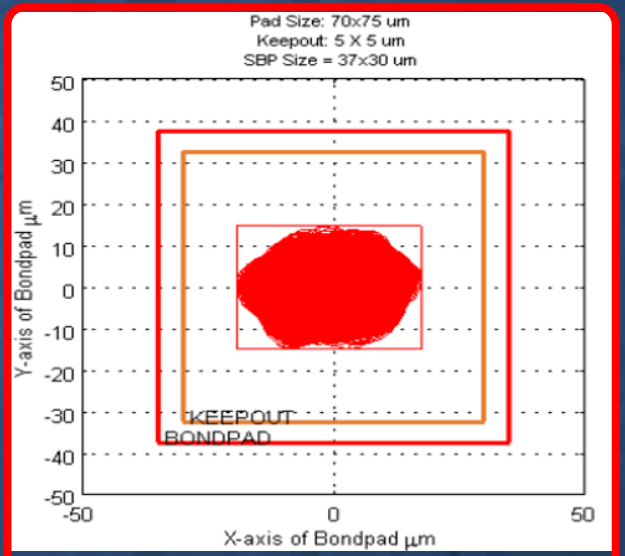
- **Super Bond Pad (SBP):**
  - Consolidation of scrub marks superimposed on top of each other to establish a single virtual pad representing all scrub marks
  - SBP calculation removes systematic errors not associated with the probe card capability

- Parallelism: x136
- Array size : Full Wafer
- Pad size: 70um x 75um
- Keep out: 5um
- 100% of scrubs in pad area meeting the keep out spec



SBP Size = 30x36um

@ -40C



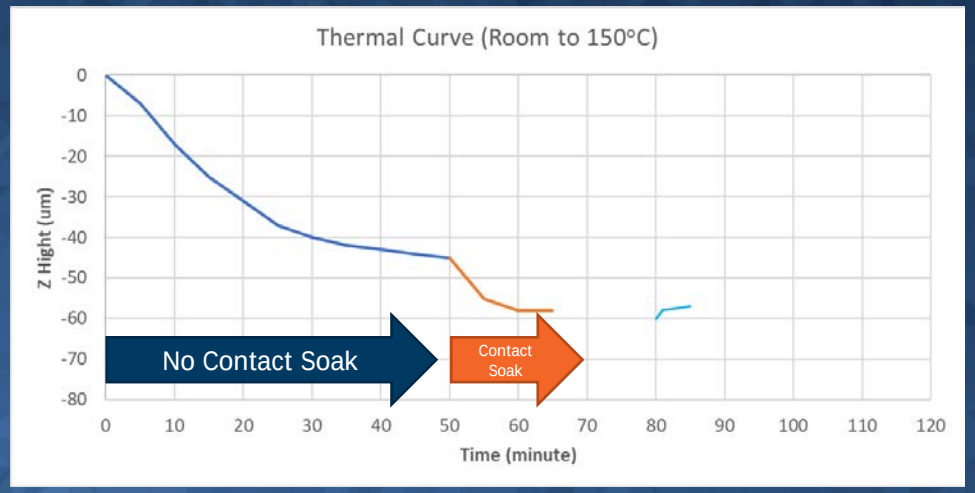
SBP Size = 37x30um

@ 150C

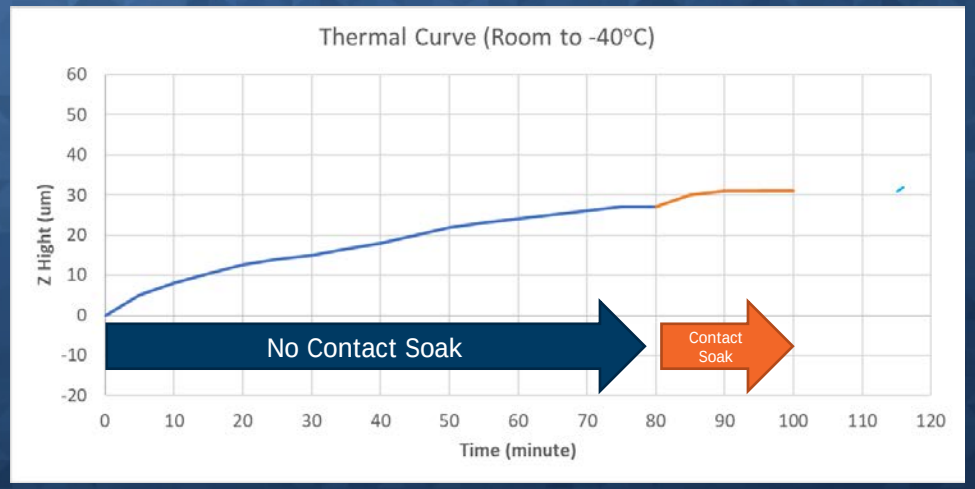
Demonstrated SBP performance <37um per side through entire temperature range

TrueScaleMatrix Thermal Characterization

- **Experiment for Room to 150ºC :**
  - Measuring the change of height over time:
    - Full Wafer TSM with 20k probes
    - Prober preheated overnight before loading PC
    - Non-contact soak at -500um
      - 50 minutes
    - Contact soak to achieve final soak condition
      - 15 minutes and achieves thermal stability
  - **Results:**
    - ✓ Only 58um Z-height movement after complete soak
    - ✓ 2 um Z movement after chuck away from card for 1 min.

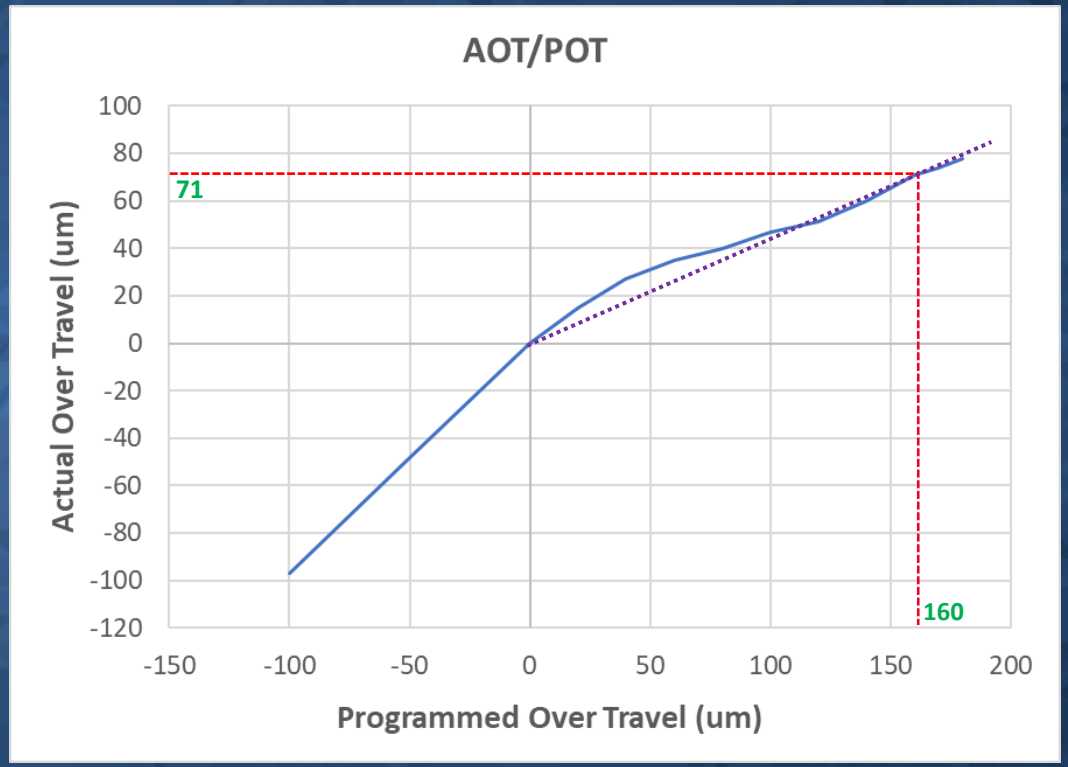


- **Experiment for Room to -40ºC :**
  - Measuring the change of height over time:
    - Full Wafer TSM with 20k probes
    - Non-contact soak at -500um for
      - 80 minutes
    - Contact soak to achieve final soak condition
      - 20 minutes and achieves thermal stability
  - **Results:**
    - ✓ Only 31um Z-height movement after complete soak
    - ✓ 1 um Z movement after chuck away from card for 1 min.



AOT/POT Experiment

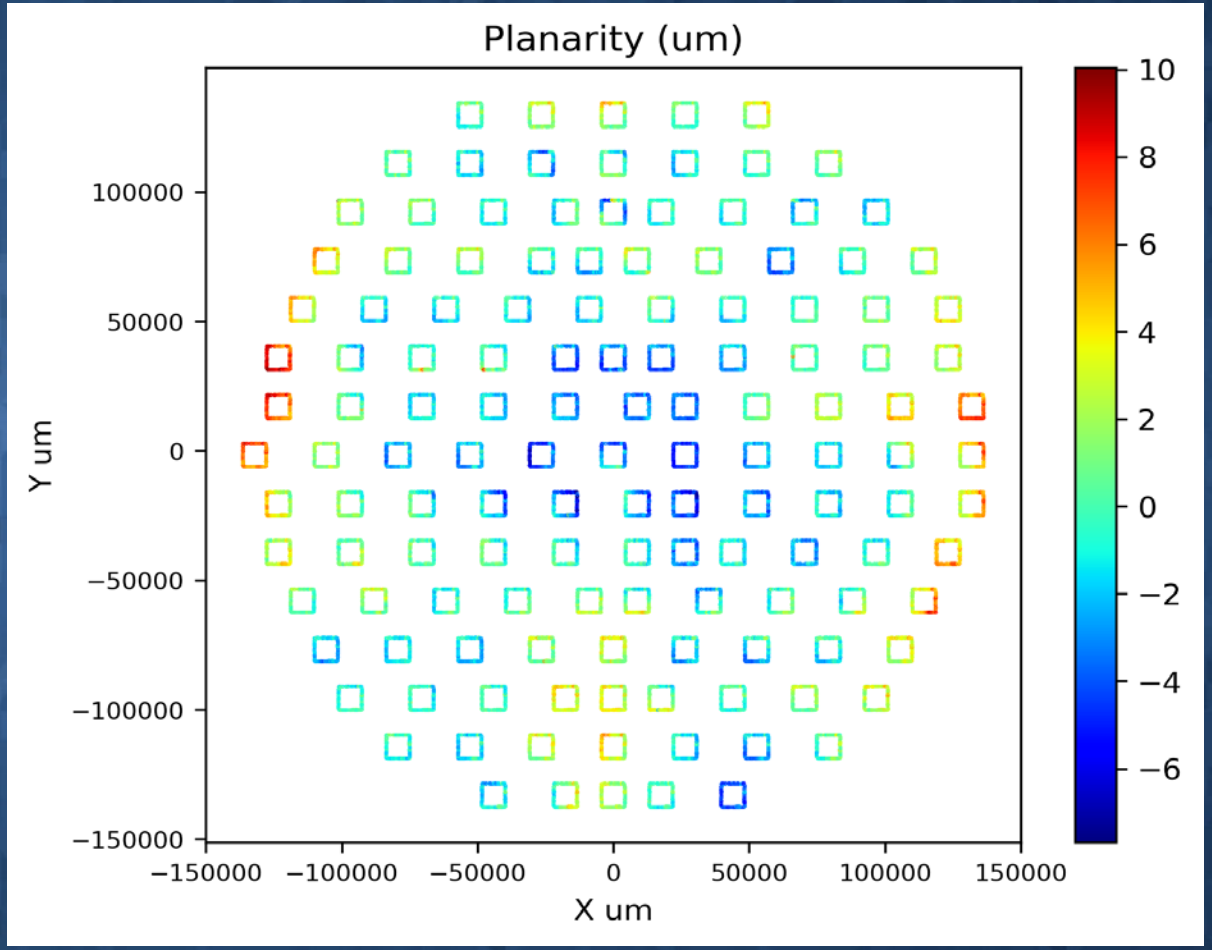
- **Objective:**
  - Measuring the actual overtravel based on the applied programmed overtravel
  - Typically see AOP/POT deviate from 1 as pin count and parallelism increase
- **Experiment:**
  - Field Size: Full Wafer
  - Probe Count: ~20K
  - Tester: Advantest V93K DD
  - Prober: TSK Accretech UF3000 EX-e
- **Results:**
  - At recommended AOT of 70um the POT was measured 160um.
  - AOT/POT of around 44%



TrueScaleMatrix Planarity Performance

- **Measured outgoing Optical Planarity at FFI:**
  - Less than 20um on entire array

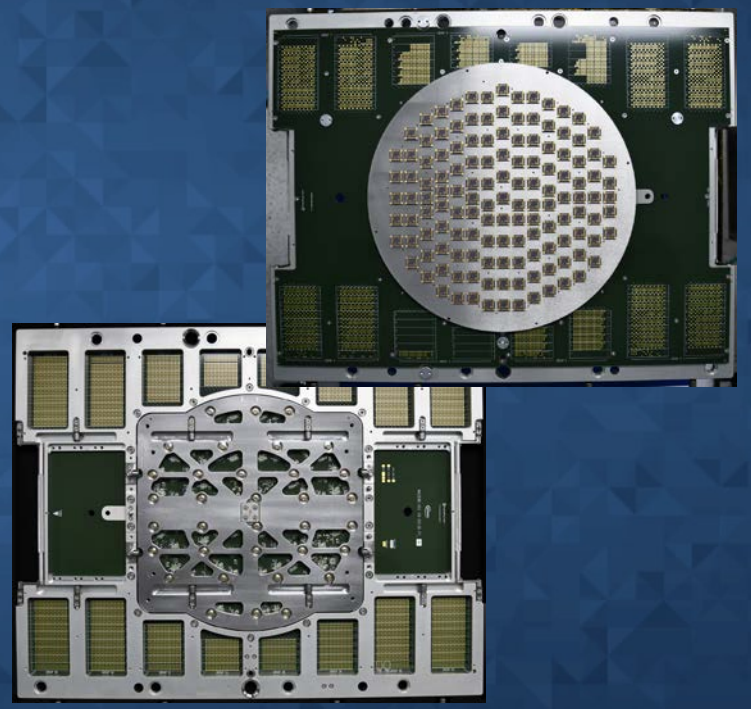
Planarity	Min.	Max.
17.8 um	-7.7um	10.1um



TSM provides excellent planarity of <20um across the full 300mm array

Summary

- Strong automotive IC market growth requiring not only lower test cost but also higher wafer throughput.
- Full wafer contactor solutions enables increased throughput and lowers cost of test compared to compact PH option
  - Increase parallelism to reduce TD count
  - Improve TD efficiency to optimize utilization of tester resources
- FormFactor has a full wafer contact solution for wafer test on V93K Direct-Dock tester
- The TrueScale Matrix 300mm full wafer contactor has been fully qualified by customer for high parallelism automotive device probing



Acknowledgements

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  - Infineon
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    - Alan Liao
    - Cameron Harker